# A CMOS image sensor for Earth observation with high efficiency snapshot shutter

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## Abstract

This article describes a 4 / 16 Mpixel CMOS image sensor with 106 dB efficiency snapshot electronic shutter and 62 dB dynamic range within +/- 3 % linearity. It is monolithic, front side illuminated and processed on plain 0.35 µm process with stitching. This sensor could be an interesting alternative to power consuming TDI CCD sensors in LEO orbit configuration.

## 1. Introduction

With increasing performances, CMOS detectors are gradually becoming attractive for CCD replacement in space applications. First used where the added functionality of CMOS devices is most obvious (e.g. star trackers) [1], they are now competing with observation detectors [2][3]. This paper presents the specification definition, the design and the characterization of a sensor compatible with a LEO orbit mission.

## 2. Application

Spaceborne Earth observation missions implemented by CNES (French space agency) for metric resolution imaging, from Spot satellites to Pleiades, are mostly based upon scanning satellites with camera operating in a puhsbroom mode from a polar heliosynchronous LEO orbit.

Detectors at the focal plane are linear CCD arrays and the 2D image is sequentially built by a line by line integration of photogenerated charges, with a sampling period along the velocity axis matched to the flight duration over the requested ground pitch.

A significant improvement in signal to noise ratio was reached with linear CCD arrays operated in Time Delay Integration (TDI) mode. TDI allows dissociation of the integration time from sampling period along the velocity axis. In a TDI detector the linear array is repeated over N stages. Photogenerated charges are transferred from stage to stage at a speed matching satellite motion, allowing an integration time N times the sampling period. When combined with back thinning technology, which offers high quantum efficiencies, linear CCD TDI arrays are interesting for high resolution earth observation applications [4].

It remains however necessary to investigate and develop alternative solutions to CCD TDI back thinned detectors as they suffer from several drawbacks:

- Clock levels required to operate the CCD need specific driving devices, and lead to high power dissipation,
- The offer in back thinned CCD TDI products is decreasing: it is now limited to only one company in Europe.

The emergence of CMOS image sensors (CIS) and their very fast development for high volume applications bind the actors of the space borne sensing applications to take a look at the performance achievable with CMOS technologies.

For Earth observation applications in the metric resolution range from LEO scanning orbits, one solution is to re-create in CMOS technology the principle of TDI operation, in order to keep the benefit of large integration times decoupled from sampling period. Such a device has been developed by Cypress, under Thales Alenia Space contract [5], proving that the concept is adaptable to CMOS technologies. It shows however some limitations:

- The complexity of the architecture and the readout noise both increase with the number of TDI stages,
- As no charge transfer is performed in CMOS devices, synchronisation between charge transfer and satellite velocity is no more applicable, and MTF degradation has to be taken into account, along the velocity axis. This drawback may be circumvented by oversampling but it adds more complexity to the architecture.

An alternative solution is to use CMOS 2D-arrays. 2D single shot image construction offers several advantages:

- Geometric corrections due to the satellite pointing axis drift, or instability during scanning, are no more required,

- The temporal axis dedicated to the image line by line construction in the case of a linear array is free and available to be used for multispectral imaging or image summation.

A 2D CCD array is operated on the French satellite PARASOL, launched in December 2004, on a LEO polar orbit, to observe the Earth atmosphere with a 5 km ground pitch. In this case the temporal axis is used to explore the spectral domain: 15 narrow band filters and polarizers are placed in succession in front of the 2D CCD array [6].

For metric resolutions, as the time allowed for integration decreases, it becomes necessary to include a mechanism for compensation of the satellite motion during image shot, and a shutter mechanism to prevent illumination during image readout. The conjunction of these two mechanisms is a significant drawback when compared to the TDI solution.

Thanks to the CMOS technology, the shutter function may be performed electronically and thus contributes to the simplification of the overall concept.

Taking into account the capabilities of the CMOS technology CNES decided to revisit the trade-off between 2D arrays and linear arrays, via the development of a snapshot 2D CMOS array for metric resolution Earth observation applications.

The main specifications were established to meet the requirements of a typical 1-meter resolution instrument, on a LEO microsatellite (see Table 1).

| **Requirements** | **Min** | **Typical** | **Max** |
|---|---|---|---|
| Spatial resolution (m) | | 1 | |
| Swath width (km) | 8 | 12 | 20 |
| Altitude (km) | 500 | | 700 |
| Spectral band (nm) | | [480 – 830] | |
| Spectral radiance useful range ($W/m^2.sr.\mu m$) | | [10 – 320] | |
| Optics diameter(m) | 0.3 | | 0.4 |
| Pointing stab. (µrad/s) | | | 100 |
| SNR @ 90 $W/m^2.sr.\mu m$ | 90 | | |
| MTF at Nyquist frequency | 0.1 | | |

Table 1: typical satellite requirements.

To effectively compete with linear array solutions, the design of the CMOS 2D-array detector had to be oriented toward the driving specifications below [7]:

- High quantum efficiency: the snapshot electronic shutter must be included in the pixel at minimum reduction of the fill factor. High QE is requested to keep integration time in the range allowed by pointing stability constraints.
- High shutter efficiency: to maintain the parasitic signal due to a high illumination during readout less than 2 % of the minimum useful signal at low illumination the shutter efficiency must be higher than 86dB.
- High readout frequency: minimise readout time.
- Large array size: the minimum size was specified at 2 k x 2 k, with the objective to reach 4 k x 4 k in order to reach a 12 km swath width with easy arrangement in the focal plane.
- MTF: as CMOS devices operate with reduced voltages, care must be taken in the selection of doping profiles to ensure a correct depletion depth. This is a key requirement to achieve a MTF as good as in CCD over the specified spectral band.
- Charge capacity: the charge capacity has to be designed to cover the full dynamic range and meet the signal to noise specification. The minimum specification was set at 75 $ke^-$.

## 3. Image sensor design

The sensor (Figure 1) has an array of 2004 x 2058 pixels divided into top and bottom sub blocks, enabling simultaneous read out of two rows. Pixel control, row control and biasing blocks are on the left side of the sensor leaving the right side free of bonding pads for abutting. Goal is to build a larger array (4008 x 4018) with the same mask set. As the pixel pitch is 14 µm, both devices are larger than the reticle size, therefore stitching technique is required. The sensor is monolithic and front side illuminated.

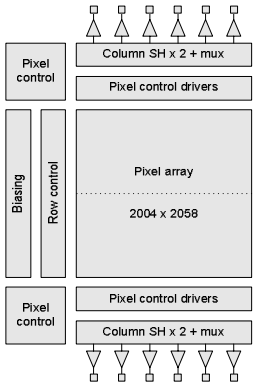


Figure 1: block diagram.

On chip control circuitry is straightforward. Pixel commands, synchronous for all pixels (electronic shutter), are directly controlled off chip. Rows and columns are selected via shift registers. Column sample and hold commands are also accessible directly off chip. Biasing is tuneable via off chips resistors.

The pixel (Figure 2) has 6 transistors and a capacitor. This architecture allows “snapshot” acquisition. If the integration time is longer than the frame read out time, off chip correlated double sampling is possible using

non destructive read out. Two frames are read out: one right after reset and one after the integration time. If the integration time is shorter than the frame read out time, then only "Raw" read out is possible, i.e. single frame read out after the integration time without kTC noise correction. In this case, the pixel array is operated as follows: it is first reset, and after the integration time the signal on the photodiode is sampled on the capacitor. Top and bottom frames are then read out simultaneously in a rolling shutter sequence through respectively top and bottom sample and hold arrays. Integrate while read out is only possible with raw read out.

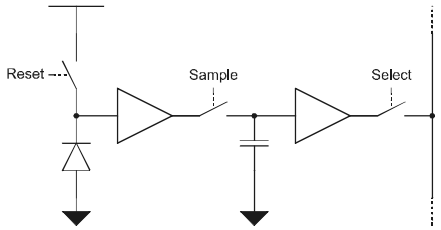


Figure 2: pixel architecture.

Main specifications driving the pixel were full well charge, fill factor, MTF and parasitic light sensitivity (PLS) of the electronic shutter. The PLS is defined as the ratio of the sensitivity when the shutter is closed (read out) and opened (integration time). The initial goal specification, 1/20000, is very low and multiple techniques have been used to meet it.

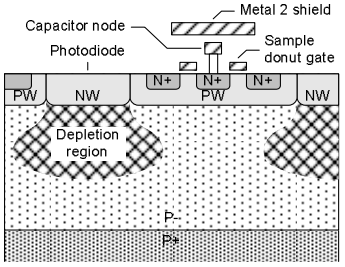


Figure 3: pixel simplified cross section.

One source of PLS is the sample switch. The reversed bias junction of the transistor tied to the capacitor is acting as a second photodiode and corrupts the signal stored on the capacitor in the period between the end of the integration time and when the row is read out. An obvious solution consists in shielding it from light to avoid direct charge generation (Figure 3). This is however not preventing collection of charge generated in the Pwell or the epi layer in the vicinity of the junction, even if the Pwell is repelling free electrons from the epi layer.

In [8], a deep NWell is efficiently used to shield the junction. However, this process step is not available in all technologies and typical large spacing design rules associated are not compatible with relatively small pixel. In addition, it is competing with the photodiode, especially for charges generated deep in the substrate (long wavelengths), resulting in a QE x FF degradation. Instead, the sample transistor has been drawn with a donut shape [9], de facto surrounding the parasitic light sensitive region with a ring of N+ active acting as a shield. This structure is more compact, with an N+ layer smaller and closer to the junction than in [8]. The rest of the pixel is classical. The photodiode is a NWell [10].

During frame read out, rows are sequentially sampled by column sample and hold stages. After the signal is stabilized, the row is multiplexed to 12 analogue outputs. In order to reduce the row blanking time, i.e. the dead time between two rows multiplexing burst required to sample a row onto the sample and hold stages, two rows of sample and hold stages on each side are used alternatively. Together with fast analogue outputs, this is reducing the frame read out time, which at the same time reduces the impact of PLS on the signal.

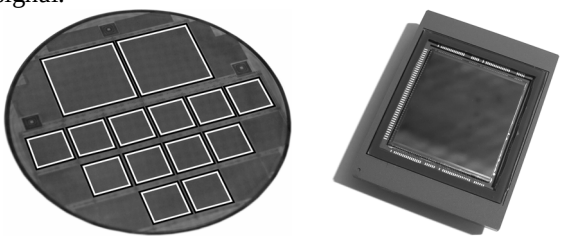

Figure 4: first wafer and device in PGA package.

The device has been processed in the 0.35 µm XFAB technology. In order to reduce costs, both low (4 Mpix) and high resolution (16 Mpix) devices have been processed on the same wafer (2 big and 12 small devices, see Figure 4Figure 4). Currently only the low resolution device has been assembled. Thanks to yield driven design techniques and an intrinsically reliable technology, preliminary estimation of the yield is excellent: on 19 devices assembled from 2 wafers, all are functional and 7 have hardly a dozen off specification pixels. Yield of the big resolution device is then expected to be fairly high.

## 4. Experimental results

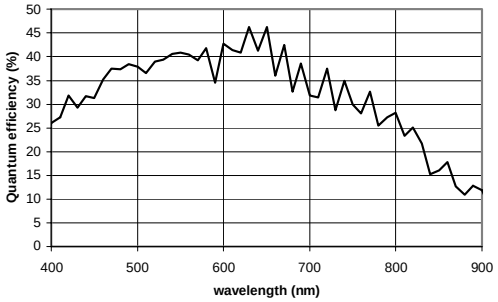


Figure 5: measured QE x FF.

Fine characterization has been completed and results are summarized in Table 2. All specifications have been met or exceeded. Measured external quantum efficiency is given in Figure 5. Peak QE is about 45 % and the roll off starts at about 650 nm, which is consistent with a 7 µm epi. Parasitic Light Sensitivity is at least 10 times better than the specification. A picture taken with the sensor is given in Figure 6.

| Parameter | Value | Remark |
|---|---|---|
| Pixel size ($\mu m^2$) | 14 x 14 | |
| Pixel array | 2004 x 2058 (4008 x 4018) | |
| Pixel type | NWell – 6T | |
| Analogue outputs | 12 (24) | |
| Mean output data rate (Mpps) | 300 (600) | Using only one SH array. |
| Main power supply | 3.3 V | |
| Full well ($ke^-$) | 130 | Flat saturation |
| Full well ($ke^-$) | 80 | Within +/- 3 % linearity |
| Read noise ($e^-$) | 60 | Raw mode |
| Dark current | 0.1 $nA/cm^2$ | |
| QE x FF | 35 % | Average on [470 – 830] nm |
| PLS | < 1/200000 | > 106 dB |
| MTF at Nyquist frequency | > 0.6 | X and Y, on [470 – 830] nm |
| Chip size ($mm^2$) | 29.1 x 31.6 (57.2 x 59.0) | |

Table 2: key specifications and measurements. High resolution sensor values are given in between brackets.

Figure 6: image with off line FPN correction.

## 5. Conclusions

A CMOS image sensor for Earth observation with high efficiency electronic shutter is presented. All specifications have been validated experimentally on a 2 k x 2 k array; 4 k x 4 k arrays will soon be assembled and evaluated.

## 6. Acknowledgement

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[9] Patent pending.

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