CHARGE COUPLED DEVICES FOR IMAGE SENSING

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ABSTRACT. The applications of charge coupled devices (CCDs) in high resolution image sensing will depend on the performance and fabrication yield that can be obtained in devices of various sizes. Much work is proceeding in order to experimentally demonstrate the capabilities of various technologies. One object of this paper is to present some of the design considerations for high resolution charge coupled area image sensors (CCAIS). Results that have been obtained with 106x128 element CCAIS's in both black and white and color television and with a 1500 element linear image sensor will be presented.

I. DESIGN OF AN AREA IMAGE SENSOR

The Frame-Transfer Principle[1] would seem to be an optimum choice for fabricating CCAIS's, so long as back surface thin down and a method of preventing back surface recombination are used. When this is done such a device will have the same very high quantum efficiency of the silicon diode array camera tubes. Any design using front surface illumination, particularly those using lateral transfer into shielded registers, will have a geometrical reduction in sensitivity of ~30-50% plus reflection and absorbtion losses through the semi-transparent electrodes. In the blue part of the spectrum these losses could be especially large, while in the red part, the incident light will penetrate into the undepleted substrate and minority carriers that diffuse to the shielded registers will cause smearing. Thin down should also permit the generation of carriers by the acceleration of electrons emitted from a photocathode for greater sensitivity.

The advantages of the basic Frame-Transfer structure are greatly enhanced by the use of an interlace technique[2] and the introduction of anti-blooming drains.[3] The interlace technique, illustrated in Fig. 1, makes use of the fact that integration of the optically generated carriers under different electrodes in the imaging part of the array causes the center of gravity of the

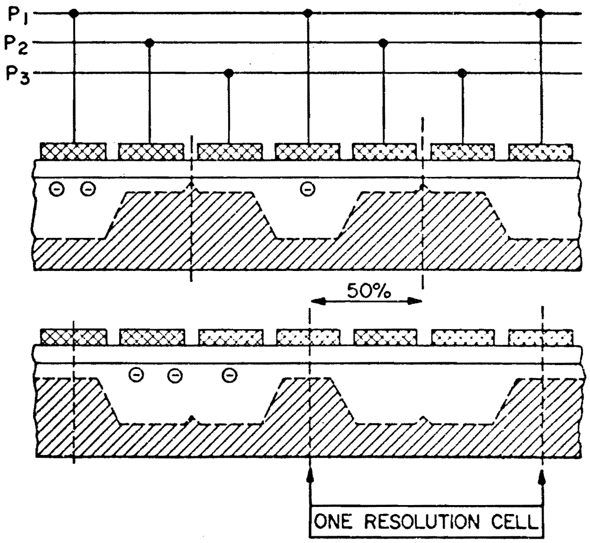

Fig. 1 Schematic illustration of the operation of the interlace principle in a 3-phase CCD.

resolution cell to be displaced. Conventional 2:1 interlace is most readily obtained in a two phase structure but a 3-phase structure can be used, as illustrated in Fig. 1, by integrating Field 1 under the phase 1 electrodes and phase 2 under electrodes 2 and 3 turned on together. A nearly two fold increase in resolution for a given number of elements has been obtained in this way.[2] Thus the total number of vertical elements in both the imaging and storage sections of a Frame/Field Transfer array equals the number of displayed lines.

Anti-blooming drains can be readily incorporated into such an array as illustrated in Fig. 2

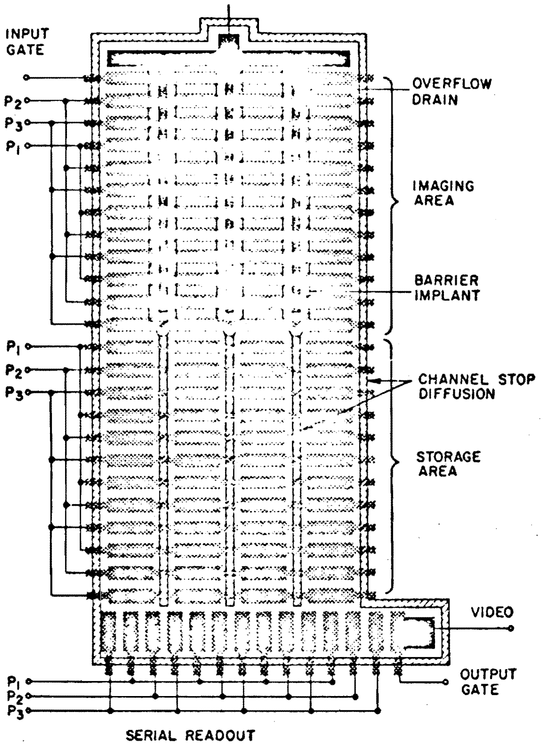

Fig. 2 Schematic plan view of a frame-transfer CCAIS with anti-blooming drains in the imaging area.

A potential barrier formed either by doping the substrate or using a barrier electrode on either side of the overflow drain contains the signal charge in the transfer channel but permits the excess charge generated by highlights to overflow into the reverse biased drain. The use of such a technique has been demonstrated[3] in an experimental CCAIS.

One specific aspect of the design of a CCAIS is to consider the effects of transfer inefficiency ε. Plots[4] showing the effect of $n\varepsilon$, where n is the number of transfers, on the modulation transfer function indicate that $n\varepsilon \leq 0.2$ will cause a negligible degradation in picture resolution. Figure 3 shows the three kinds of charge transfer that occur. Field transfer, which is a low frequency continuous transfer, and line step, which is also low frequency but discontinuous, make up the vertical transfer processes. The maximum $n\varepsilon$ values specified for each are 0.1. Although this applies to the corner resolution it is seen to be a less tight specification when the effect of the interlace is considered. The summary of the field transfer and line step parameters are shown in Tables 1 and 2. In the horizontal case a limit of $n\varepsilon \leq 0.2$ for the

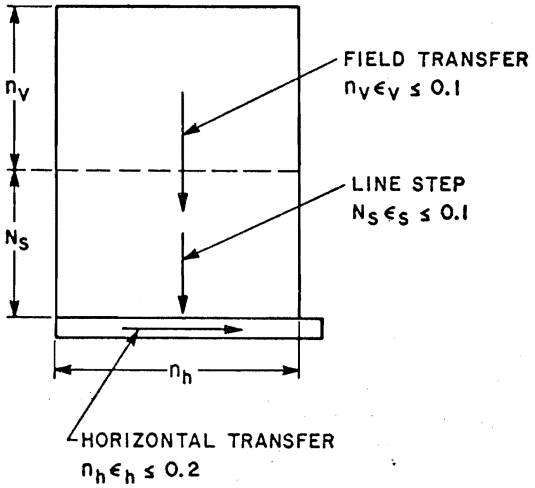

Fig. 3 Illustrating the transfer sequence and limits on the transfer inefficiency product in a frame-transfer CCAIS.

TABLE I - FIELD TRANSFER

	256	525
Number of TV lines		
Number N_V of vertical transfers	3x128	3x262
Minimum transfer frequency	1.5×10^5	3×10^5
To give $N_V\epsilon_V \leq 0.1$, $\epsilon_V \leq N$	2×10^{-4}	1×10^{-4}
Predicted values of ϵ_V ($N_{ss} = 2\times10^{10}$ cm^{-2} eV^{-1})	$2\text{-}5\times10^{-4}$	
Measured values of ϵ_V (12.5 µm surface n-channel)	$2\text{-}5\times10^{-4}$	

TABLE II - LINE STEP

	256	525
Number of TV lines		
Number N_s of line steps	128	262
Minimum transfer frequency	5×10^4	1×10^5
To give $N_s\epsilon_s \leq 0.1$, per step $\epsilon_s \leq$	8×10^{-4}	4x10-4
Predicted values of ϵ_s ($N_{ss} = 2\times10^{10}$ cm^{-2} eV^{-1})	$\sim 1\times10^{-3}$	

TABLE III - HORIZONTAL TRANSFER

	256	525
Number of TV lines		
Number N_H of horizontal transfers	3x212	3x525
Transfer frequency	2×10^6	8×10^6
To give $N_H\epsilon_H \leq 0.2$, $\epsilon_H \leq$	3×10^{-4}	1×10^{-4}
Maximum electrode length (surface n-channel)	16-20 µm	7-10 µm
Predicted values of ϵ_H ($N_{ss} = 2\times10^{10}$ cm^{-2} eV^{-1})	$\sim2\times10^{-4}$	$\sim2\times10^{-4}$
Measured values of ϵ_H (25 µm wide surface n-channel)	2×10^{-4}	

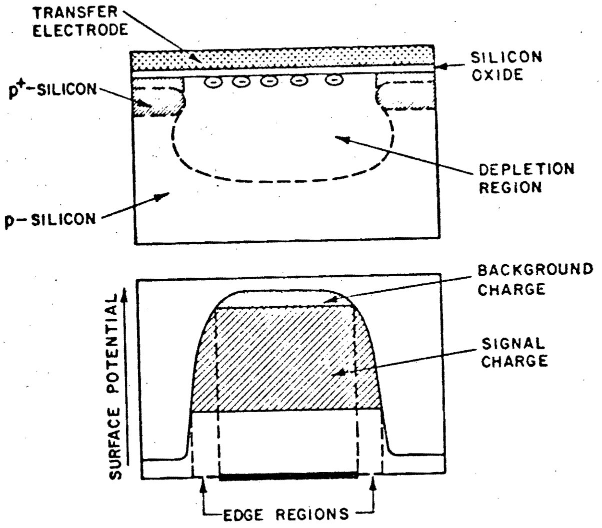

Fig. 4 Illustration of the edge-effect in a surface channel CCD.

total length of the read-out register is assumed and the consequences of this are seen in Table 3. Comparison of the necessary ε values with experimentally obtained ones indicate that the best surface channel devices are just adequate so long as a small background charge is used. The major limit is the edge effect illustrated in Fig. 4, which shows how larger charge packets spread over a larger area of the interface. In the buried channel device, the larger charge packet always spreads over a much larger volume of silicon, but the indications are that the density of bulk taps is such that the net effect is a smaller transfer inefficiency. In addition no background charge is necessary or is even possible. Referring to Table 3 it is also seen that the maximum electrode length is limited to 7-10 µm in a 500x500 array. The higher bulk mobility and the larger fringing fields in a buried channel device ease this design limitation considerably.

An aspect in which surface and buried channel devices vary significantly is in the amounts of transfer noise. In a surface channel device, the noise is a relatively fixed amount independent of the size of the charge packet, whereas in the buried channel device it varies, more favorably, with the size of the charge packet being transferred. For typical values in a 500x500 device, the peak signal to noise ratio for a surface channel device would be on the order of 50 dB, whereas a buried channel device should have this as a worst case value only at small signal levels.

TABLE IV - PULSE PROPAGATION DELAY ALONG PARALLEL TRANSFER ELECTRODES

Phase shift of component of frequency $F = X(\pi_F R_\square C_o)^{1/2}$

$R_\square$ = Resistivity per square of electrode metallization

C_o = Oxide capacitance per unit area

X = Half width of array, which is assumed addressed from both sides

ASSUME PHASE SHIFT $< \pi/10$

AND FIELD TRANSFER TAKES PLACE DURING VERTICAL RETRACE

FOR <u>256</u> LINE SYSTEM $\boxed{R_\square < 100\Omega}$

FOR <u>525</u> LINE SYSTEM $\boxed{R_\square < 12\Omega}$

Another important consideration in fabricating large area image sensors is the delay and attenuation introduced into the transfer pulses as they propagate along the electrodes. Table 4 indicates that for a 500 line system the resistance per square of the electrode material should be less than 12Ω. A 500x500 CCAIS will cover about 3.6 cm^2 of silicon and an electrode structure that will give a low defect density over such an area is another very stringent requirement.

II. CCAIS IN COLOR TELEVISION CAMERAS

If the use of CCAIS's is attractive in black and white television, then they are potentially many more times attractive in color television. Since a color camera using CCAIS's could be designed to be more compact than present black and white cameras, it becomes possible that new applications, where color information could be used, might be realized. As compared to existing color cameras, a color camera using CCAIS's would have no problems of alignment and registration, since a fixed geometry device is used, greater sensitivity, zero lag, lower power dissipation and drift free, unattended operation. An experimental three device camera using 128x106 element CCAIS's[5] has already been demonstrated[6] and Fig. 5 shows a photograph of the camera.

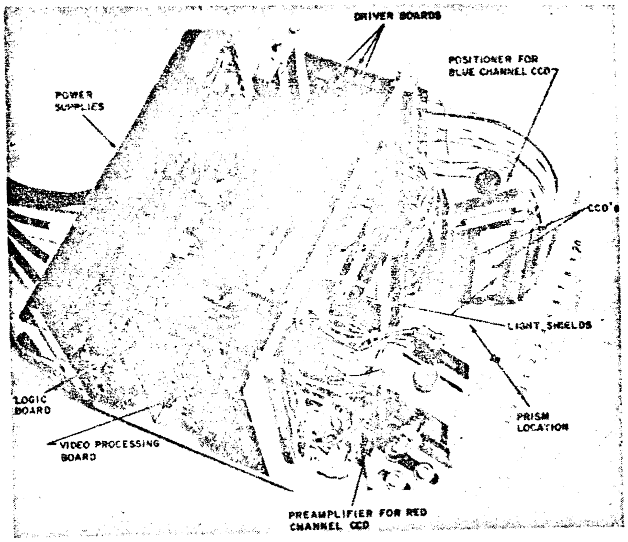

Fig. 5 Photograph of exploratory color television camera using CCAIS's with the light separation prism removed. The scale is in centimeters.

III. LINEAR IMAGE SENSING

A 1500 element gated dual-linear 4-phase charge coupled image sensor has been made and demonstrated. It was a surface channel device but the transfer inefficiency was less than 10^{-4}. Figure 6 shows a photograph of some printed material scanned with the device.

IV. ACKNOWLEDGMENT

The results discussed in this paper arise as a group effort and other major contributors were W. J. Bertram, T. A. Shankoff and E. J. Zimany, Jr.

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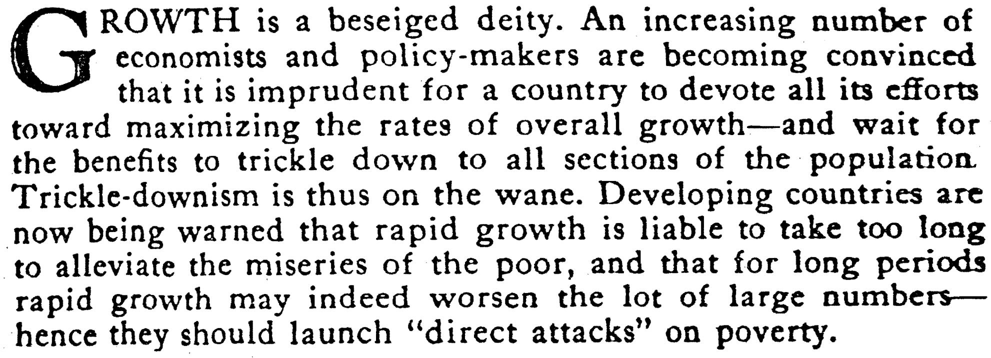

GROWTH is a beseiged deity. An increasing number of economists and policy-makers are becoming convinced that it is imprudent for a country to devote all its efforts toward maximizing the rates of overall growth—and wait for the benefits to trickle down to all sections of the population. Trickle-downism is thus on the wane. Developing countries are now being warned that rapid growth is liable to take too long to alleviate the miseries of the poor, and that for long periods rapid growth may indeed worsen the lot of large numbers—hence they should launch "direct attacks" on poverty.

Fig. 6 Copy of printed material read using a 1500 element linear image sensor. The self-scan direction is horizontal.

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