Design and Operation of Buried Channel Charge-Coupled Devices

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INTRODUCTION

A buried n-channel charge-coupled device[1,2], shown schematically in Figure 1, has a shallow n-layer between the insulating dielectric material and the p-type substrate of the conventional surface n-channel device structure. When the doping level and the depth of the layer are chosen properly, an energy minimum is formed in the layer by the depletion of the free carriers from the layer. Signal electrons are then stored and transferred in the bulk silicon without being trapped at the interface-states.

The absence of trapping phenomena due to interface-states increases the transfer efficiency and also eliminates noise coming from bias charge and the interface-states[3]. This allows one to take full advantage of the charge-coupled device concept.

In this paper, properties of the shallow n-layer are studied, both experimentally and theoretically, using an implanted gated diode as a test vehicle. The results are compared in terms of operating voltages and transfer efficiencies with those obtained by actual CCD operation.

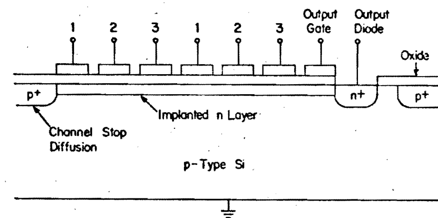


Figure 1. Schematic Diagram of a Buried n-channel CCD

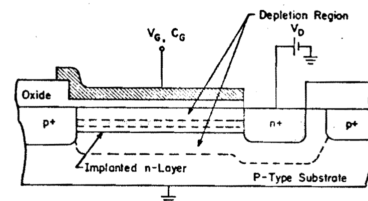


Figure 2. Cross-Section of an Implanted Gated Diode

C-V CHARACTERISTICS OF AN IMPLANTED GATED-DIODE

A cross-sectional view of the implanted gated-diode is shown in Figure 2. The shallow n-layer underneath the gate oxide is obtained by implanting donor ions through the gate oxide. The C-V characteristics of this structure depend on the energy of the ion beam and the dosage of the ions during the implantation. An example is shown in Figure 3. This C-V characteristic can be interpreted using the depletion approximation. When the gate voltage has a large positive value and the diode is biased, electrons are accumulated at the interface between the oxide and the n-layer. If the gate voltage is reduced, deep depletion of the n-layer takes place and, as the depletion width increases, a point will be reached at which the implanted n-layer is completely depleted (punch through). This point is observed by a sudden drop in gate

capacitance. At the time of punch through, the maximum potential in the n-layer (φ_{max}) is approximately equal to the voltage applied to the diode. Also, the position of the potential maximum can be found from

$$d = \text{channel-depth} = \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot X_{ox} \cdot \left(\frac{C_{ox}}{C_G} - 1\right)$$

where d is the distance between the interface and the potential maximum, C_G is the gate capacitance just before punch through and X_{ox} is the oxide thickness. After punch through, φ_{max} is independent of the diode voltage and controlled by the gate-to-substrate voltage only. For large negative values of V_G, the n-layer is inverted at the surface and the surface potential (φ_s) becomes zero. The potential difference between the maximum potential and the surface potential ($\varphi_{max} - \varphi_s$) can be obtained approximately by observing that diode voltage which is just large enough to punch through the implanted layer.

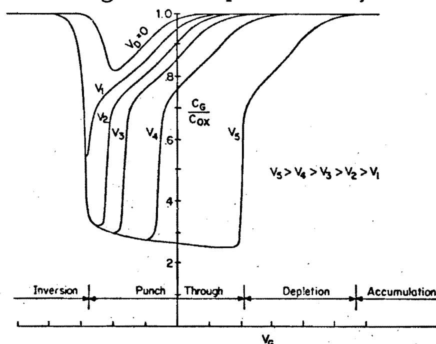
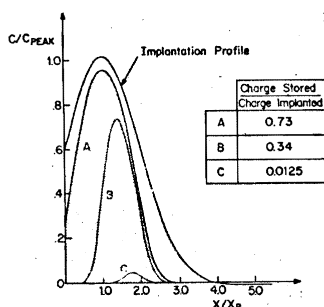


Figure 3. C-V Characteristics of an Implanted Gated-Diode



	Charge Stored / Charge Implanted
A	0.73
B	0.34
C	0.0125

Figure 4. Electron Distribution for the Implantation Shown in Figure 3

ONE-DIMENSIONAL CALCULATION

In order to understand the properties of the shallow n-layer in more detail and also to find the charge storing capability of a CCD with such a layer, the one-dimensional Poisson's equation has been solved numerically. The distribution resulting from an implantation process is approximately

$$C(X) = C_{peak} \exp\left[-(X - X_p)^2 / 2\sigma^2\right]$$

where X_p is determined by the energy of the ion-beam and σ is determined by the implantation energy and subsequent high temperature processes[4]. Figure 4 shows the implantation profile and electron distribution for the case shown in Figure 3. These electron profiles show several important results. First, the depletion approximation used to interpret the C-V characteristics is not valid in a strict sense. This is because the width of the electron profile is not large enough compared with the extrinsic Debye length in that region. However, it has been found that the position of the potential maximum and $\Delta\varphi = \varphi_{max} - \varphi_s$ obtained from the calculation are in reasonable agreement with the value from the C-V characteristics. Secondly, as the number of electrons stored in the potential well increases, they are distributed closer to the interface and $\Delta\varphi$ becomes smaller. This gives an upper limit to the charge storage capability.

In Figure 5, φ_{max} and φ_s are plotted as a function of charge stored. One can impose a limit on $\Delta\varphi$ such that

$$\Delta\varphi = \varphi_{max} - \varphi_s = m \cdot \frac{kT}{q}$$

where m is a numerical factor which has to be chosen to insure isolation of the signal charge from the interface-states. If one chooses m = 10,

$$\Delta\varphi \geq 0.26 \text{ volts}$$

at room temperature, and the charge storing capability for the particular implant is

$$Q/Q_{imp} \leq 0.42$$

where Q_{imp} is the charge associated with

implanted donors. If the amount of charge stored exceeds this limit, the device can no longer be considered as a true buried channel structure because of the interaction between the stored charge and interface-states.

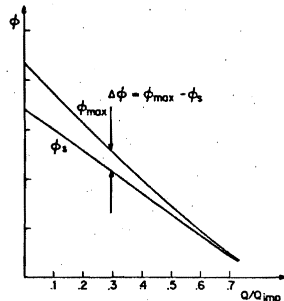


Figure 5. Variation of φ_{max} and φ_s with Charge. This plot is for the implantation shown in Figure 4.

CCD OPERATION

From the discussion in the second section, it is clear that the clock voltages applied to the CCD gates should be larger than the value which gives inversion of the n-layer. The high level of the clock voltages have been found experimentally to be independent of the diode voltage. This is due to the difference between the gated diode and the actual CCD structure. In a CCD, there are many gates which are pulsed while, in the gated diode, a single gate is biased with D-C voltage. Moreover, the clocking sequence in CCD operation is to move the electrons to the output diode. As a result, the electrons associated with the implanted impurities are pumped out during the initial period of clocking and punch through of the n-layer is achieved with the clock voltages higher than predicted from the C-V measurements.

Once the punch through of the n-layer is achieved, controlled amount of charge can be injected into the device either electrically or by light. When light is incident on the device, electron-hole pairs are generated and the electrons are collected in the potential well. The holes generated deep in the substrate are absorbed in the substrate. On the other hand, the holes generated near the interface will travel toward the interface where the potential is lower and then to the substrate through the p^+-channel stop region.

As discussed in the third section, the performance of the buried channel device depends on $\Delta\varphi = \varphi_{max} - \varphi_s$ which is determined by the implanted n-layer. If $\Delta\varphi$ is too small, some of the charge stored will be trapped at the interface-states thereby reducing the transfer efficiency. This effect is illustrated in Figure 6 which shows two pictures taken with 500 element linear imaging devices. In these pictures, the result of poor transfer efficiency can be observed by comparing the resolutions on the lefthand side and the righthand side. This is possible since the charge packets for the righthand side of the picture go through a large number of transfers. The two devices used in Figure 6 have different implanted n-layers so that $\Delta\varphi$ in the absence of signal charge is larger for picture (b) than (a). The righthand side of picture (a) has such a poor resolution that the device is almost useless as a high resolution imaging device. In comparison, picture (b) has high resolution all across the picture indicating that a higher transfer efficiency is associated with the larger $\Delta\varphi$ difference.

Another important parameter for charge storing capability is the depth of the potential maximum (d). If one assumes that the charge is stored at the point of the potential maximum without any spread, the change in φ_{max} due to the presence of signal charge can be estimated by

$$\varphi_{max}(Q = 0) - \varphi_{max}(Q = Q_1) = \frac{Q_1}{C_{eff}} \quad *$$

where C_{eff} is the series combination of the oxide capacitance and depletion capacitance of width d. For a larger storing capability, therefore, one would like to have a thin gate oxide and a very shallow buried channel. On the other hand, a deeper channel may be preferable for high speed operation of the device because of the higher fringing fields[5] which result in this mode.

CONCLUSION

A buried channel charge-coupled device offers many advantages over a surface channel device with only a slight complication in fabrication, i. e., the addition of

* In actual device, the signal charge is distributed with finite width and C_{eff} is a function of charge stored. This generally gives higher charge storing capability than estimated.

(a)

(b)

Figure 6. Pictures Taken with 500 Element Linear Imaging Device. Picture (a) has poor transfer efficiency with small $\Delta\varphi$.

the implantation process to form a shallow n-layer. The performance of the device is sensitive to the properties of the n-layer which can be characterized by two parameters:

(1) The potential difference between the channel region and the interface = $\Delta\varphi$.

(2) The depth of the channel region = d.

Qualitatively, larger $\Delta\varphi$ and smaller d will give higher charge handling capability. However, a device with larger d will have higher fringing fields. The ultimate choice of the parameters will depend on the particular systems requirements, such as clock voltages, speed, and charge storing capability.

A buried channel CCD can be considered as an analog shift register with wide dynamic range. This opens up new application areas including low light level imaging, analog delay lines and analog matched filters. It is expected that new applications, not thought of so far, will materialize in the future.

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