DESIGN, FABRICATION, AND PERFORMANCE OF A 128 X 160 ELEMENT CHARGE-COUPLED IMAGE SENSOR*

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ABSTRACT

Three types of organization for solid state image sensors are discussed; a horizontal line-by-line system; a separate photocell with interleaved readout registers system; and the vertical frame transfer system. The vertical frame transfer system is the most useful system at the present time for exploring the problems associated with the actual manufacture of very large solid state image sensors. The design considerations for a 128 x 160 element (275 x 375 mil pellet) three-phase charge-coupled image sensor are discussed. The sensitivity, spectral response, resolution and other performance data are given for operation at standard TV frame rates.

INTRODUCTION

The need for a self-scanned solid state image sensor to replace beam scanned devices has served to focus much research effort on the use of the charge-transfer concept for imaging purposes. Rapid advances are being made in the size and quality of image sensors employing the charge-transfer concept. Because of the large physical size of the pellet required for moderate and high resolution image sensors, and because of certain constraints imposed by device physics, the design of a large charge-coupled image sensor presents some unique problems.

The development of a solid state image sensor that is compatible with a beam-scanned vidicon requires: fabrication of a pellet that is at least five times larger in area than current commercially produced LSI devices; defect-free and blemish-free processing technology equal to that used for the silicon vidicon; clocking of large MOS-like structures at speeds up to 10 MHz.

In order to illuminate some of the real-world problems associated with making very large area image sensors, a device having 60,000 mil^2 of active area (thin oxide) was built and tested. Its design, fabrication and performance are described below.

DESIGN CONSIDERATIONS

In a standard beam-scanned vidicon, the method of extracting video signals from the target is, by convention, restricted to a line-by-line rectangular raster scan. This restriction does not exist in digitally scanned solid state image sensors. In fact, quite the opposite is true. A large variety of new system organizations are possible in the design of a solid state image sensor. Although the tradeoffs are not always well defined, some of the factors that must be considered in evaluating each system design are:

1. The total number of transfers, n, that a charge packet must undergo at various clock rates.

2. Susceptibility to shading and preferential degradation of resolution as a function of n, the number of transfers, if transfer efficiency is less than ideal.

3. Ability to obtain standard TV compatibility (i.e., interlace).

4. Problem of efficiently getting light to photosensitive area.

5. Problems associated with wafer

thinning (if required).

6. Total silicon area required for given resolution.

7. The size of the basic unit cell (maximum and minimum).

8. Number of steps in fabrication process.

9. Dynamic range, blooming, spectral response, etc.

Three types of charge-transfer imaging systems are shown in Figs. 1, 2 and 3. (Other organizations exist and may, in the long run, prove to be useful.)

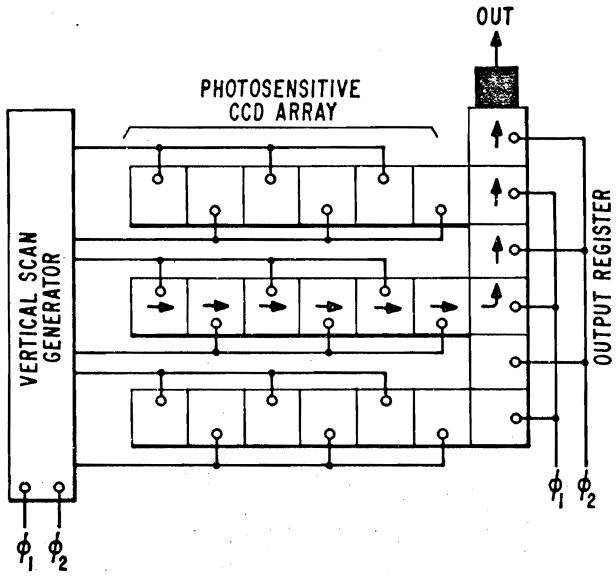

Fig. 1 Horizontal Line-By-Line System

Fig. 1 shows a horizontal line-by-line system. The individual charge-transfer registers serve the dual purpose of photodetection and readout. The photogenerated signals in each horizontal line of the array are read out sequentially when the vertical scan generator addresses that particular row. As the photogenerated carriers arrive at the end of a particular row they are fed into an output register which transfers them to a low capacitance output. A system of this type was built at RCA Laboratories in 1970 in a 32 x 44 element array using bucket-brigades.[1-5] The unit cells were 3 mils x 3 mils. As the unit cell size becomes smaller, it becomes increasingly difficult from a topological standpoint to get two separate clock lines to each row.

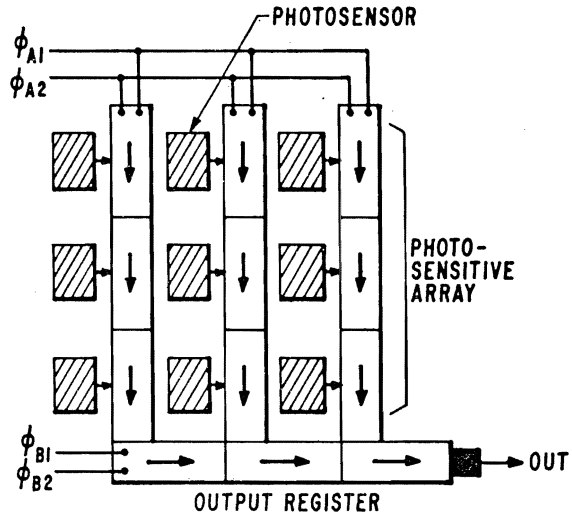

Fig. 2 Separate Photocell With Interleaved Readout Register System

Fig. 2 shows a second type of organization for an image sensor system.[6] In this system, the photodetection and charge-transfer readout functions have been separated. This has great potential in that the photodetector can be optimized for a specific purpose (e.g., IR photodetectors may be built). However, from a practical standpoint, the interleaving of the charge-transfer register and the closely spaced photodetector array presents some problems in optical shielding. This problem would be particularly troublesome if it became necessary to thin the wafer and image through the back thereby requiring the optical shield on the back surface to be aligned with the structure on the front surface.

Fig. 3 shows a third type of system — the frame transfer system as originally described by Bell Labs.[7] In this system, as in Fig. 1, the charge-transfer register is used for both photodetection and for charge readout. The photogenerated signals are transferred in parallel during the vertical retrace period to a temporary storage region. They are then read out one line at a time via the output register. From a topological and processing standpoint this system offers the simplest structure to fabricate. However, the total device area must be increased slightly to include the space for the frame

store. A 45 x 60 element (90 x 60 when vertically interlaced[8]) sensor of this type was built at RCA[9,10] in 1971. More recently (1972), a 128 x 160 (256 x 160 when vertically interlaced) sensor has been built and tested. The details of this sensor are given below.

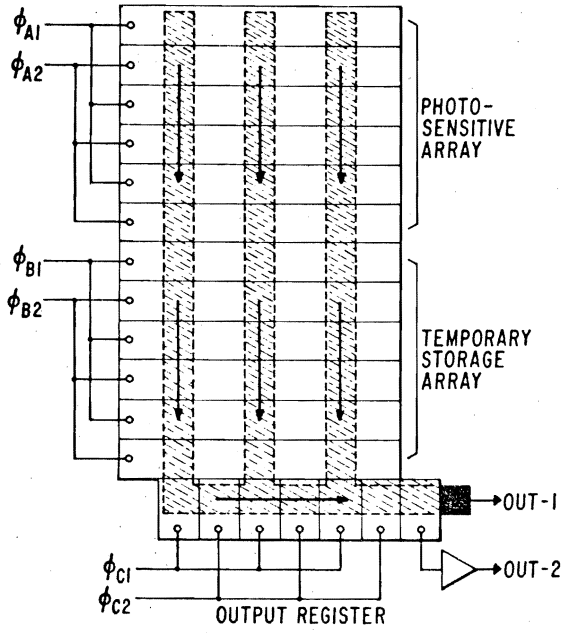

Fig. 3 Frame Transfer System

Two-phase clocks were used to illustrate the systems shown in Figs. 1, 2, 3. The same systems can be built using three and four phase clocks. As a matter of fact, the frame transfer system (Fig. 3) is easier to fabricate in large areas as a three-phase single level metallization system. Building this system in the comparatively simple three-phase technology serves as a vehicle to explore some of the generic problems of mask making and fabrication of very large area arrays.

DETAILS OF 128 X 160 DESIGN

Fig. 4 shows a schematic layout of the 128 x 160 element (256 x 160 when vertically interlaced) three-phase charge-coupled image sensor. The total active area of the device is 60,000 mil^2 and the pellet itself is approximately 103,000 mil^2 (275 x 375 mils). Fig. 5 shows the relative size of the 45 x 60 array and the 128 x 160 array. If a 100 x 100 element array were built to the

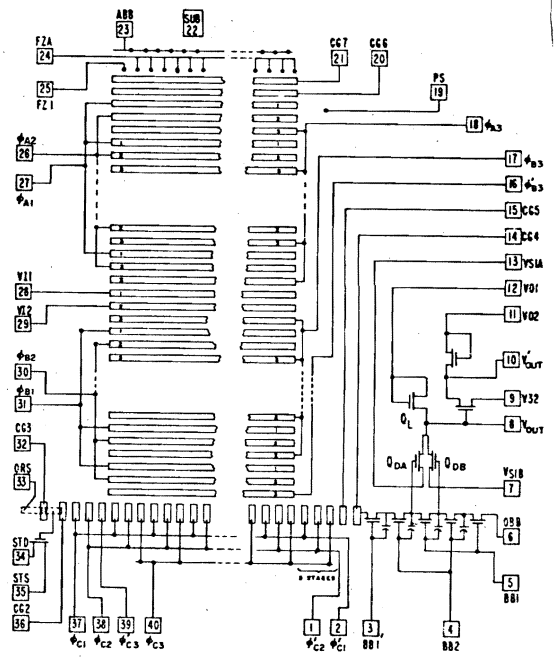

Fig. 4 Schematic of 128 x 160 Element, Three-Phase, Charge-Coupled Image Sensor

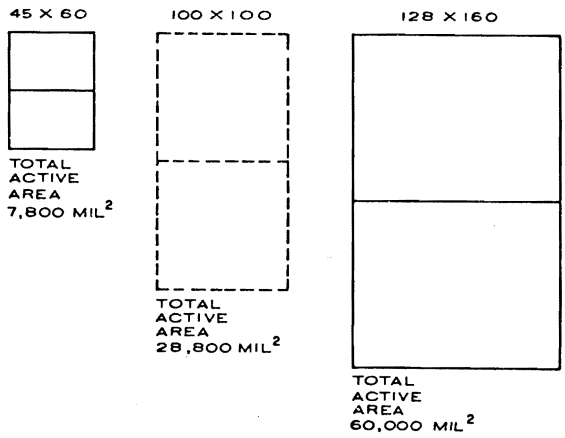

Fig. 5 Comparison of Array Sizes

same design it would appear as shown in the center of the figure. Table I lists some of the specifications of the 128 x 160 array.

128 x 160 AREA IMAGER

UNIT CELL SIZE	1.2 x 1.2 MILS
ELECTRODE LENGTH	0.3 MILS
GAPS (NOMINAL)	0.1 MILS
ACTIVE CHANNEL WIDTH	.8 MILS
OXIDE THICKNESS	2300 A
PHOTOSENSITIVE ARRAY	128 VERTICAL ROWS (256 IF INTERLACED) 160 HORZ. COLUMNS
TEMPORARY STORE	128 VERTICAL ROWS 160 HORZ. COLUMNS
TOTAL UNIT CELLS (SENSOR AND STORE)	40,060
TOTAL ACTIVE AREA OF DEVICE 60,000 SQ. MILS (APPROX.)	
FOR TOP ILLUMINATION: TRANSPARENT TO OPAQUE AREA 1 TO 4	
PELLET SIZE	275 x 375 MILS

Table I Specifications of 128 x 160 Image Sensor

The gaps between the aluminum electrodes were 0.08 to 0.1 mils. One of the major problems was to be able to define the gaps over the full 60,000 sq mil area with no shorts between phases. The total length of the 0.1 mil (2.5 μm) gap on the array is approximately 12 feet. The output register can be phased to transfer the charge to either the left or the right. At the left end of the register the signal is detected by a floating diffusion connected to the gate of a MOSFET. At the right end of the register the photogenerated charges are transferred into a two-phase bucket-brigade circuit.[3] The bucket-brigade circuit allows cancellation of the clock voltage swings by sampling the signal at two successive nodes (using the gates of Q_{DA} and Q_{DB}). This is a type of time multiplexing. As the array size becomes larger, the clock frequency increases, thus causing the bucket-brigade processing circuit to become less efficient in removing all evidence of the clock waveform from the output signal.

The successful operation of a large area array requires that the proper phase relations between the three clocks be maintained in each of the three functional areas (see Figs. 3 and 4). In the case of three-phase, single-level metallization technology, the inherent resistances and capacitances associated with the aluminum and N^+ diffusion must not limit operation up to 10 MHz. In the case of two-phase[11] or four-phase sealed channel structures (Al, Poly Si gates), the inherent RC of the polysilicon must also be considered. As an example of this clock phasing problem in the three-phase structures, consider one of the phases of the output register as shown in Fig. 6. The inherent resistance and capacitance of the N^+-diffused tunnel used for driving one set of gates is distributed as an

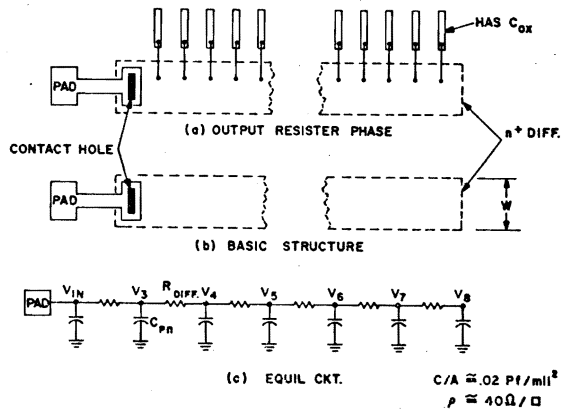

Fig. 6 Equivalent Circuit of Clock Line Requiring Diffused Tunnel for Connection to Each Electrode

RC transmission line. The sheet resistivity of the N^+ is process-dependent and may range from 15 ohms per square to 40 ohms per square. Also the P-N junction capacitance is a function of the profile, the resistivity, the magnitude of the reverse bias, etc. A value of 0.02 pF/mil^2 is a typical number and was used in a computer simulation. The simulation was carried out for a N^+ tunnel 500 mils long. If a 10 MHz clock (one-third duty cycle), V_{IN}, is impressed on one end of the transmission line, the voltages that appear at 100 mils (V_3), 200 mils (V_4), 300 mils (V_5), etc., along the line are shown in Fig. 7a. Note that the signal at 500 mils (V_7) is severely attenuated and therefore useless for efficient charge-transfer. Fig. 7b shows the results of "double-end connecting." In this case the drive voltage, V_{IN}, was connected to a point at 0 mils and a point at 600 mils. Substantial improvement over the "single-end-connected" mode is obvious. However, the waveforms are still nonoptimal from the standpoint of

charge-transfer, and further measures must be taken if the output register is to operate efficiently at 10 MHz. Fortunately, a straightforward topological solution to the problem exists and consists of strapping and multiple drive points.

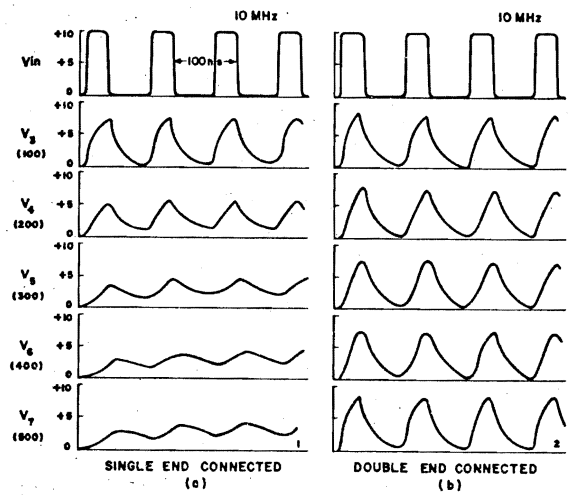

Fig. 7 Waveforms at Various Locations Along Diffused Tunnel

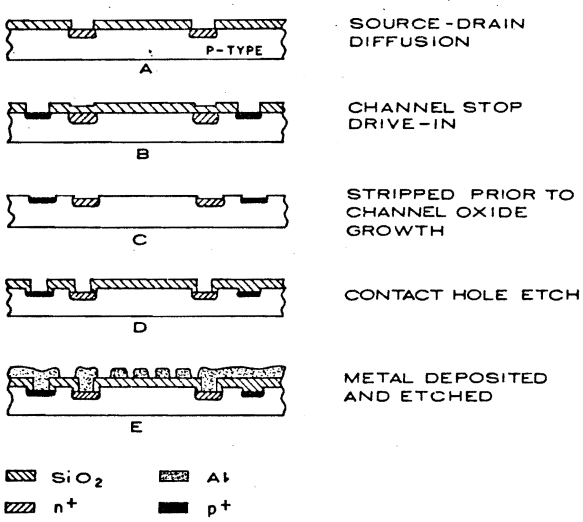

Fig. 8 Fabrication Steps for 128 x 160 Three-Phase Charge-Coupled Image Sensor

Fig. 8 shows the basic steps used in fabricating the 128 x 160 arrays. Basically, four masks are required for construction of a device: source-drain diffusion, channel stop diffusion, contact hole, and metallization. An additional mask may be used for an overcoat. The planar surfaces and the simple process contributes to the relatively high yield of these devices.

OPERATING PERFORMANCE OF 128 X 160

The 128 x 160 sensors have been operated in a mode compatible with the standard 525 line TV system. The all-over picture quality is good. The measured spectral response for the 128 x 160 CCD's is very similar to that of a silicon vidicon. The quantum efficiency is very high in the visible and the near-infrared regions but drops off in the infrared region because the carriers are generated too far from the charge flow channel to be efficiently collected. The peak quantum efficiency is between 25 and 30% and is a factor of 3 to 3.5 times lower than that of a good silicon vidicon. See Table II. This slight loss in sensitivity is due to blockage of light by the aluminum phase fingers. The sensitivity of these CCD's is about 1300 μA/lumen 2854°K. The full well charge-storage capacity in the image sensing area has been measured to be 250,000 electrons for the 1.44 square mil area and drive voltages used. A 20% of full well "fat zero" has been found to be necessary for good performance. This leaves 200,000 electrons per cell for the image signal. The above-stated sensitivity of 1300 μA/lumen 2854°K, 200,000 electrons per cell signal storage, and 16.66 msec (1/60 sec) integration time places a requirement of only 1.5 foot candles (2854°K) illumination onto the CCD for maximum signal. This is equivalent to 0.75 W/m^2 2854°K irradiance.

	128 x 160 Element Array
Full Well Charge	2.7 x 10^{10}/cm^2 (250,000 electrons/cell)
Fat Zero	20% of full well
Dark Current	10 nA/cm^2 (1.9 nA/sensor area)
Max D.C. Signal (1/60 sec integration)	260 nA/cm^2 (50 nA/sensor area)
Sensitivity	1300 μA/lumen 2854°K
Peak Quantum Efficiency	25-30%
Exposure for Full Well with Fat Zero Present	0.15 fc 2854°K 0.075 W/m^2 2854°K
Lag	None

Table II Performance Data on 128 x 160 Image Sensor

SUMMARY

A 128 x 160 element charge-coupled imager has been successfully built and operated. This circuit is a MOS LSI device having the largest area of pinhole free contiguous thin oxide (60,000 sq mil) that has been built to date. This demonstrates the feasibility of building very large arrays that are TV compatible. The problems encountered (mask making, processing, design, device physics, etc.) in making this 275 x 375 mil device are generic to the whole field of large area solid state image sensors and can be directly applied to the design and fabrication of larger two and three-phase arrays.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of all the people involved in the RCA Corporation program[12,13] in solid state image sensors. In the particular phase of the work described above, the contributions of P. A. Levine and R. L. Rodgers have been substantial. The authors would like to acknowledge K. H. Zaininger for his direction of this project.

* The research reported in this paper was sponsored in part by the Naval Electronics Systems Command, Washington, D.C., under Contract #N00039-73-C-0014.

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