APPRAISAL OF CHARGE TRANSFER TECHNOLOGIES FOR PERIPHERAL MEMORY APPLICATIONS

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ABSTRACT. The basic criterion for the selection of a charge transfer technology (CTT) suitable for peripheral memory applications are speed, power, and cost. The speed required for present applications does not exceed a few MHz. Even bucket-brigade and CCD shift registers made by non-self-aligned standard MOS process and using p-channel technology have met this requirement. This leaves only system cost as the major criterion, with chip cost and system overhead cost the subdivisions.

The chip-cost criterion has basically three factors: The first two are yield and wafer processing cost (each depending on the number of photoresist masking steps required to fabricate the silicon chip); the third is the area per bit required for a particular structure on the silicon chip. Since the width of the bit area is independent of the specific CTT circuit, only its length ℓ, in the direction of bit propagation, determines the size and therefore the cost. A comparison is made of ℓ for ten CTT structures as a function of the layout rules. The result indicates particularly low cost for the anodized aluminum three-phase CCD and the self-aligned gate bucket brigade.

In a memory system of given architecture and performance, only the power requirements of the memory chip incorporating some CTT can be considered systems overhead cost specific to its particular structure. Recalling that CV^2f, in general, determines this requirement, the clock amplitude and the capacitance per memory bit control the power requirements of a given CTT structure. The layout pattern - serpentine vs series-parallel-series (SPS) or electrode per bit (E/B) - affects the overall power requirement per chip to an overwhelming degree, but since any of the CTTs can utilize it, it does not affect the differentiation.

In general, it appears that after the selection of a low cost-per-bit CT technoology, the most fruitful direction of improvement is the reduction of system overhead cost by full integration.

APPRAISAL OF CHARGE TRANSFER TECHNOLOGIES

Criteria

The basic criteria for the selection of a charge transfer technology (CTT) suitable for peripheral memory applications can be considered speed, power, and cost.

The speed required for typical applications at present does not exceed several MHz Currently, bucket brigade and CCD shift registers made by essentially standard p-channel MOS processes can operate at 1-2 MHz clock frequencies, and simple multiplexing could increase the system bit rate by a factor of four above this limitation. Since even the simplest CTT technology can meet the requirements, speed does not constitute a valid criterion for selection.

The power dissipation associated with a given charge transfer technology has a two-fold effect: it may limit the maximum size of a chip, and it will affect the size of the power supply and driver circuits. Both are really factors that affect the overall cost of a system incorporating a specific technology.

Therefore, the sole criterion remaining is the complete cost of the whole system. This cost divides very simply into the cost of fabricating a packaged chip containing the CTT memory building block, and the cost of the overhead electronics and structural elements which tie all these chips together into a system functioning as a peripheral memory. However, both of these cost aspects are affected by the specific architecture used in organizing the memory on the chip.

Chip Architecture

One of the basic advantages of the CTT approach is the large number of its bits that can be accommodated on a single chip of silicon. Since both storage of and access to the information is accomplished by shift registers, some way of adapting the basically linear geometry of a shift register to filling the two dimensional space of the surface of a silicon chip is necessary. Three typical approaches have been described.[1]

In Fig. 1, the "serpentine" layout is demonstrated. At the INPUT GATE, a given bit is placed into the first stage of the shift register. Consecutive clockings move it down until it has reached the edge of the silicon chip. The direction of movement is now reversed, and simultaneously the bit is refreshed. Then the bit is moved back up again until it reaches the top, where it is again refreshed, and its direction is reversed. Thus the bit traverses the whole area of the chip in a serpentine manner, until it reaches the output amplifier. The numbers in the boxes representing the shift register stages, indicate the position of the bit in a string of information entering from the input gate. The salient feature of this approach is the fact that adjoining shift registers move bits in opposite directions; each bit enters every stage of the shift register, and it requires a refresh very frequently. Aside from the areas occupied by input, output, and refresh amplifiers, the total area of the chip is essentially proportional to the number of bits, i.e., the total area is $N_B \times \ell \times b$, where N_B is the total number of bits, ℓ is the length of the bit in the direction of transfer, and b is the breadth of the bit at right angles to the transfer direction.

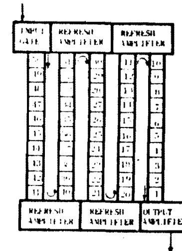

FIG. 1 Serpentine layout.

In Fig. 2 the "Series-Parallel-Series" (SPS) form of a shift register is demonstrated. A given bit enters the INPUT GATE and is shifted in the horizontal series shift register at some clock rate f. When it has reached the fifth stage of the series register, the TRANSFER gates are clocked and all five bits are transferred in parallel into the row of parallel shift registers directed downwards. The TRANSFER GATES are turned off immediately while the information continues to move into the input series shift register at its clock rate. Again after five clockings, the bits in the series register are transferred into the parallel registers, which simultaneously shift their contents by one stage downward. A

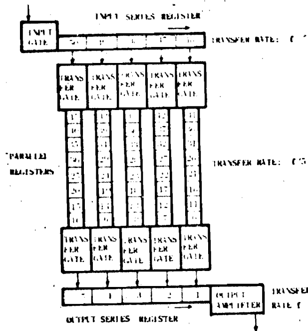

FIG. 2 Series-Parallel-Series layout.

given bit thus proceeds down a parallel register at a clock rate that is one-fifth that of the input rate, until it gets transferred, via another TRANSFER GATE, into the output series register. Now it gets moved towards the OUTPUT AMPLIFIER at a rate that is equal to the output rate. Again the numbers in the boxes representing the shift register stages indicate the position of the bit in the original string of information as it entered the input gate. The salient feature of this layout is the fact that all parallel shift registers move their bits in the same direction at the same rate. In addition, each bit traverses only one fifth the number of stages, it therefore requires much less refreshing. However, there must be two sets of clocks, one for the I/O series registers, and one, operating at one fifth the rate, for the parallel registers. This clearly complicates the overhead circuitry, but there is one important payoff. Since the power dissipation is proportional to the clock frequency ($CV^2f/5$), roughly only one-fifth the power is dissipated while the rate of information transfer occurs at the original rate f at input and output. The total area of the chip is defined by a rectangle whose one side is roughly $N_C \times \ell$ (the number of bits in a parallel branch N_C times the length ℓ of the bit in the direction of transfer) plus some length due to the transfer gates, times the length of the serial shift register which is given by $N_R \times \ell$. Thus, the total bit area is $N_R \times N_C \times \ell^2 = N_B \times \ell^2$, the total number of bits N_B times the square of the lengths of the bits ℓ in the direction of transfer. Since the breadth b of the bit at right angles to the direction of transfer is roughly one-half that of ℓ, a chip laid out using this simple architecture will occupy about twice the total area of the serpentine layout. Clearly, what is needed is a buffer that interleaves two consecutive strings of bits into a set of N_R parallel strings, with the serial registers having length $N_R/2$. The serial output register, operating in a reverse manner, also requires a buffer and a length of $N_R/2$.

The multiplexed electrode per bit approach (ME/B) is shown schematically in Fig. 3. It consists of N_B parallel strings

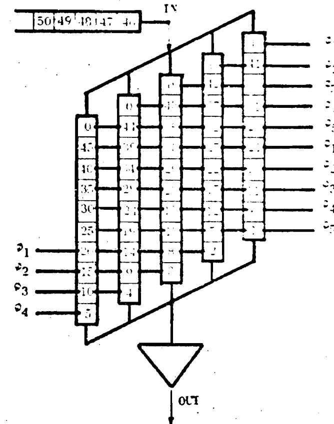

FIG. 3 Multiplexed electrode per bit layout.

that are N_C number of bits in length. First, the rightmost string must be filled with zeros, then, pulsing clock ϕ_1 results in the transfer of the first bit into the rightmost string. When the next bit has reached "IN", the ϕ_2 is pulsed, and so on ad infinitum. The number of clocks required is equal to N_C. But now only one electrode is required per bit, in contrast to the two to four electrodes used in the previous two approaches. Since each electrode is charged or discharged only $1/N_C$ times, power dissipation is even less than in the SPS approach. However, now an N_C-bit-commutator is required to generate the N_C clock pulses from a one or two phase system clock. The total area occupied by bits in tights layout will be a rhombus using a roughly $2N_C \times N_R$ rectangular area or $2N_B \times \frac{\ell}{2} \times b$, roughly about equal to that of the serpen-

tine approach. If, instead, of the simple input shown, a separately clocked multiplexer is used, it appears possible that, even with all that added peripheral circuitry on the chip, the total area may be near the minimal $N_B \times \ell \times b/2$.

Cell Area

The previous discussion indicates that the total chip area is nearly proportional to the area of an individual memory cell. The cell dimensions are defined by its length ℓ in the direction of current transfer, and breadth b at right angles to ℓ. The value of "b" is determined by the minimum width necessary to isolate adjoining parallel or antiparallel shift registers, and the minimum width of each shift register itself. Whether isolation is achieved by field oxide, diffused walls, or air, the minimum widths will be about 0.2 to 0.4 mils. The width of the shift register itself is governed by the same dimension, regardless of the specific CTT used. Thus a common minimum breadth "b" of 0.5 mils can be assumed for all technologies. Therefore, only the value of "ℓ" associated with each CTT will determine the total cell area, and with it, silicon chip area. An unimportant exception to this independence of "b" is the original MOS type three-phase CCD in the serpentine layout, since a diffused line, sufficiently isolated from adjoining CCD's plus an ohmic contact for every cell, has to be provided between every second pair of CCD strings in order to facilitate reversal of electrode phase sequence for every second string. This is not true for either two or four phase devices; and the SPS and ME/B architecture does not require reversal of phase sequence for its parallel strings.

In the following discussion it will be assumed that the width of all CTT structures is independent of its specific realization. It is also assumed that all overhead circuits are made by the same MOS technology. In the discussion of minimum cell length ℓ it will be assumed that the same quality of LSI processing is applicable to all processes. Specifically, the minimum widths w of junctions and metals, and minimum spacing s between junctions or between metals will be assumed to apply to all approaches. The registration tolerance $\pm$ r is the maximum deviation tolerable in either of two directions from an assumed ideal location.

Single level metal CCD. This is the original version of the three phase CCD, using originally a straight MOS technology approach (4 masking steps for diffusion, gate area definition contact, and metal albeit with a requirement for a maximum spacing of 0.1 mil between electrodes. This cell structure has been made with closer spacings by the method of anodizing evaporated aluminum[1] requiring two maskings for metalization. The simple buried channel approach[3] also utilizes this structure, but two masking steps in addition to the simple MOS process are needed for the definition of the ion implanted channel, and an isolation diffusion. Finally, there is a complete set of depletion mode devices possible, utilizing either an MOS, a junction or a Schottky barrier gate. All three require an additional masking step for isolation, which may be achieved by tub or epi-wall diffusion, or by air or dielectric isolation on insulating substrate. The cross section of this approach is shown in Fig. 4.

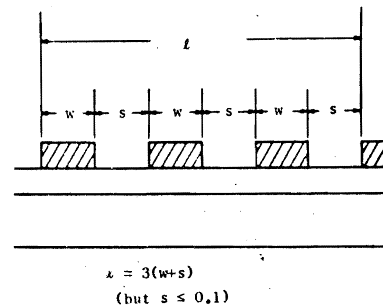

FIG. 4 Three phase CCD.

The structure is sensitive to ionic contaminants settling on the thin gate area between two electrodes. This problem however, can be eliminated with a new way of forming gate electrodes. This approach utilizes "resistive gates"[4]. In effect, the whole area over the gates is covered with polycrystalline silicon of very high resistivity. Those areas selected as electrodes proper are made conductive by diffusion.

Stepped Dielectric CCD. This structure[5] made the use of only two phases possible in contrast to the three or four phases necessary for the single level metal approach. Clearly, all the technological modifications cited for the former structure are applic-

able here also, except that for all an additional masking step is necessary to define the second thickness of the gate dielectric.

The cross section of this structure is given in Fig. 5. It will be observed that the minimum length ℓ is essentially the sum

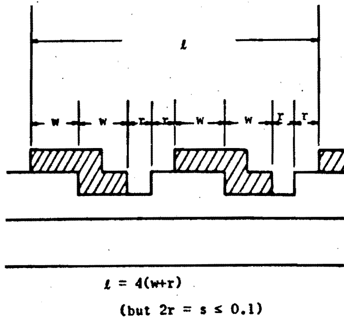

FIG. 5 Stepped dielectric CCD.

of the widths of the dielectric steps and the registration tolerances.

Two level metal (staggered gates) CCD. This structure eliminates the gap of uncontrolled potential between adjoining electrode surfaces.

A cross section of this approach is shown in Fig. 6 This technology utilizes

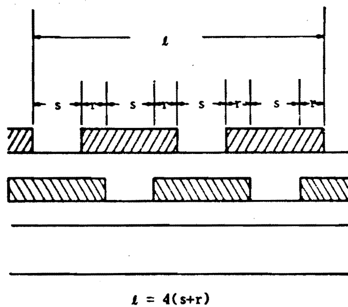

FIG. 6 Two level metal CCD.

two sets of metallic electrodes separated from each other by a second insulating layer. Its cell length ℓ is determined by the electrode to electrode spacing within one set, and the registration tolerance r between the two sets. Clearly, the lower set can be made by a silicon gate approach[6]. However, an added photoresist step is necessary because this silicon layer has to be used as a diffusion mask first. After that process is completed, silicon used to shield the region between adjoining gates from the diffusion has to be removed. The same structure can be realized by the use of molybdenum gates[7] or by anodizing portions of two consecutively evaporated aluminum layers.

Bucket Brigade. This approach to CTT is clearly the oldest[8]. The cross section of this structure is shown in Fig. 7.

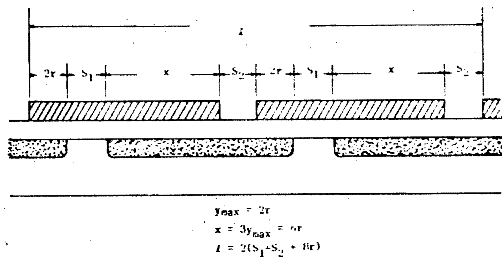

FIG. 7 Bucket brigade.

Looking at the length of this cell it is clear that it is heavily dependent on the registration tolerance r. This arises from the fact that the gate-to-drain capacitance must be at least three times the value of the gate to source capacitance. Since the maximum source capacitance y_{max} is twice the registration tolerance, this heavy dependence is the result. However, the bucket brigade is the only technology that permits the use of any standard MOS process without modification. The cross section shown assumes a simple non-self-aligned approach. There are only two phases necessary.

Implanted barrier CCD. The cross section of this structure is shown in Fig.8. Comparison with the non-self-aligned bucket brigade structure (Fig. 7), reveals that they share identical lengths. This is due to the fact that the implanted barrier devices really shares many features with the bucket brigade. It is therefore just as heavily dependent on registration tolerance. In addition, it requires another masking step to define the ion-implanted region. In order to reduce the need for the three or four phases in the CCD analog of the

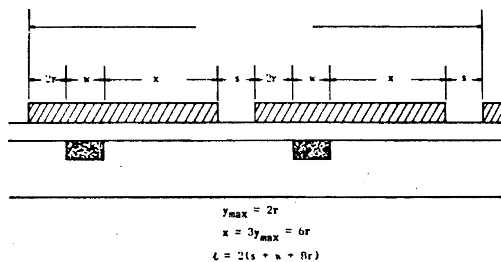

FIG. 8 Ion-implanted CCD.

buried channel, this addition has been proposed. This has increased the number of masking steps required for this technology to seven.

Silicon self-aligned gate bucket brigade. The cross section of this device is shown in Fig. 9. It is electrically identical

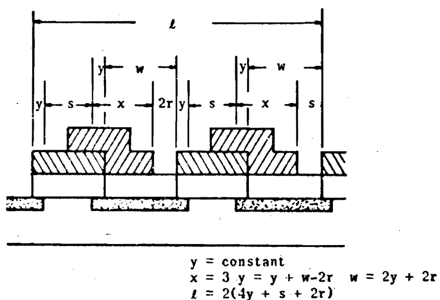

FIG. 9 Self-aligned silicon gate bucket brigade.

to the bucket brigade, except that the diffusion has been formed by a silicon self-aligned process. This way of processing has eliminated the dependence of the cell length on registration tolerance to a large degree. Because now the gate to source capacitance is represented by the lateral diffusion occurring under the silicon gate, only the added metal layer needed to increase the gate to drain capacitance to its proper value is sensitive to registration tolerance. The overall result is a dramatic shortening of the cell compared to the previous two structures. Since a self-aligned process is most desirable for the overhead circuitry anyway, a very fortunate combination of advantages is evident.

C4D technology. This technology[10] represents a merging of the ion implanted and bucket brigade approach, where the structural assymetry needed for two phase operation in the bucket brigade is accomplished by replacing the high gate to drain capacitance by an ion implanted barrier at the source end of the channel. There are clear advantages over both non-self-aligned technologies, in that the need for multiple registration tolerances is eliminated. In Fig. 10, the self-aligned gate version is shown. Surprisingly, its dimensional

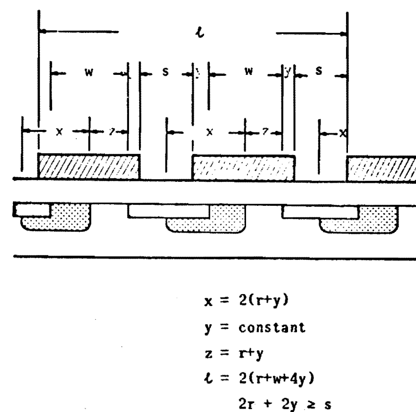

FIG. 10 Conductively connected charge-coupled device.

characteristics are quite similar to those of the self-aligned silicon gate bucket brigade, except for the need of a fifth masking.

Chip Cost

The chip cost criterion has basically three factors: Firstly, wafer processing cost, secondly, yield, each proportional to the number of photoresist masking steps required to fabricate the silicon chip. The third is the area per bit required for a particular structure. Since the width of the bit area is independent of the specific CTT circuit, only the length ℓ shown in Figs. 4 to 10 determines the size and therefore the cost. This length is intimately dependent on the layout rules applied to form the specific geometrics. Table I shows a study of cell length ℓ for ten CTT

structures as a function of layout rules. ℓ was calculated from the equations given in Figs. 4 to 10. Each column is headed by the set of layout rules used to derive its cell lengths.

In order to calculate the cost of a packaged CTT memory chip we will assume that it cost about $50 per major process step and the masking operations associated with it. It is assumed that a yield loss of about 20% for a chip of 100 x 100 mil^2 active area is associated with each such major step plus masking. It is further assumed that 2.5 inch slices (about 300 complete 125 x 125 mil^2 chips) are being used, and that the total cost of packages, packaging and final testing added about $1.00 to the chip cost. Table II summarizes these calculations: Column A gives the number of major process steps plus associated maskings, Column B the consequent cost of slice processing, Column C the final yield, and Column D the cost of a good chip. The last Column (E) has the price of packaging added to the chip. In order to get a measure of the cost of each CTT technology, we will now combine the results of Tables I and II. Specifically, we already know the cost of a chip containing 100 x 100 mil^2 of active area, and we know the length ℓ associated with each CT technology. The area per bit is the minimum average breadth b, which we set at 0.5 mil, times the chosen length ℓ. It appears that the layout rules given in the third column of Table II are tight but not too difficult, and since the payoff is high we will assume that this third column "ℓ" is used in the peripheral memory chip layout. Thus the cell area is defined. We will assume that either serpentine or SPS chip architecture is used. Clearly, all values may be divided by two, if the ideal area reduction implied in the ME/B architecture can in fact be realized in a completely laid out chip. With these considerations, the groundwork is laid for Table III. Since the cost of a memory of stated capacity is ultimately important, the number of packages containing 100 x 100 mil^2 active area chips is calculated, which then permits the calculation of the cost of a memory module of one million bit capacity. Clearly, the number of bits/chip is obtained by dividing the active area by the size of the bit area.

Inspection of Table III indicates that the three phase anodized aluminum technology promises the lowest cost system due to very small cell size, and relatively simple process technology. In addition, there is little penalty in an SPS layout since its length ℓ is very nearly the same as the minimum breadth b. In all other CTT's, chip area, or chip overhead circuitry must be paid for the advantages of the SPS architecture. The second most attractive CTT is the self-aligned silicon gate bucket brigade approach, with other technologies significantly more expensive. Since different manufacturers will be on different portions of the learning curves inherent in each technology, a consideration of total investment vs total return will have a furthere influence on the individual choice of a specific CTT.

Cost of System Overload

In order to obtain a realistic appreciation of the systems overhead required for a CTT memory, a megabit memory system has been designed on paper. The characteristics of this system are as follows:

1024 bits/shift register
16 shift registers/chip
16 K bits/package (12 pin DIP)
64 packages/system

16 bits/word
8K words/block
8 blocks/system
64K words/system

A block diagram of the system is shown in Fig. 11. This configuration provides address decoding and control to allow selection of a single 16-bit word. The chip is organized as an 8K word x 2 bit shift register with one of eight parallel shift registers connected to the I/O pins. The organization for half a chip is shown in Fig. 12. This addressing mode may not be desired or required, but it provides a starting point for a system design which accounts for every component required. The clock voltage assumed is 10 V, the maximum bit rate per I/O line 1 Megabit/second. A rough estimate of the resulting system overhead cost is given in Table IV, with the items separated by their dependence on the power dissipation of the number of packages of the CTT components themselves.

In a memory system of given architecture and performance, only the power requirements of the memory chip incorporating some

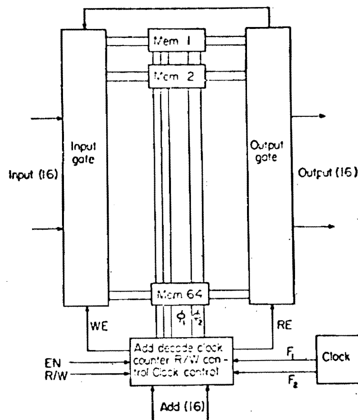

FIG. 11 Block diagram of peripheral memory system.

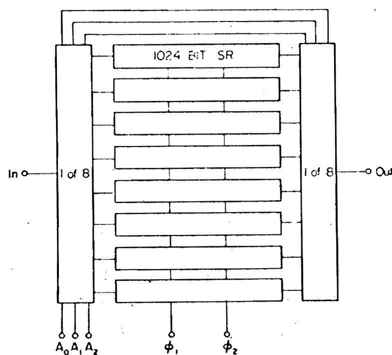

FIG. 12 Block diagram of half a CCD memory chip.

CTT can be considered systems overhead cost specific to its particular structure. Recalling that CV^2f in general determines this requirement, the clock amplitude and the capacitance per memory bit control the power requirements of a given CTT structure. The chip architecture - serpentine vs SPS and ME/B - already affects the overall power requirement per chip, but since any of the CTT's can utilize it, it does not affect the differentiation. In Table V quantities related to power dissipation have been calculated from the 10 V clock amplitude, and from the capacitance per bit, assuming a minimum width "w" of 0.2 mils. The power dissipation in the chip depends on the capacitance per electrode C/E, the number of electrodes per bit E/B, the size S of closed arrays used in SPS and ME/B approaches, and the number N of these closed arrays to make up the 1 Megabit capacity. Clearly, the frequency f also enters into consideration. The pertinent, albeit approximate, formulas for a megabit memory are given in Table V.

TABLE V

Chip Architecture	Power in a Megabit Memory
Serpentine	$(C/E)V^2 f (E/B)^2\ S \times N$
SPS	$(C/E)V^2 (f/\sqrt{S}) (E/B)^2 N$
ME/B	$(C/E)V^2 (f/\sqrt{S}) (N/\sqrt{S})$

It is assumed that all chips are being exercised at full power (there is no stand-by condition), in order to keep every bit refreshed. From the chip organization described below S = 1024.

Inspection of Table VI reveals that only the serpentine chip architecture requires consideration of the contribution of power by a given CTT, the SPS approach drops the power dissipation on all chips to less than 10% of the power used in the independent overhead circuitry and the ME/B approach makes the contribution by any given CTT infinitesimally small. This is, of course, exact only within the context of the paper system described before. Clearly, comparisons can still be made on an absolute basis after the independent system overhead cost has been brought down to the general level of the memory component cost. Inspection of Table VI reveals, in addition, that the number of CTT packages affects the cost of the enclosures, so that bit density also affects system overhead cost.

Conclusion

This study has indicated that there are indeed preferred technologies for use in peripheral memory applications. For a minimum cost per bit of the CTT components proper, clearly the anodized aluminum and the self-aligned silicon gate bucket brigade stand out. For minimum power dissipation, a consideration in space and airborne applications, it would seem that a chip architecture approach is more effective, since orders of magnitude in power reduction can be achieved. In contrast, CTT selection provides a range only of a factor of three.

In general, however, the most important reduction in cost can be achieved by a concentrated attack on the design of the complete system. While at the presently known stage of development, a system cost of 0.1 cents per bit appears achievable, complete integration of the peripheral system should result in a cost closer to 0.02 cent per bit.

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TABLE I

CELL LENGTH ℓ VS LAYOUT PARAMETERS
(All dimensions in mils)

	w = 0.3 r = ±|0.1| s = 0.3	w = 0.2 r = ±|0.1| s = 0.2	w = 0.2 r = ±|0.05| s = 0.2	w = 0.2 r = ±|0.05| s = 0.1
3ϕ CCD-MOS	(1.8)[1]	(1.2)[1]	(1.2)[1]	0.9
3ϕ CCD-Al_2O_3 ($s \sim 0$)	0.9	0.6	0.6	0.6
3ϕ CCD-Buried Channel	1.8	1.2	1.2	0.9
2ϕ Stepped Dielectric CCD	(2.4)[2]	(1.2)[2]	1.0	1.0
Two Level Metal CCD	1.6	1.2	1.0	0.6
Bucket Brigade	2.8	2.4	1.6	0.8
Ion Imp.-MOS	2.8	2.4	1.6	1.0
Ion Imp.-Buried Channel	2.8	2.4	1.6	1.0
SAG-Bucket Brigade[3]	1.4	1.2	1.0	0.8
SAG-C4D	1.4	1.2	1.0	0.8

[1] $s > 0.1$ will not permit coupling of nearest neighbor

[2] $2r = s > 0.1$ will not permit coupling of nearest neighbor

[3] $y = 0.05$ formed by lateral diffusion under silicon gate

TABLE IV

SYSTEM OVERHEAD COST FOR MEGABIT
SYSTEM USING SERPENTINE BUCKET BRIGADE CHIPS

Function	Independent of CT Technology	Dependent on CT Technology	Total Cost
I/O and Address Control	\$100	-	\$100
Enclosure	\$ 50	\$100	\$150
Power Supply	\$100 (12 W)	\$200 (24 W)	\$300
Clocks & Drivers	-	\$100	\$100
	\$250	\$400	\$650

TABLE II

RELATIONSHIP OF THE NUMBER OF MAJOR PROCESS STEPS PLUS ASSOCIATED MASKING, WITH THE COST OF THE FINAL CHIP

A No. of Maskings	B Cost of Slice Processing (Col A x $50)	C Yield (0.8 Raised to Power of Col A)	D Cost Per Good Chip (Col B/300 x Col C)	E Cost of Packaged Chip (D + $1.00)
4	$200	0.41	$1.63	$2.63
5	$250	0.32	$2.61	$3.61
6	$300	0.26	$3.85	$4.85
7	$350	0.21	$5.55	$6.55

TABLE III

COST OF PERIPHERAL MEMORY STORAGE COMPONENTS AS A FUNCTION OF SPECIFIC CT TECHNOLOGIES

A CT Technology	B # Masks	C Cost Per Package (Table II, Col E)	D Area/Bit Mil^2 (Table I-Col 3, x 0.5)	E No. of Bits Per$(100 mil)^2$ (10^4/Col D)	F No. of Pkgs. Per Million	G Cost/ Million Bits (Col.F x Col C)
3 ϕ CCD-MOS	4	2.63	0.6	17 K	60	$158
3 ϕ CCD-Al_2O_3	5	3.61	0.3	33 K	30	$108
3 ϕ CCD-Buried Channel	6	4.85	0.6	17 K	60	$291
2 ϕ Stepped Dielec. CCD	5	3.61	0.5	20 K	50	$180
Two Level Metal CCD	5	3.61	0.5	20 K	50	$180
Bucket Brigade	4	2.63	0.8	13 K	80	$218
Ion Imp-MOS	5	3.61	0.8	13 K	80	$288
Ion Imp-Buried Channel	7	6.55	0.8	13 K	80	$524
SAG-Bucket Brigade	4	2.63	0.5	20 K	50	$131
SAG-C4D	5	3.61	0.5	20 K	50	$180

TABLE VI

POWER DISSIPATION IN A MEGABIT OF CTT CHIPS

		C/E pf	E/B	Power for Megabit in Watts Serpent.	SPS	ME/B
3ϕ CCD-MOS	3ϕ	0.018	3	16.2	0.5	0.002
3ϕ CCD-Al_2O_3(s ~ 0)	3ϕ	0.027	3	24.3	0.8	0.002
3ϕ CCD-Buried Channel	3ϕ	0.018	3	16.2	0.5	0.002
2ϕ Stepped Dielectric CCD	2ϕ	0.024	2	9.6	0.3	0.002
Two Level Metal CCD	Two ℓ	0.024	2	9.6	0.3	0.002
Bucket Brigade	BB	0.058	2	23.2	0.8	0.004
Ion Imp.-MOS	II	0.058	2	23.2	0.8	0.004
Ion Imp.-Buried Channel	IIBC	0.058	2	23.2	0.8	0.004
SAG-Bucket Brigade[3]	SAGBB	0.024	2	4.6	0.3	0.002
SAG-C4D	C4D	0.018	2	7.2	0.2	0.002