# CONCEPTUAL DESIGN OF AN EIGHT MEGABYTE HIGH PERFORMANCE CHARGE-COUPLED STORAGE DEVICE

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**ABSTRACT.** The first part of this paper describes the conceptual design of an 8 megabyte charge-coupled device memory for use as a high-speed electronic, direct-access storage device. The proposed memory has random access to blocks of closed loop shift registers, and utilizes self-contained CCD chips with on-chip decoding. The final design has 256 bits per register, 128 registers per chip, 32 chips per card and 73 storage array cards. A word has 64 data bits plus 8 check bits, and uses a modified Hamming code to provide error correction. The design data rate is 32 megabits per second, access time is 256 $\mu$sec to a 2048 byte block with an additional 512 $\mu$sec average to a word.

The second part of this report describes the fabrication and operation of charge-coupled device memory chips designed to test storage concepts. The models were limited in capacity to that necessary to show feasibility of the approach used in the conceptual design. Two experimental structures were fabricated; a high-density, 256-bit unrestored shift register and a dual 480-bit register with 10 restore amplifiers. The high density memory cells (~ 0.32 $mil^2$ per cell) permit a bit packaging density equivalent to $3 \times 10^6$ bits per square inch. The registers are fabricated with a self-aligned silicon gate (SAG) technology modified to permit use of metal and polysilicon gate electrodes.

## INTRODUCTION

The most common type of storage organization in a computer system is a two-level hierarchy, consisting of fast main storage and slower, less expensive auxiliary storage (magnetic tape, disks or drums). Main memory is usually relatively small and because of high cost is carefully managed to assure efficient use. Auxiliary storage, being less expensive and much lower, is used for bulk storage. Data in auxiliary storage is usually arranged serially or blocked so that the time required to call up the information is important in system performance.

The advent of new storage technologies such as CCD may blur the traditional distinction between main and auxiliary storage because they imply lower cost than main storage and operate at speeds much faster than current auxiliary storage. The potential role of CCD in the auxiliary storage field requires careful assessment of storage systems based upon these devices as they are expected to offer cost-performance advantages over presently used head per track disks.

Briefly, the projected characteristics of a high performance CCD storage are:

1. All electronics block oriented direct (random) access storage organization.
2. Data rate in excess of 30 M bps.
3. Bit densities of $10^6$ bits per square inch.
4. Average block access time faster than one millisecond.
5. Asynchronous operation.
6. Nondestructive readout.
7. Operating power of approximately 4 microwatts per bit.

Assessing these features and weighing them against the added system complexity of another level of storage is risky, but the promise of a fast auxiliary storage device is appealing. The high speed storage

potential seems to offer substantially increased performance over electromechanical technologies used to implement similar computer functions.

The purpose of this paper is to describe the conceptual design of a direct access storage device using charge-coupled device technology incorporating these features and report results of feasibility models constructed to test key points of the circuit concepts.

## CCD STORAGE DESIGN

The conceptual design of a charge-coupled mass storage unit is based upon a projected application similar to that of a head-per-track disk. This type of application commonly employs storage capacities of 5 to 10 megabytes, suggesting a design centered about 8 megabytes.

The system is designed to be used in a block-oriented mode, in which random access is provided to blocks of information, which are then read out or written in serially. Physically, this means that the CCD chip is divided into a number of closed-loop shift registers that store the blocks of information. Random access to these shift registers is provided by on-chip FET decoders. Propagation in the shift registers, which occupy the major portion of the chip, is accomplished with a two-level interconnection pattern activated by an external four-phase electric field.

The further organization of such chips into a memory system depends on a number of design criteria. Since the application contemplated here was industrial, low cost and operational life was emphasized. In addition, the storage system was required to be of small size and low power and to operate in typical industrial environments without elaborate support. Consequently, the chip design should give reasonable chip yields, the package should be reasonably easy to manufacture, and the means of achieving the reliability should not be a prohibitively expensive fraction of the total storage. These topics are considered in the next several sections. The one remaining task of this section is to specify the access time and data rate of the storage system. After examining present and future needs, it was decided to aim for average access times below $0.5 \times 10^{-3}$ sec and data transfer rates of at least $3 \times 10^{6}$ bytes/sec. The next few sections describe the influence of these requirements on the design evolution. Because the key element in the conceptual design is the CCD storage cell, the design description will progress from the storage chip upward to the system.

### CHIP SIZE

It is desirable to have as many bits per chip as possible, consistent with reasonable chip yield. In addition, high speed and low cost are easier to obtain as the density of information storage (bits/square cm) increases. These are the primary considerations in choosing the size of the chip.

Based on fabrication experience and on progress in the industry, it seems reasonable to assume that layout ground rules with 0.15-mil minimum line widths will be practical for the late-seventies. Assuming that a four-phase structure is used to store a bit of information and that information flow is reversed between adjacent parallel channels to close a shift register, topological considerations yield a storage cell area of $15.4\ w^2$, where w is the minimum line spacing. This corresponds to a storage density of $\sim 2.9 \times 10^{6}$ bits per square inch. With such densities, a 32,768 bit chip might be feasible.

### CHIP LAYOUT

The chip organizational layout is uniquely determined by the average access time that the system is to have. Except for some relatively small decoder delays, the average time $T_A$ is given by

$$T_A = 1/2\ B_{SR} T_S$$

where $B_{SR}$ is the number of bits per shift register and $T_S$ is the time period of one shift. The shift frequency is chosen to be 500 kHz to minimize chip power and allow variable speed operation. Hence, $T_S = 2 \times 10^{-6}$ sec. It was stated earlier that $T_A$ should be less than $0.5 \times 10^{-3}$ sec. Therefore, $B_{SR}$ must be less than 500 bits. The nearest binary number is 256 bits so the proposed chip design calls for 128 shift registers of 256-bits. This results in an average time of 256 $\mu$sec plus a small amount of decoder and other delays.

The chip layout is shown schematically in Fig. 1. Each of the 128 closed-loop shift registers has an input-output amplifier, four restore amplifiers and a select decoder. These are organized into four nearly square groups of 32 shift registers, allowing shortened phase lines to drive from the center of the chip. Each shift register is folded four times to match I/O amplifier pitch. A restore amplifier follows each 64-bit register segment.

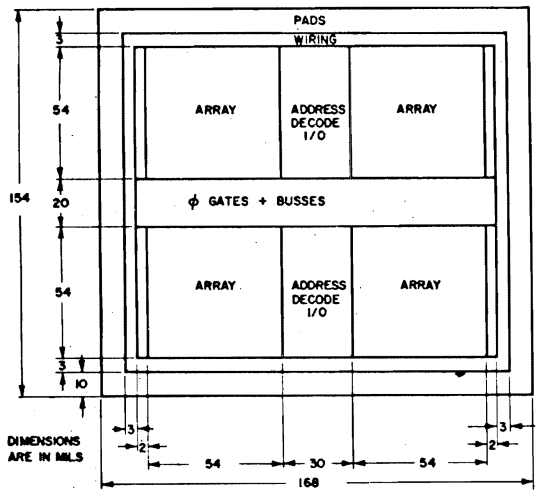


Fig. 1. Proposed memory chip layout

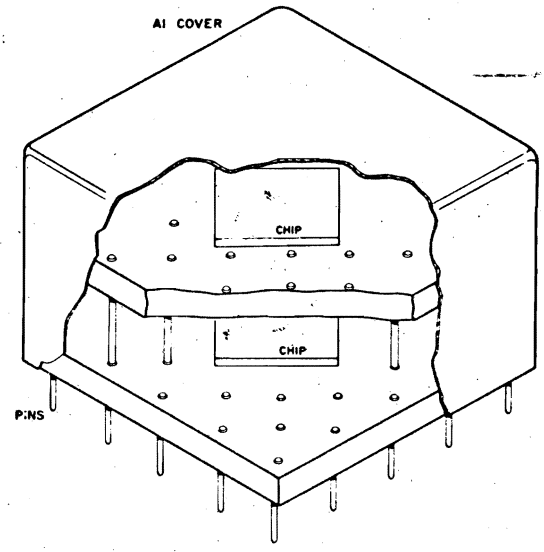


Fig. 2. Basic memory module

Register selection, writing, reading and clearing are all accomplished with 14 control lines. Phase drive, reference voltage and supply voltages require 11 lines, resulting in 25 I/O connections per chip.

## MODULE DESIGN

The proposed module is a design extension of IBM's widely used logic and monolithic memory module. The proposed module, however, is 35 percent larger than the standard module (0.580 in. square) and provides an increase number of I/O pins. Since only one chip is active at a time, the module thermal characteristics permit two chips to be accomodated per module. Consequently, the module has two stacked ceramic substrates, with one chip per substrate (Fig. 2), joined by the IBM controlled collapse solder connection.

To keep the number of interconnections per module down to an acceptable level, the chips are arranged so that address, phase and voltage connections are shared. Input-output and select control lines are separate, resulting in a total of 28 active connections.

## CARD DESIGN

Further assembly of the memory proceeds by placing 16 of the modules described above on a printed circuit card as shown in Fig. 3. This package or card also contains partial address decode, refresh, control logic, and address interface and phase drivers to provide drive for the memory modules.

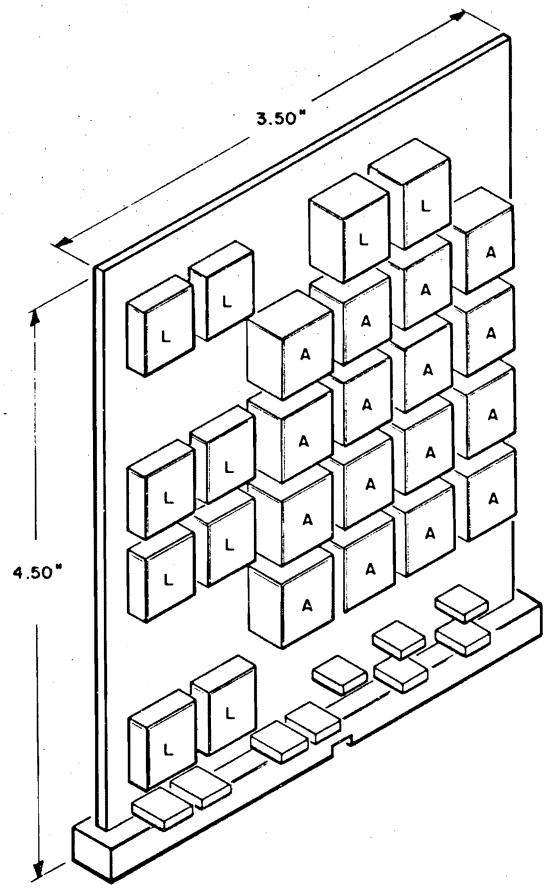


Fig. 3. Storage card assembly

The card or memory sub unit is actually a self-sufficient memory in its own right (except for logic and driving circuits), providing a storage capacity of $10^6$ bits organized in a one million word by one bit configuration.

## SYSTEM

The design approach suggested to satisfy the conceptual requirements was the use of self-contained, charge-coupled storage chips with on-chip decoding. In this approach, the information on the memory chip is stored in a group of closed-loop shift registers, and random access is provided to any one of the registers by an on-chip dynamic FET decoder.

The eight megabyte CCD memory is realized by stacking up the appropriate number of card building blocks. They lend themselves to several different memory organizations, the exact number depending on the organization chosen. In the "bit-per-card" design, a memory word consists of 64 data bits, 8 check bits, plus a position synchronization bit, for a total of 73 cards. The memory is operated in a mode where only one chip per card is selected at a time, providing a substantial savings in card power dissipation. Since the cards are independent sub-memories, serviceability is enhanced. The operating characteristics are summarized in Table I.

Table I. Characteristics of the Design of an 8 Megabyte Memory

| | |
|---|---|
| Capacity | $1.0 \times 10^6$ words of 73 bits each |
| Shift Frequency | 500 kHz |
| Data Rate | $32 \times 10^6$ bits/sec |
| Access Time | 256 $\mu$sec to a block of 256 words |
| | 512 $\mu$sec to a word |
| Power | 237 W |

## ELECTRICAL AND MECHANICAL DESIGN

Many of the reasons for the particular choice of chip, module and card design have been given in the preceding paragraphs. For further discussion, however, it is necessary to know how the memory will be organized, and this requires a knowledge of the electrical circuitry, packaging, and error correction coding needed to implement the possible organizations. Discussion of these topics, comparisons and tradeoffs, however, will be based on the above described chip, a module with two chips and a card with 16 storage modules, logic and interface drivers as described.

## CIRCUIT REQUIREMENTS

The circuits designed to implement the functions defined in the memory system design are tentative and have not been optimized. They are only intended to represent a reasonable estimate of complexity and power consumption. For the sake of discussion, all the numbers that follow pertain to the bit-per-card organization.

The general functional diagram of the system is shown in Fig. 4. Twelve address lines provide addressing to each of the 4096 2048-byte clocks of stored data. An eight-byte (64 data bit) parallel data bus provides a high data transfer rate with an acceptable investment in power and error correction circuitry.

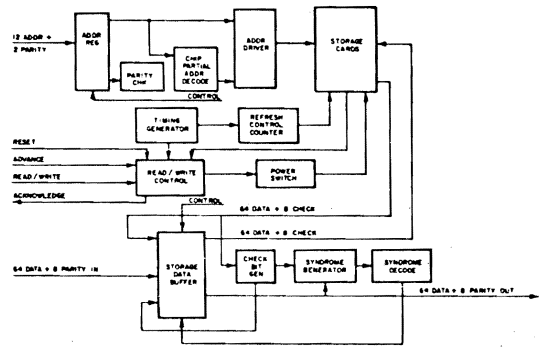


Fig. 4. Functional diagram

The power and equivalent gate count for each function are presented in Table II. The system power is presented in Table III.

Table II. Power Requirements for System Control Functions

| Function | Equivalent Gate Count | Power (W) |
|---|---|---|
| Address Register | 105 | 3.9 |
| Parity Check Circuit | 56 | 0.7 |
| Chip Partial Address | 21 | 0.7 |
| Address Drivers | 57 | 2.6 |
| Timing Generator | 43 | 2.3 |
| Refresh Control Counter | 188 | 4.0 |
| Read/Write Control | 161 | 6.8 |
| Power Switch | 147 | 7.1 |
| Storage Data Buffer | 588 | 9.5 |
| Check Bit Generator | 845 | 18.1 |
| Syndrome* Generator | 76 | 1.5 |
| Syndrome Decode | 180 | 3.3 |
| | 2467 | 60.5 |

*Syndrome-encoded signals generated as a result of a bit error from which the incorrect bit can be located.

Table III. Power Requirements (Watts) for Memory System

| | |
|---|---|
| System Logic | 60.5 |
| Storage Array 73 Cards @ 2.185 | ~ 160.0 |
| Storage Fan–out Drivers | 15.7 |
| | 236.2 |

Packaging design relies upon IBM's standard card and board concepts. The technical objectives of this design concept are (1) minimization of interconnection complexities, (2) adequate environmental protection, (3) sufficient thermal efficiencies to employ forced ambient air cooling, (4) modular flexibility features suitable for expansion, and (5) favorable economic costs.

The overall packaging configuration of the memory system is pictured in Fig. 5, resulting in a volume of 2.9 cubic feet.

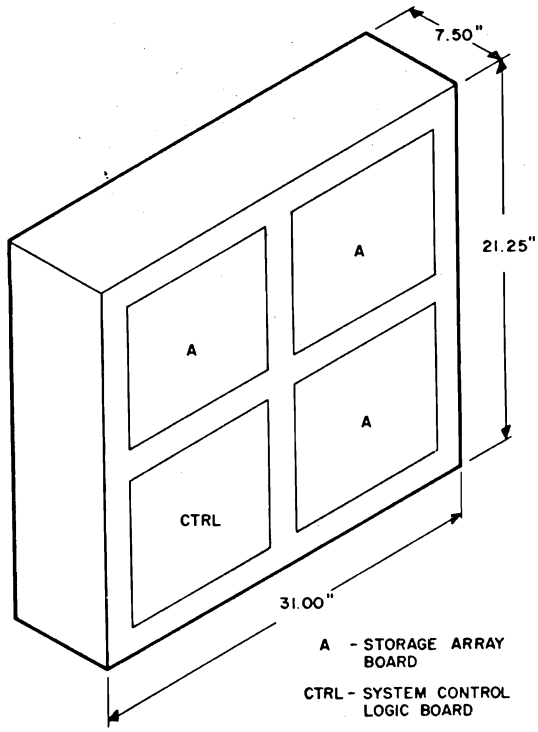


Fig. 5. Eight megabyte storage unit

The unit consists of a gate-structure containing four multilayer circuit boards, covers, interconnecting cables, and pluggable modular card subassemblies containing logic and memory circuits. This unit design does not contain power supplies. It is assumed power and cooling air will be furnished by the host machine.

## POWER CONSIDERATIONS

The CCD cell uses a dynamic charge storage principle and must be periodically regenerated to account for the charge "lost" from the storage node. The regeneration is accomplished by means of restore amplifiers in each shift register. Information is stored as charge in the potential wells, and the ability to differentiate between the amount of charge represents a bit of information. The minimum operating frequency of the shift registers is determined by detectable charge difference, which is a function of time and leakage rate. Careful consideration of these factors results in a lower shift rate of 5 kHz with a restore amplifier located every 64 bits. The restore amplifier senses the charge difference remaining at the end of a register segment and restores the charge levels to those corresponding to an initial one or zero for the next register segment. At this frequency, the chip requires a "standby" power of 19.4 mW. In the standby state, information integrity is maintained but all functions not required to that end are dc-powered using pulse power techniques.

The maximum operating frequency is determined by the allowable power dissipation of the chip for forced air cooling. These considerations result in a shift frequency of 500 kHz with a selected chip (i.e., all circuits fully powered) power of 321 mW.

## ERROR DETECTION AND CORRECTION

A preparatory phase of formulating a reliable storage system requires careful consideration of failure modes for the devices used in the system. Prediction of classes of device failures for the complete memory system is used to impose constraints upon both the chip and system organizations to assure the desired reliability. These considerations are based primarily upon the relative amount of circuitry used to implement the reliability-enhancement features.

To overcome the effects of shift register malfunctions, the memory system is organized so that each bit from a shift register is part of a word located on a different chip.[1] In this memory system organization, the memory device failure modes manifest themselves as either single, or, with lesser probability, double bit errors.

The widely-used Hamming-type SEC/DED* codes, for example, can correct any single-bit error in a memory word, but can only produce an error message in case of a double or higher-order bit error. Such codes, therefore, are most effective in systems organized so that as many failure mechanisms as possible cause only single-bit errors.

## FEASIBILITY MODELS

This section deals with the feasibility models that were built to test and demonstrate the major operating features of the conceptual memory design described above. The models were to be limited in capacity to that necessary to prove feasibility of the approach used in the conceptual design. The essential features of the conceptual chip design and the models are summarized in Table IV.

The feasibility model chips differ from the conceptual chip not only in scale but also in that they do not demonstrate on-chip decoding or closed-loop operation. These have been relatively simple functions to accomplish, as shown by workers in this laboratory and industry as a whole. Mounting of the conceptual chip uses techniques well-known to industry.

Critical features of the conceptual design have been demonstrated by the feasibility models. These include the storage cell density, operating speed, sensing and amplification, and sufficient operating parameter tolerance for actual machine environment.

## DEVICE STRUCTURE

The charge-coupled device uses basically MOS technology. The described structure consists essentially of three layers and is a junctionless device except for small diffused junctions that serve as input and output modes of the shift register. The surface of a semiconductor, such as silicon, is oxidized to form a thin insulating layer. A metal pattern of electrodes is deposited on top of the insulator. In operation, the shift register depends on the transfer of charge from the potential well developed under one electrode to another by application of suitable voltages to these electrodes.

Table IV. Summary of Chip Design Features

| |
|---|
| **Conceptual Design** |
| Self-contained CCD chip with on-chip coding |
| n-type substrate SAG technology |
| Closed loop shift registers |
| Operating speed of 5 to 500 kHz |
| 64-bit shift register segments |
| Shift register turnaround and restore amplifiers |
| Four-phase operation |
| $2.9 \times 10^6$ bits/in.$^2$ |
| Operation in a machine environment |
| **Operating Feasibility Model** |
| High Density Model |
| n-type substrate SAG technology |
| 256-bit single shift segment |
| $2.1 \times 10^6$ bits/in.$^2$ |
| Operating speed of 500 Hz to 5 MHz |
| Four-Phase operation |
| Operating Memory Module |
| n-type substrate technology |
| 480-bit, segment shift registers |
| Shift register turnaround and restore amplifier |
| Four-phase operation |
| Operation in a machine environment |
| Operating speed of 500 kHz |
| Wide operating parameters |
| I/O amplifier |

A cross-sectional view of the overlapped electrode devices fabricated in this test chip is illustrated in Fig. 6. In the structure shown, each spatial bit has associated with it four independent electrodes. The $\phi 1$, $\phi 3$ electrodes, doped polysilicon, define the storage potential well (node) locations. The $\phi 2$, $\phi 4$ aluminum electrodes serve as transfer/isolation gates between storage nodes.

## DEVICE SIZE

The proposed CCD storage cell is designed with an electrode separation of 0.15 mils and 0.05-mil overlap. Channel width is 0.15 mils with a channel separation of 0.28 mils, resulting in an average area

*Single-Error-Correction/Double-Error-Detection

per bit of 0.35 mil$^2$. In the high density devices described here[2], the average area per bit is 0.48 mil$^2$ corresponding to a channel width and separation of 0.2 and 0.4 mils. Calculations of the potential barrier between channels indicate that the channel separation can be reduced to 0.2 mil, while still providing adequate isolation in 1-2 ohm-cm material.

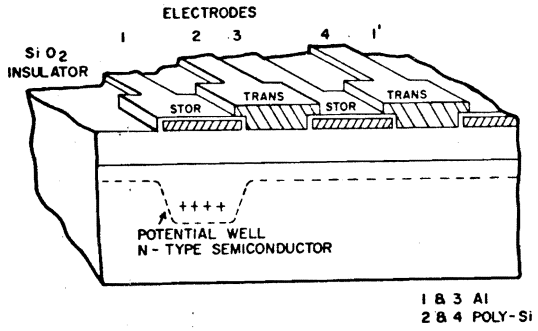


Fig. 6. CCD storage cell

## FREQUENCY RESPONSE

In those pulse powered memory applications where access time minimization and power are important considerations, the frequency response is an important parameter. The frequency response curve for the normalized worst case one/zero difference ($\Delta D$) of a typical 128-bit shift register is presented in Fig. 7.

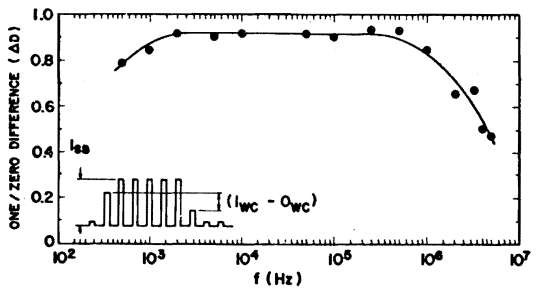


Fig. 7. CCD charge transfer characteristics

Since the one/zero difference is directly related to the charge transfer efficiency, the data imply that the transfer efficiency characterizes device operation over an extremely wide clock frequency range.

The primary mechanism determining the low frequency limit of device operation is the thermal charge generation rate and the tendency of the empty potential wells to fill with thermally generated minority carrier charge. The 500-Hz data point indicates that such room temperature leakage is negligible at information dwell times of at least 1/4 second.

The primary parameter affecting the high frequency limit of device operation is the surface mobility and its determination of the maximum transfer times needed to preserve efficient charge transfer between storage nodes. At a clock frequency of 5 MHz, the nominal transfer time duration is 60 nsec at which a slight drop in signal occurs. The signal difference is sufficiently large so that sensing is not impaired.

There are two primary ways in which temperature can impact CCD operation. First, high frequency response is expected to be lowered with increasing temperature due to a decrease in surface mobility and a consequent decrease in charge transfer efficiency. Secondly, the low frequency response limit is expected to increase with increasing temperature due to the increased rate of thermally generated charge filling an empty potential well. The observed temperature dependence at the three clock frequencies shown in Fig. 8 clearly displays the second effect described below.

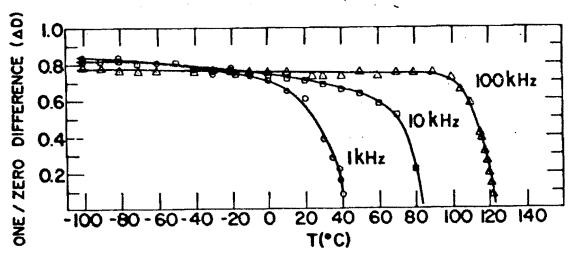


Fig. 8. CCD temperature characteristics

These data were obtained with the substrate biased at a relatively high level (8V), representative of stress conditions. At more moderate substrate bias potentials (~ 2V) the curves shown shift to significantly higher temperatures. This is due to the fact that a reduction in substrate bias reduces depletion region depth, resulting in a reduction in the rate of carriers filling the potential wells.

## TRANSFER EFFICIENCY

In a digital storage application where access time minimization is an important consideration, the use of long shift registers and slow clock rates are generally undesirable. Furthermore, short registers and complex support circuitry may have a significant effect upon the average bit density. The practical implementation of a storage application is dependent upon achieving large values of charge transfer efficiency in each CCD cell to minimize these limitations.

Measurements of test devices are summarized in Table V and imply the use of simple, compact refresh amplifier designs after 32-64 bits without significant impact upon average bit density.

Table V. Typical Transfer Efficiencies for Tested Devices

| | Number of bits $N_B$ | | |
|---|---|---|---|
| | 128* | 128 | 256 |
| Overall transfer efficiency, $\eta_o$ (%) | 98 | 95 | 90 |
| Transfer efficiency per bit $\eta_b$ (%) | — | 99.96 | 99.96 |
| Transfer efficiency per transfer $\eta_t$ (%) | $99.99^+$ | 99.98 | 99.98 |

*Best available device

## OPERATIONAL MEMORY

All the proposed circuit design concepts were exercised in a fully operational memory system.[3] The chosen memory system used dual 2880-bit shift register memory buffers operating at a fixed clock frequency of 500 kHz. The two 2880-bit shift register buffers were fabricated from six dual 480-bit open-loop shift register memory chips, serially connected to form the memory buffers. Each chip contains two 480-bit shift registers and is fabricated as previously described. Data flow proceeds in one direction for 47 1/2 bits and is then amplified and launched in the reverse direction by a sensitive but simple amplifier that introduces an additional 1/2-bit delay. The restore amplifier, designed to operate in so-called fat-zero mode, consists of three FET's as illustrated in Fig. 9. The amplifier inverts the signal and provides a small signal gain of about 80 from channel to channel. In operation, the signal at the launch node is clamped to either VR2 or near ground and the gain realized is only that necessary to compensate for the losses in the channels. Input and output support circuitry for the CCD shift registers interface directly to machine logic levels. Machine logic is diode-transistor with logic zero at ground and logic one at plus six volts. The chip is capable of driving a minimum of one logic load (sink 1.7 mA to ground) and is fully compatible with both machine logic levels and CCD memory chips.

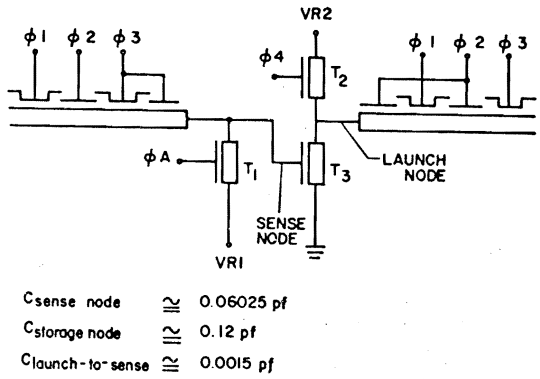


Fig. 9. Restore amplifier

In summary, the work done in fabricating, testing, and designing the feasibility chips has demonstrated that the CCD technology is sufficiently mature and understood so that design and fabrication of an 8 megabyte storage system is possible with an acceptable risk factor.

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2. N. A. Patrin, "Performance of Very High Density CCD," IBM J. Res. Develop., Vol. 17, No. 3, May, 1973.

3. N. G. Vogl and T. V. Harroun, "Operating Memory System Using Charge-Coupled Devices," 1972 IEEE ISSCC Conference Digest, February, 1972.