CCD Digital Memory for Radar Applications

Dr. Ronald A. Belt

A.F. Avionics Lab.

ABSTRACT

The applicability of CCD digital memory to radar signal processing is discussed. Minimum chip specifications are outlined and important chip design tradeoffs are discussed. A 32K bit CCD chip is considered possible using existing CCD and n-channel MOS technology. This chip holds great promise for meeting the needs of real time high resolution radar systems.

INTRODUCTION

Radar systems have become more and more sophisticated as digital techniques have evolved. The use of CCD's for low cost digital memory indicates a continuation of this trend. If CCD memories can be made available at prices below 0.1 cents per bit, radar designers will be able to consider higher resolution systems at costs which remain within the limitations of future Air Force budgets.

Among the high resolution radar systems which can benefit substantially from CCD memory are an assortment of ground-based search radars now in development at various contractors. However, it is with the particular class of high resolution radars known as synthetic aperture radars that CCD memory will have its greatest impact. These airborne systems are desired for reconaissance and weapon delivery.

Present synthetic aperture radar systems are analog and do not operate in a real time mode. Digital versions are real-time and much more flexible, but are limited at present by excessive size and power dissipation, lower reliability, and exhorbitant cost. All these drawbacks are consequences of the processor and display refresh memories, which typically require on the order of 10^7 bits each and which dominate the system performance features. CCD memory holds great promise for not only reducing the cost but also for improving the performance of these complicated digital signal processing systems.

With this brief summary in mind, I shall now go back and consider a few points in greater detail. First of all, I will discuss why CCD memory is the most reasonable choice for radar memory applications.

MEMORY TECHNOLOGY COMPARISON

The major selection criterion is system bit cost. The system bit cost is a function of the cost per bit at chip level and any required systems overhead, such as clocking, multiplexing, address control, I/O control, power supplies, and packaging. Table I lists the expected bit costs at chip level for a number of candidate devices. A 32K bit CCD chip has been assumed along with a 32K bit magnetic bubble device. Both are considered feasible using existing technology.

It is seen that the CCD memory device is expected to have the lowest bit cost of all other semiconductor approaches, including the 4K RAM. This is possible because bit density has been gained at the expense of random access. Serial operation is tolerable in a radar system as long as

the registers are not too long, because the information is processed in a serial fashion anyhow. Of course, a RAM can be operated in a shift register mode by suitable address control, but the effective shifting rate will be limited by the read and write cycle times, and the additional overhead circuitry will further increase the system cost. For this application a 4K RAM is not considered competitive with a 32K CCD memory.

The situation is slightly different with respect to magnetic bubble memory. The lack of commercial marketing experience for magnetic bubble devices makes it difficult to estimate an accurate bit cost; however, the similarity of bubbles to CCD implies that the cost per bit will be roughly similar. Actually, it is possible that bubble costs will be slightly higher because materials costs are higher, fewer companies are competing, and packaging with a bias field is more complex and as yet unsolved.

Even if the cost of bubbles and CCD were exactly the same, the bit rates of magnetic bubble devices are an order of magnitude lower than for CCD's, necessitating a larger amount of multiplexing circuitry at additional overhead cost. Of course, the chief advantage of bubbles, namely their non-volatility, is of no additional help in this application. Consequently, a 32K CCD memory is considered more desirable than a 32K bit magnetic bubble chip. This is especially true if CCD is placed on the market sooner, for then designers will have acquired a familiarity with the product which yields reluctance to change.

If one proceeds further to consider factors such as size, power dissipation, and reliability, the 32K bit CCD chip still proves superior. Interms of size, the single package occupies much less space than the eight equivalent packages for a 4K RAM device. Reliability is also improved due to the fewer chip interconnections which are needed. Finally, system power dissipation is much lower with the CCD memory than with the 4K RAM device, and it is definitely competitive with the magmetic bubble device. This is true because it is possible to organize the CCD chip for very low power operation, and because the power-saving feature of a non-volatile memory is nullified in a radar memory by

Table I. MEMORY DEVICES FOR RADAR SYSTEMS

IN PRODUCTION 1973	IN PRODUCTION 1975	IN PRODUCTION 1977
CORE 600 NS Access 0.3 Cents Per Bit		
PLATED WIRE 100 NS Access 10 Cents Per Bit		
BIPOLAR RAM 1024 Bits 45 NS Access 10 Cents Per Bit		
P-MOS RAM 1024 Bits 250 NS Access 0.4 Cents Per Bit	N-MOS RAM 4096 Bits 350 NS Access 0.1 Cents Per Bit	
PMOS SHIFT REGISTER 1024 Bits 0.1 MS Access 0.5 Cents Per Bit	CCD SHIFT REGISTER 32K Bits 0.05 MS Access 0.05 Cents Per Bit	MAGNETIC BUBBLE SHIFT REGISTER 32K Bits 1 MS Access 0.05 Cents Per Bit

the constant accessing of data. CCD, then, is considered an excellent choice for this radar application.

Table II shows the impact of CCD memory on a typical synthetic aperture radar system. The HIRSADAP azimuth processor in this example contains a four megabit corner-turn memory which is presently constructed using 1K bit PMOS shift registers. (Shift registers were chosen over 1K RAM's because at the time of fabrication their cost was lower.) The CCD memory is seen to be superior in nearly every respect.

CHIP SPECIFICATIONS

The characteristics of a CCD chip which will satisfy a majority of radar memory needs are shown in Table III.

In order of importance, the desired chip features are: reasonable access, low cost, low power, high reliability, small size, and environmental ruggedness. Access time is most important in that it relates to acceptable performance. Processor memories require the shortest access time, which are on the order of 5 us or less to a random bit. However, since the data is ordered sequentially in long blocks, it is sufficient to relax this requirement to 5 us or less to a succeeding bit and 4 ms or less to re-access the same bit. For shift registers this translates into a range of data rates versus register lengths which are in the neighborhood of 1 Mb/sec and 4K bits.

Table II. System characteristics for HIRSADAP processor memory

	PMOS	CCD
CHIP SIZE	1K PMOS SR	32K CCD SR
NO. CHIPS	3,456	108
POWER	1500 watts	50 watts
VOLUME	8 ft^3	1 ft^3
WEIGHT	200 lbs	10 lbs
COST	$75-100K	$8-10K

After access time, low cost is the next most important feature. This implies inexpensive fabrication techniques as well as a design which permits a variety of applications. It also implies that as much interfacing as possible be included on the chip to reduce system overhead cost. Volume production for commercial markets is considered essential for low cost.

Table III. CCD MEMORY CHIP PARAMETERS

BIT DENSITY	32K bits/chip
CLOCKING	2Ø, complementary
PROCESS TECH	n-channel MOS
ACCESS TIME	5 μsec to succeeding bit 4 msec to re-access same bit
SPEED	10K to 10 M bits/sec
POWER DISSIP	32 mW @ 1 MHz
REFRESH INT	2 msec @ 95°C 300 msec @ 20°C
INPUT/OUTPUT	T^2L compatible
ADDRESS CIRC	T^2L compatible
ON-CHIP RECIRC	YES
POWER SUPPLIES	±5V, +12V
TEMP. RANGE	-55°C to +95°C (Operational) -75°C to +150°C (Storage)
MIL. ENVIRON	100%
CHIP SIZE	250 x 250 mils max
PACKAGE SIZE	18 or 24 pin DIP
UNIT COST	0.1¢/bit

The remaining features of low power dissipation, small size, and environmental ruggedness are also important, but will follow naturally from the choice of chip organization and the characteristics of the CCD device itself.

DESIGN TRADEOFFS

Some important design options for CCD memory will now be discussed. The chip can be considered to consist of an assortment of functional components which are combined in a specific organization. Components include the basic CCD shift registers, together with refresh cells, I/O circuits, recirculate logic, addressing circuits, and driver circuits.

A number of CCD structures already exist which are satisfactory for memory construction. Fig 1 illustrates some of the structures currently being examined by various companies. The two-phase structures are most desirable from the standpoint of design flexibility and clocking requirements. Processing

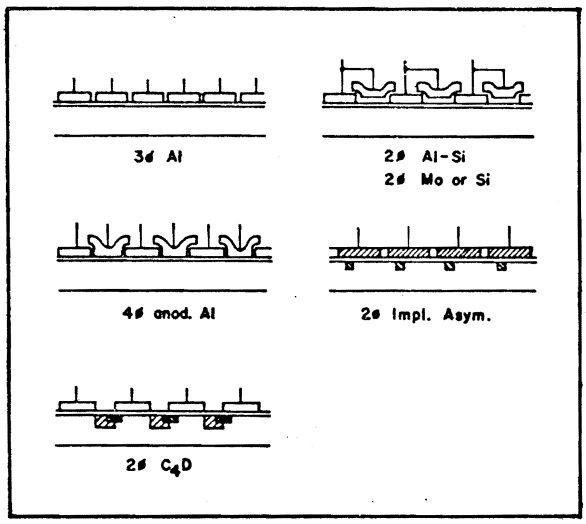

Fig I. CCD structures which have been discussed in the literature by leading manufacturers. At least seven other variations of these basic CCD structures have been examined.

simplicity is extremely important, as it affects the cost directly. Charge transfer efficiency although a factor, need not be as high as for imaging devices. Finally, buried channel construction is not absolutely required for better memory performance, although it may be beneficial for secondary reasons such as perhaps eliminating the necessity for fat zero operation.

The operational characteristics are quite similar for all these shift register structures, and are summarized in Table IV.

Table IV. Typical parameters for CCD Shift Registers.

AREA PER BIT	1 mil^2
POWER PER BIT	10 uW @ 1 MHz
SPEED	10 KHz to 10 MHz
DARK CURRENT	10 nA/cm^2
CTE PER ELECTRODE	99.99% @ 1 MHz

Refresh cells are also an important component in a CCD memory device, especially in serpentine designs. A practical refresh cell must satisfy size constraints as well as electrical and processing constraints, such as fat zero operation and insensitivity to threshold voltage variations. It is generally conceded that the simple floating diffusion refresh cell[1] does not qualify as a production device. General Electric's bifurcated input structure[2] appears interesting and could be explored further. Another possibility is to relax the dimensional constraint of two register widths by interleaving pairs of shift registers and using specialized refresh and corner-turn circuits at alternate

Table V. CCD MEMORY ORGANIZATIONS

	ADVANTAGES	DISADVANTAGES
SERPENTINE [3]	WIDE SPEED RANGE HIGH TEMP OPERATION	HIGH POWER DISSIPATION REFRESH WASTES CHIP AREA
SPS [4]	LOWEST POWER DISSIPATION HIGHEST PACKING DENSITY	NARROW SPEED RANGE LARGE ARRAYS GIVE: POOR ACCESS TIMES POOR TEMP BEHAVIOR
LINE ADDRESSABLE [5,6]	LOW POWER DISSIPATION SHORT ACCESS TIME	POOR PACKING DENSITY LARGE ARRAYS REDUCE TEMPERATURE RANGE
SCT RAM[7]	FASTEST ACCESS TIME HIGH CTE NOT REQUIRED	WORST TEMPERATURE BEHAVIOR HIGH POWER DISSIPATION WASTES CHIP AREA

nodes. In the meantime, a satisfactory solution solution appears to have been found using dynamic MOS amplifiers.

With regard to other on-chip components such as TTL compatible I/O, logic, and drivers, dynamic n-channel MOS circuits as used in other MOS memory products appear to be more than adequate. It is safe to say that all the necessary components now exist for a practical CCD memory chip. The major task which still remains in the definition and implementation of an efficient chip organization.

Chip organization may prove to be the key to a practical CCD memory. Possible memory organizations are listed in Table V, together with their relative advantages and disadvantages. A full size memory chip may utilize any one of these organizations or a combination of them to achieve the proper operation.

In selecting the proper organization, careful consideration must be given to the time between refresh. This time is determined by the clocking rate and the number of bits between refresh. It must always remain less than the signal storage time, which is a function of the threshold levels, the dark current level, and the temperature. The storage time at 20°C is in the neighborhood of 500 milliseconds and it decreases by roughly a factor of two for every 10°C in temperature. The result is that for a given number of bits between refresh, the minimum CCD clocking rate must increase as the device temperature increases. An optimum memory organization will utilize the maximum number of bits between refresh consistent with the anticipated temperature and data rate limits. For a military system this implies 4096 bits or less between refresh. It is not necessary that the time between refresh be exactly equal to the memory access time.

Proper selection of memory organization can lead to a further reduction of power dissipation. Most of the power dissipation occurs in the drivers from clocking the capacitive load. This power depends linearly on the clocking frequency; so a lower clocking rate means a lower power dissipation. An analysis of the SPS structure shows that the power dissipation for a MXN array is given by

$$P_{SPS} = \left(\frac{2}{N} + \frac{1}{M}\right) MNCV^2f.$$

For a serpentine array of the same number of bits the power is equal to

$$P_{SPS} = MNCV^2f.$$

This results in a power reduction by a factor of

$$\left(\frac{2}{N} + \frac{1}{M}\right),$$

which for a 4096 bit array is roughly 5% of the power for the serpentine device. Both devices would have the same input and output data rates.

Another aspect of power dissipation concerns itself with driver capabilities. When clocking the capacitive load of a large CCD memory chip at high frequencies, a large instantaneous current must flow thru the driver circuits. This can be minimized somewhat by using lower voltage n-channel devices and CCD structures which are less sensitive to the rise and fall times of the clock pulses. But the current-handling capabilities of most driver circuits will be severely taxed unless specifically accounted for in the chip design. This can be done without much difficulty.

Having pointed out a number of major design considerations, it is legitimate to ask at this point whether it is possible to find one organization which will satisfy all system requirements. The answer is definitely yes; in fact, more than one acceptable chip organization has been proposed.

CONCLUSION

There are many additional topics to consider in obtaining a CCD memory for radar, but time does not permit a full treatment of all essential features. However, one important topic deserves to be mentioned in connection with military applications. This is the problem of radiation hardness. It is well known that CCD's are exceptionally sensitive detectors of visible radiation. The same sensitivity applies to gamma radiation, where the detection mechanism is identical. As in the optical case, where the detected signal is related to the incident light flux, the gamma radiation problem is primarily a dose rate effect as opposed to a total dose effect. This distinction is consistent with the fact that dose rate effects are generally transient,

whereas total dose effects are more permanent. On this basis, one might expect that CCD's would have a very poor gamma dot hardness, but a total dose hardness which is equal to or better than that of ordinary MOS. Recent radiation testing results appear to confirm that CCD's can be quite hard to total gamma dose. This means that CCD's can be used in real-time applications even where radiation hardness is a requirement, as long as one can tolerate a temporary loss of data. Such is the case in radar applications.

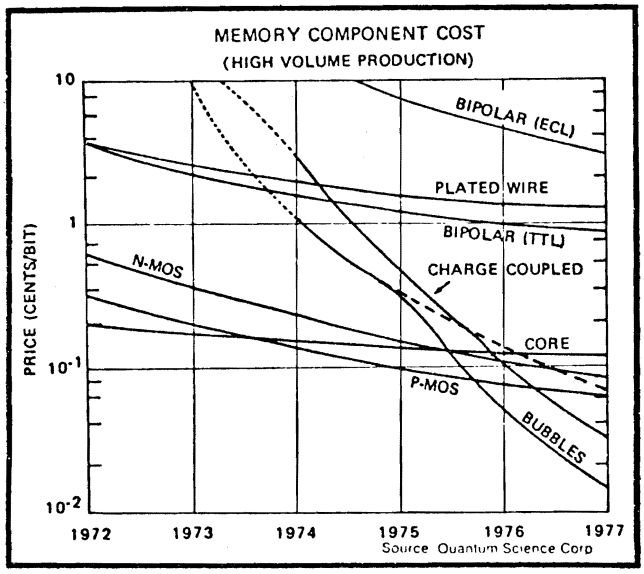

Fig 2. Projected cost per bit for the leading memory technologies. The figure is identical to that published by Quantum Science Corporation, except that the initial trend for magnetic bubbles has been extended to show the result of bubble material non-availability in production quantities. The present author believes that N-MOS will overtake P-MOS sometime after 1976.

In bringing this discussion to a close, I wish to re-iterate the low cost potential of CCD memory devices. Fig 2 shows the projected costs for CCD and other memory devices.[8] These projections are in agreement with my own assessment of each technology's capabilities. They are also in agreement with the future demand for peripheral memories and cache memories, both of which are high volume markets. If these projections are verified, then CCD memory will have much to offer for high resolution radar applications. It may well develop that CCD memories will make practical such high performance radars as UPD-X.

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