RECENT IMPROVEMENTS IN CHARGE COUPLED MEMORY DEVICES*

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ABSTRACT

The Charge Coupled Memory (CCM) combines the CCD with an MNOS permanent storage capability. Changes have been made to the basic device to improve transfer efficiency and storage characteristics. A rectangular drive voltage affords an output level of 0.5 v without amplification and an "0" to "1" ratio better than 2:1. Transfer efficiency now exceeds 0.985 as a result of structural improvements.

The charge coupled memory (CCM)combines the technologies associated with MNOS storage devices and charge coupled devices (CCD) into a nonvolatile, high density, block-addressable, read-write memory, using standard MOS silicon fabrication techniques.

The operation of a charge-coupled-memories device has been demonstrated by the authors.[1]

The structure of the CCM is basically the same as that of a CCD, except the gate oxide is replaced with a thin oxide-thick nitride sandwich, as in MNOS devices. Charge storage in the CCM is a function of oxide field strength and is dependent on applied gate voltage and the quantity of charge transferred into the local area.

Initial devices were found to operate satisfactorily, but with a number of deficiencies, including low "0" to "1" output ratio, short data storage times, transient interference, and low output levels. Changes have been made which substantially improve device performance. These changes include structural modifications, a revised drive voltage waveform, and improvements in processing.

STRUCTURE OF THE CHARGE COUPLED MEMORY

The basic device structure, shown in Figure 1, closely resembles the standard CCD. The oxide layer, however, is very thin (~25Å), and an additional layer of silicon nitride is added before the first layer gates are put on. Small p+ diffusions form p-n junctions at each end of the register. A layer of silox is added between alternate electrodes of the four-phase configuration.

In an actual device, N+ diffusion lines stop band-inversion from occurring at unwanted locations under the electrodes, and also define the edges of the CCD shift registers. Drive potentials are applied to the electrodes in the standard four-phase arrangement sweeping the charge along the potential well schedule in typical "push-broom" fashion. The depletion region edge defines the depth of the potential well and determines the position to which surface charge will tend to flow.

OPERATION OF THE CCM

The four operating modes of the CCM are as follows:

1. "Write" mode-putting charges or data into the device

2. "Read" mode-reading out the stored data

3. "Erase" mode-to erase all the stored data

4. CCD mode-operated as a CCD

In the "write" mode, the data (1's and 0's), represented by charges in the potential wells, are shifted by CCD operation to the desired positions. Then a large voltage (~30v) is applied to the storage gates. If there is sufficient charge under the gate, the field in the oxide will be high, electrons will be able to tunnel through the oxide, and some will fall into the deep traps in the oxide-nitride interface. At those sites where insufficient charge resides, a deep depletion layer is built up in the bulk, and electrons cannot tunnel through the oxide.

The "read" mode is accomplished in two stages. First, the potential wells under the storage gates are flooded with charge. Then this charge is shifted to the output. If a particular site has charge stored in the oxide-nitride layer, the field in oxide will be lower, and the associated potential well can hold fewer charges. Hence, a lower output indicates the corresponding site has "1" stored.

In the "erase" mode, a positive voltage (~30v) is applied to all storage gates, so that the charge in the traps will tunnel back to the bulk.

PERFORMANCE OF THE CCM

Initially, CCM's were fabricated using oxide and nitride layers of uniform thickness. The thickness of the oxide was approximately 25Å while the nitride was 750Å thick. 2000Å of silox was used to isolate the upper and lower gates. Four-phase sine wave voltage patterns were used to drive the CCM. Operation of the device demonstrated satisfactory performance in all functioning modes with a readout voltage "1" to "0" ratio of 0.92. Transfer efficiency of this structure when propagating charge in a CCD operating mode was measured at .97. Following this demonstration a series of modifications was undertaken to improve performance characteristics.

REVISED DRIVING CIRCUITRY

The first of these changes involved substituting a square wave drive for the sine wave propagation signals (Figure 2). The primary aim of this change was to provide for more charge to be available during the write cycle. For an equivalent peak driving voltage excursion, the square wave propagates more charge by virtue of the flat bottom potential well. Also because the wells are usually not full, the average field in the nitride is lower. Therefore, less charge will tunnel through the thin oxide during transfer. More charge, however, will be caused to tunnel through the oxide when the device is operated in the storage mode. The net result is an increased output signal, and a consequent larger ratio of 0's to 1's.

Tests conducted with the square wave drive substantiates these predictions. The trace of Figure 3 indicates this ratio exceeds 2:1, making the discrimination of written to unwritten signal easier and more reliably accomplished.

REVISED STRUCTURE

In order to provide for higher transfer efficiency, a revised structure was designed and fabricated (Figure 4). The basis for this approach was to confine the thin oxide to the storage sites only. In this manner charge can be transferred under a thick, uniform oxide through most of its route. Transfer efficiency was measured in this device at .985. Figure 5 illustrates the new device.

CURRENT PROBLEM AREAS

A. Degradation of Readout Signal

At the current state of development, limitations are placed on the number of times a stored charge pattern may be read out without significantly affecting signal quality. In one test, a CCM was subjected to 4×10^3 readout cycles without refresh.

Here it is noted certain of the signals have deteriorated to the point where it became more difficult to discriminate between 1's and 0's in the output signal. The loss of signal amplitude was attributed to small amounts of (statistical) tunneling that take place through the thin oxide layer in response to potentials applied to the propagation gates. Solution to this problem is hampered by several factors, including difficulties in reducing spurious tunneling field strength imposed by the

nitride layer. In order to transfer charge effectively, large voltages must be applied to the electrodes. This, in turn, creates the high fields at the storage sites.

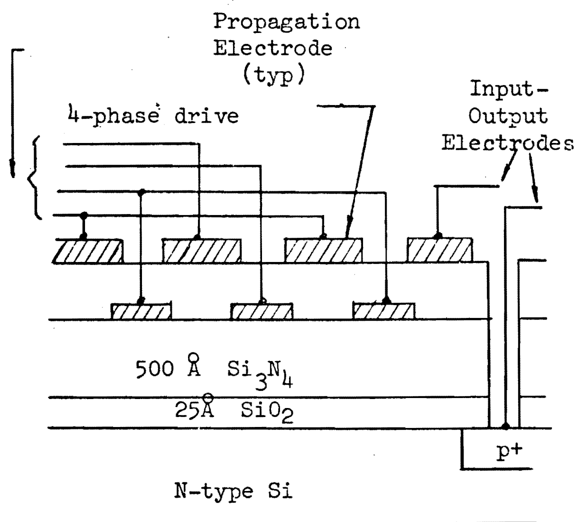
B. Transfer Efficiency

Further improvements in transfer efficiency are hampered by difficulties in annealing the Si-SiO_2 interface in the presence of the nitride layer. One approach is to limit the number of cells to be fabricated in series. This solution, however, has undesireable system applications implications.

We are currently exploring a number of alternate configurations, structures, and processes designed to resolve these problem areas.

REFERENCES

1. Y. T. Chan, B. T. French, and R. A. Gudmundsen, "Charge-coupled-memory device," Appl. Phys. Lett., 22, (1973).



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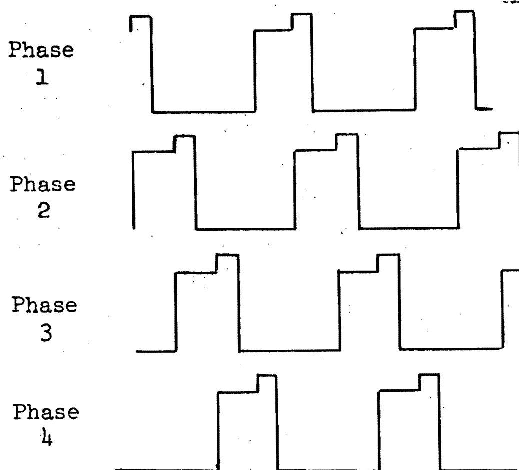

Figure 2. Rectangular Drive

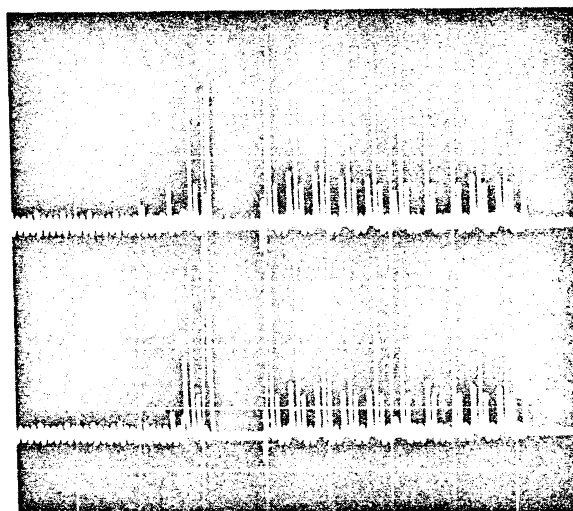

Figure 3. Improved 1/0 Ratio Using Square Wave propagation. Upper Trace: Charge propagated, no charge stored. Lower Trace: Readout cycle, charge stored at 7th cell. Vertical-.2v/cm. Horizontal-.2ms/cm

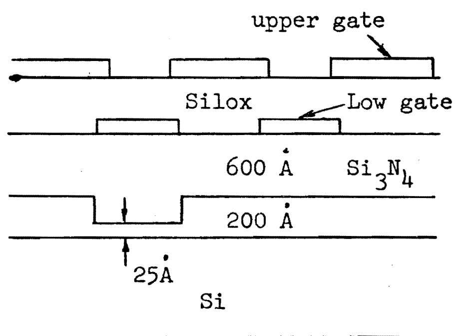

Figure 4. CCM Structure.

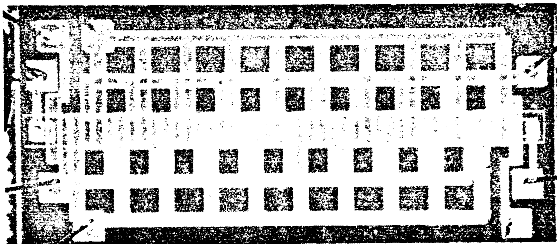

Figure 5. Photograph of new device.