256 BIT REPEATER CHAINED 2-PHASE CCD DIGITAL SHIFT REGISTER

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ABSTRACT CCDs show promise for high density serial storage. Several structures and devices will be discussed. A 2-phase 256 bit digital shift register has been successfully fabricated and tested. Repeater stages chain the data string at 16 bit intervals.

INTRODUCTION

CCDs show promise for high density memory storage. Several devices and structures have been fabricated and tested to measure CCD potential as a means of digital serial storage.

A 256 bit multiple oxide 2-phase charge coupled device[1,2] shift register has been constructed and successfully transmitted arbitrary bit patterns. The multiple oxide structure (Figure 1) provides charge directionality with the application of 2-phase voltages[3,4]. Among the aspects that are new is that we have combined 2-phase cells with repeater stages spaced at 16 bit intervals to form a long 256 bit shift register capable of extension into shift registers of arbitrary length.

MULTIPLE OXIDE FABRICATION

The multiple oxide structures were fabricated by first growing a 1000 Å thermal oxide in dry O_2. The second oxides were deposited in thicknesses from 1000 to 3000 Å from a tetraethyl-orthosilicate (TEOS) organic source or an inorganic source $SiH_4 + O_2$. Additionally, some oxides were doped with P_2O_5 to observe gettering effects on contaminants. Further, the final structures were given various annealing treatments. Typically, Q_{ss} for the first oxide is on the order of 2 to 3 x 10^{11} states/cm^2 for (111) oriented material. It has been found that the Q_{ss} at the oxide-oxide interface can be an order of magnitude higher or lower than this depending on type of deposited oxide and annealing technique. We observe inorganic sources giving lower values of Q'_{ss} than organic sources[5]. Further, we note an anomalous introduction of positive space charge caused by phosphorous resulting in a negative shift in flat band voltage.

The devices were fabricated on 111 silicon 5 ohm-cm, N-type material. Thick oxide is used for shift register isolation. The final step is the deposition of aluminum and etch to complete the structure. The photomicrographs in Figures 2 and 3 show the detail of the structure. The polysilicon length is approximately .8 mil; the aluminum electrode .4 mil. Polysilicon gates over 1000 Å gate oxides had nominal-2 volt thresholds. Depending on oxide sandwich thickness and oxide-oxide fixed charge surface states, the aluminum gates had thresholds ranging from -6 to -16 volts. Mobility at -3 volts gate voltage is about 200 cm^2/V-S for these p-channel devices.

CCD SHIFT REGISTER DESIGN AND OPERATION

The design of a digital shift register requires a knowledge of dynamic response and quasi static surface potential configuration. For a fixed geometry, the transfer efficiency establishes the number of bits before a repeater stage is necessary. Further, it is well known that operating in the fat zero mode is beneficial for

surface devices.

OPERATING MODES

The basic 2-phase CCD shift registers can be operated in several modes. A 32 bit and a 256 bit repeater chained shift register are shown in Figures 4 and 5 respectively. These devices have been operated in static clock mode, dynamic clock mode, and uniphase mode as shown in Figure 6. The static clock mode is made up of simple non-overlapping clock phases driven by square waves. In this mode, the signal charge can occupy not more than about 1/3 of a full bucket; this follows from the required constraints on surface potentials which maintain directionality in the device. Basically, a full bucket can be transported using a dynamic or push clock mode(6). The finite clock fall times eliminate the need for surface potential margins required in the non-overlapping clock mode.

Some of the devices tested had a relatively thick second oxide of 4000 Å. Other devices with thinner second oxides on the range 1000 Å have also been fabricated and operated. Thinner oxides allow alternative operating modes. The relatively thick second oxide increases device yield by reducing the probability of phase to phase shorts in the overlap areas. A relatively thick oxide also reduces the clock to clock capacitance; it also increases the aluminum gate threshold. Because the surface potential under the aluminum gate is reduced compared to the poly region for the same gate voltage, one loses dynamic range when operating in the non-overlapping clock mode. The push clock mode has several advantages: The dynamic range of the device is increased compared to the non-overlapped clock mode and by proper choice of fall times, a maximum difference in surface potential is maintained between buckets. Repeater stages are placed at sufficient intervals to maintain a recoverable signal.

Figure 7 shows a data pattern transmitted through a 256 bit device chained by a repeater stage every 16 bits (Figure 5). The data rate was 100 KHz. Phase clocks are -5 to -15 volts operating in the dynamic clock or push clock mode. The output signal is derived from a resistor in series with a MOSFET gated by a final repeater stage. The bit size is 3.1 mil^2. The average bit size including repeaters is 4 mil^2.

REPEATER STAGE

The basic repeater stage is shown in Figures 8 and 9. This device is capable of being operated in several modes. The diode ϕRS essentially sets the reference voltage. In a particular mode, this can be one of the phase clocks. The upper portion of Figure 9 shows the physical look of the stage. The lower portion shows the equivalent electrical circuit. Basically, the stage operates by setting the control node to a fixed reference state which sets the voltage of the repeat gate to some standard level. Next, the signal charge arrives. The control node equilibrates to a new voltage determined by the amount of signal charge arriving. The line V_S is a charge source for the repeater. Depending on repeater operating mode V_S can be a DC voltage or a clocked source. In addition, the repeat clock V_C can act as a charge barrier when the source is clocked negative. The point B (Figures 8 and 9) can act as a fat zero storage site. Point B is returned to a known reference state once each cycle and is thus capable of injecting a fat zero. A particular advantage of this type of repeater is that the minimum row to row spacing can be maintained since no extra lines have to run between adjacent serpentine data flow rows. If the presence of charge indicates a one and the absence of charge a zero, then this repeater stage inverts the message in the repeated bit. The arrival of charge at the node causes the surface potential to approach zero volts and turns off the signal control gate. The absence of charge causes the control gate to stay turned on. The repeat V_C clock is activated only after the equilibrium voltage is achieved. It is apparent that the final voltage is a strong function of the applied control voltages, overlap capacitances, and amount of signal charge.

2-DIMENSIONAL EFFECTS: COMPUTER SIMULATION USING FINITE ELEMENTS

The initial theoretical characterizations of charge coupled devices solved the electrostatic problem for infinitely wide plates. Using such one dimensional models, it is possible to derive analytic

expressions relating gate voltage, signal charge, and surface potential. It was then pointed out that the dynamics of charge transport in long electrode devices could be limited by a slow diffusion term encountered in nearly empty charge buckets; transfer efficiency could be greatly improved by operating the device in the "fat zero" or trickle charge mode. Another method of improving efficiency is to use very short length electrodes which result in fringing fields which aid charge transfer(7). The fringing fields are inherently a result of the two dimensional effects which simple analysis cannot handle accurately. In the practical world of computer memory, the small bit size possible with CCD is of great interest; thus, there is a need to accurately model two and three dimensional effects which naturally occur in high density devices.

Most solutions of the two dimensional potential problem have used the method of finite differences(8). In charge coupled devices, mixed boundary conditions of voltage and charge naturally arise. Further, CCDs can have very complicated geometries such as multiple oxides, finite conductor thicknesses, and overlapping electrodes. In addition, the effects of distributed Q_{ss} and non-constant diffusion profiles can be critical. Using finite differences in the presence of complex boundary conditions such as those mentioned above is difficult--although possible. Amelio has pointed out that more elegant techniques might be advantageous(8). We have solved the electrostatic CCD problem using finite elements for arbitrary charge, voltage, and geometries(9). We find that by using finite elements it is particularly simple to handle complex boundary conditions. This follows from the natural formulation of the problem in terms of charge and voltage when using finite elements. Finite elements also result in computational economies due to a more accurate representation for equal number of nodal points and the ease of using variable element size. Figure 10 illustrates the result of finite element calculation for geometries near those discussed in this paper. For convenience, the flat band voltages are assumed to be zero. For very high density devices, computer simulations using such techniques as finite elements will be invaluable.

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(9) Wilson, E. A. and Tchon, W. E., "Calculation of Transfer Potentials in Charge Coupled Devices with Arbitrary Voltage and Charge Boundary Conditions Using the Finite Element Method," The Record, 25th Southwestern IEEE Conference, pp. 550-555, April 1973.

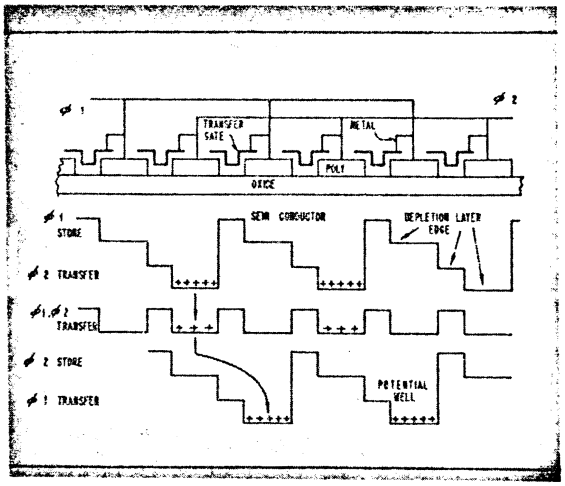

FIGURE 1
2-PHASE CCD SHIFT REGISTER STRUCTURE

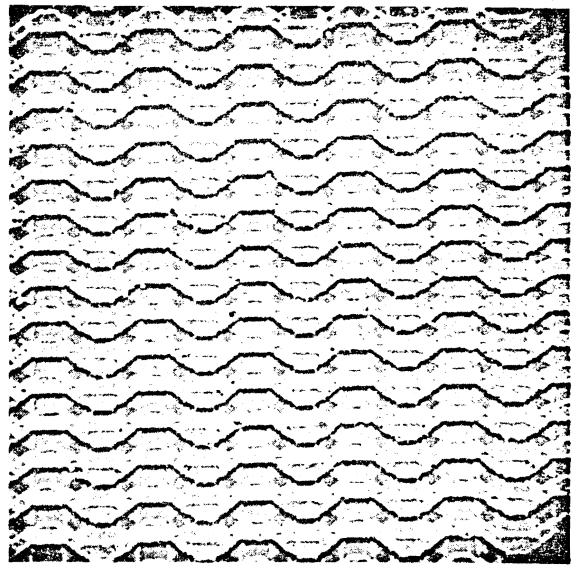

FIGURE 3
ARRAY DETAIL OF 256-BIT CCD (SEM)

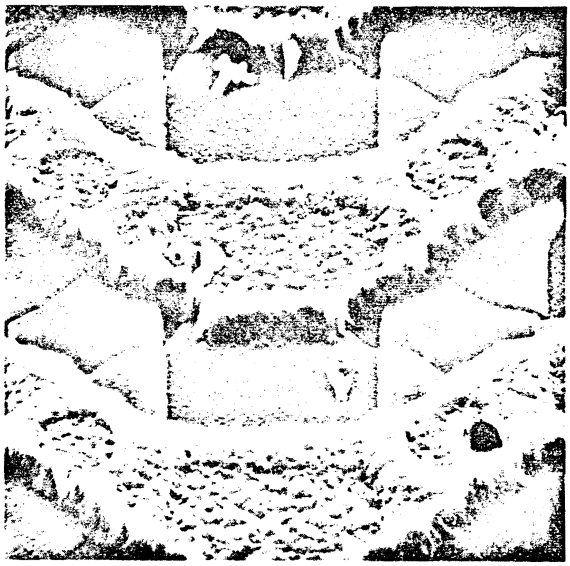

FIGURE 2
MULTIPLE ELECTRODE CCD (SEM)

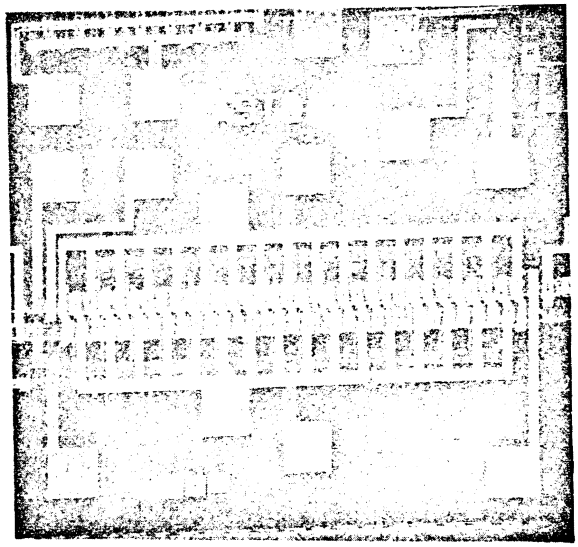

FIGURE 4A
32-BIT CCD (SEM)

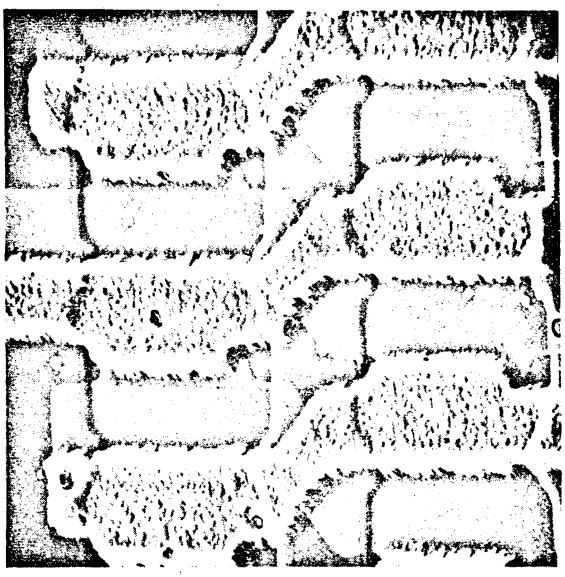

FIGURE 4B
ARRAY DETAIL 32-BIT CCD (SEM)

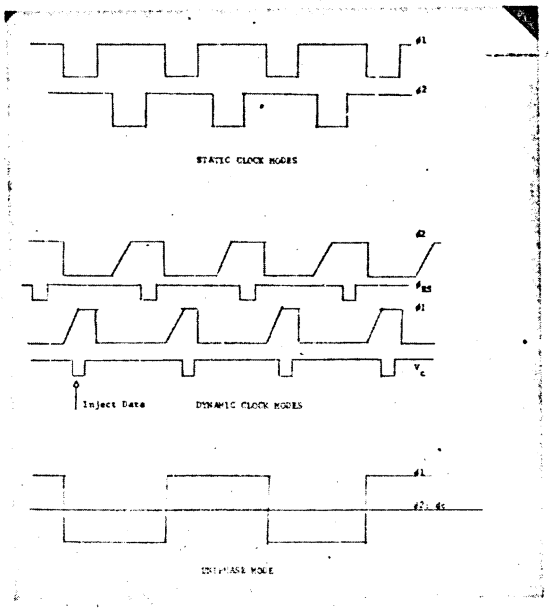

FIGURE 6
CCD OPERATING MODES

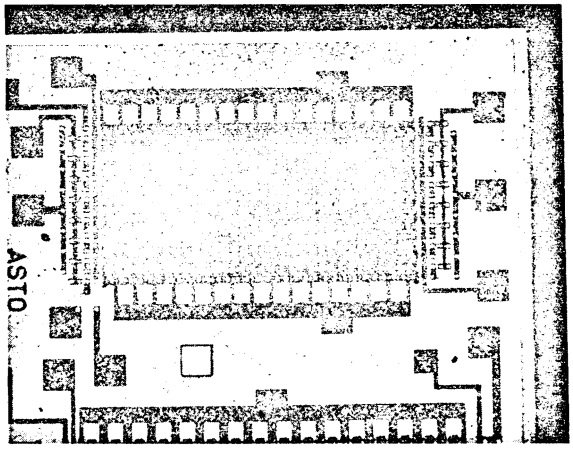

FIGURE 5
256-BIT REPEATER CHAINED CCD

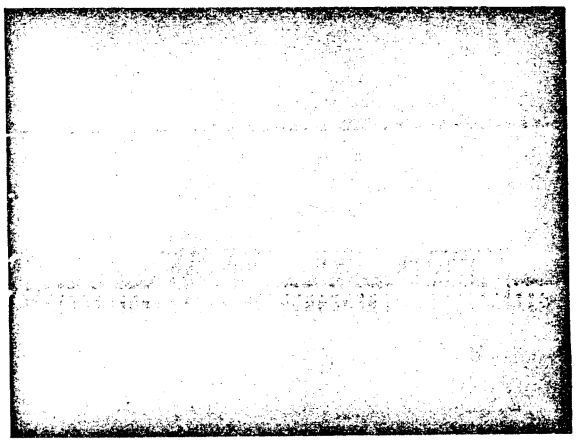

FIGURE 7
TRANSMISSION OF ARBITRARY BIT PATTERN
THRU 256-BIT CCD
INPUT = 10 V/CM; OUTPUT 1 V/CM; 50 μS/CM

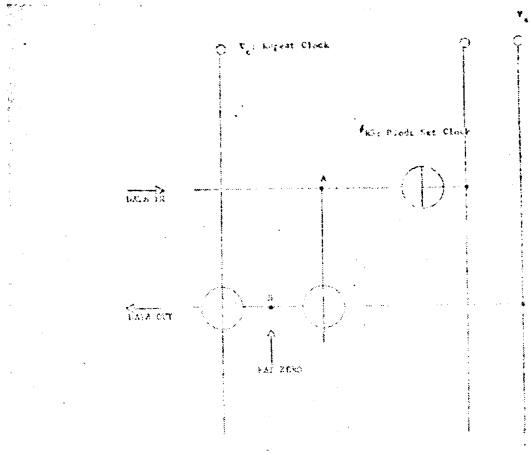

FIGURE 8
REPEATER STAGE SCHEMATIC

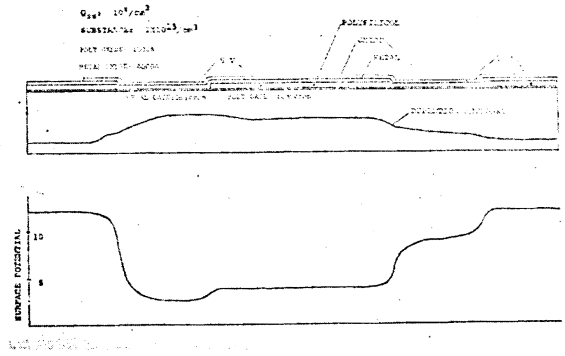

FIGURE 10
NUMERICAL SIMULATION OF CCD USING
FINITE ELEMENT TECHNIQUE

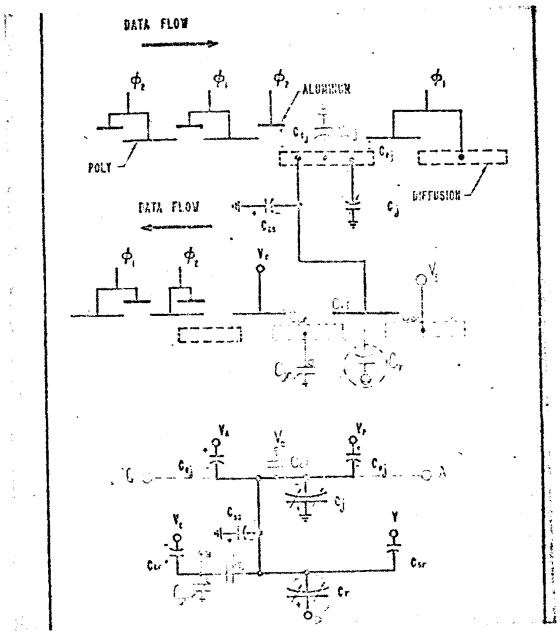

FIGURE 9
REPEATER STAGE ELECTRICAL DETAILS