PERFORMANCE CHARACTERISTICS OF CCD SHIFT REGISTERS FABRICATED USING ALUMINUM-ANODIZED ALUMINUM-ALUMINUM DOUBLE LEVEL METALLIZATION*

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ABSTRACT. The performance characteristics of n-channel 64-bit and 500-bit double-level metallization (Al-Al_2O_3-Al) linear surface channel CCD shift registers show excellent charge transfer efficiency, 99.98 percent at 1 MHz. This CTE was achieved on devices on 929 μm^2 (1.44 mil^2) per bit area. The stability of these devices is excellent when compared to three-phase single-level metallization devices. A novel double clocking scheme is used to drive the four-phase devices. These results indicate advantages of the Al-Al_2O_3-Al metallization system in ease of fabrication, testing, reliability, charge carrying capability, and high-speed operation of large arrays.

I. INTRODUCTION

Performance characteristics of 64-bit and 500-bit surface channel CCD linear shift registers fabricated with a double-level metallization technique are described in this paper.[1,2,3,4] Both metal levels are standard aluminum and the insulation between the two metallization levels is aluminum oxide formed by anodization. This technique relaxes the 3-μm (0.12 mil) electrode separation tolerance required for single-level metallization, since the thickness of the Al_2O_3 forms the interelectrode gap. The thickness of the Al_2O_3 ranges from 700 Å to 6,000 Å depending on the particular fabrication procedure used. Due to these extremely narrow gaps, the surface potential is controlled in the region between the electrodes, thus permitting operation with high transfer efficiency. The Al-Al_2O_3-Al structure also seals the interelectrode gap from ambient effects and provides an equipotential surface over the interelectrode gap. These devices are not affected by ambient conditions and are very stable, as opposed to single-level metallization devices which are extremely difficult to passivate. No high temperature processing (>500°C) is necessary during the double-level metallization process. Anodization provides a simple, quick method for forming the double-level system insulation. The high conductivity of both levels of metallization in the Al-Al_2O_3-Al system allows operation of large CCD arrays at high frequencies. The long RC time constants associated with "resistive seas" or polysilicon electrodes are absent in the Al-Al_2O_3-Al system and this allows both higher operating speeds and greater architectural design freedom.[3]

II. DEVICE FABRICATION AND OPERATION

The fabrication and operation of 8-bit anodized aluminum p-channel shift registers has previously been described.[1,3] These devices operated with approximately 99.9 percent CTE at 2 MHz. The electrode lengths were 25.4 μm (1.0 mil) and the channel width was 254 μm (10 mils) for a bit size of 2.6 X 10^4 μm^2 (40 mil^2). This paper describes the extension of this technology to the fabrication and operation of both 64 X 1 and 500 X 1 linear shift registers. These devices again used the same four-phase Al-Al_2O_3-Al double-level metallurgy; in addition, the devices were fabricated using n-channel technology.[5] This n-channel technique allowed higher frequency operation as a result of the increased mobility of electrons, and also decreased the possibility of metal opens by reducing the thick-to-thin oxide transition. The devices were fabricated on ⟨100⟩ p-type (Boron) 40-Ω-cm silicon. The gate oxide was 1,200 Å in thickness. The electrode length was 7.6 μm (0.3 mil) and the channel width was 30.5 μm (1.2 mils) for a bit size of 929 μm^2 (1.44 mil^2). The input of a 500 X 1 bit shift

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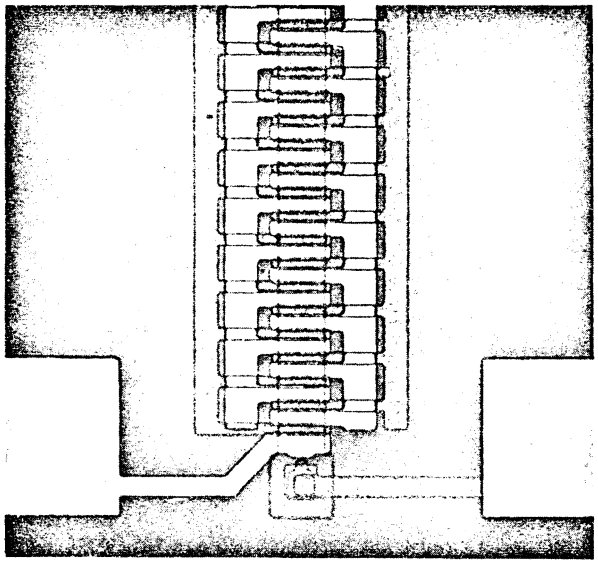

Figure 1. Photomicrograph of the Input of a 500 X 1 4-Phase Anodized Aluminum Double Level CCD Shift Register

register is shown in Figure 1. The input diode, the input gate, and approximately five bits of the shift register are shown. The white electrodes are the input gate and clock electrode phases two and four.

The chip itself contains both the 500 X 1 and the 64 X 1 4-phase anodized aluminum shift registers along with other CCD structures. The artwork for the chip was computer generated at Texas Instruments from cell designs and the resulting computer output was, in turn, fed to a computer-controlled pattern generator. The long length of the 500 X 1 shift register, 1.53×10^4 μm (602 mils) required that the photomasks be composed using four reticles. The resulting chip was approximately 8/10 of an inch long–2×10^4 μm (800 mils) and a photomicrograph of the chip is shown in Figure 2. Because of the length of the chip, only approximately one-third of the chip appears within the photomicrograph (one-fourth of the chip length extends from cross mark to cross mark).

Charge transfer efficiences of 99.98 percent at 1-MHz data rates have been achieved on these surface channel devices with narrow channel widths–30 μm (1.2 mils). Charge transfer loss (1 – CTE) versus frequency data for a typical device is shown in

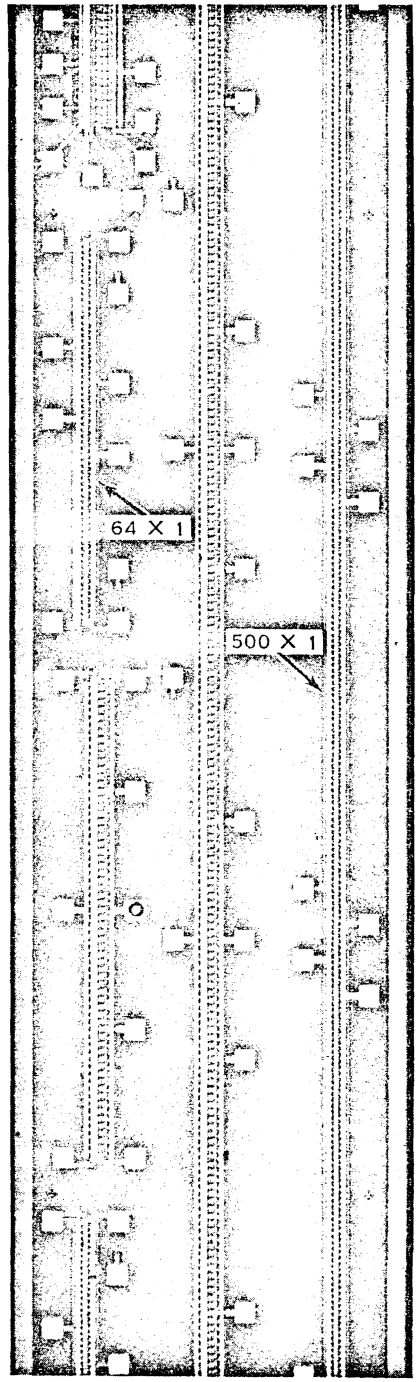

Figure 2. Photomicrograph of the 500 X 1 Anodized Aluminum CCD Shift Register in Wafer Form

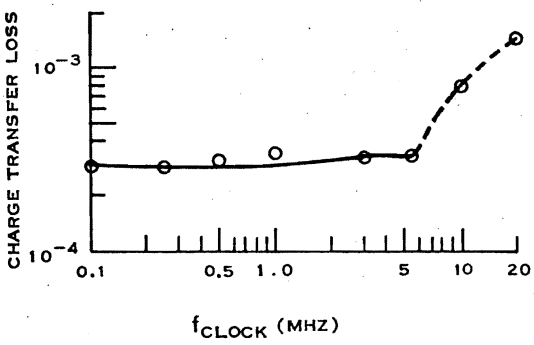

Figure 3. Loss Versus Frequency for a Four-Phase 64 Bit CCD

Figure 3. The measurements were taken with ≈15-percent fat zero and the waveforms of the clocks were varied to obtain the maximum transfer efficiency. The data below 10 MHz was taken with 15-volt clocks, while the data at 10 MHz and above was taken with 10-volt clocks, due to driver limitations. The charge transfer efficiency of surface channel devices is known[6] to depend on channel width and the charge transfer efficiency achieved on these Al-Al_2O_3-Al devices is essentially equivalent to the best charge transfer efficiency obtained from three-phase surface channel single-level metallization devices of similar geometry and fabrication schedule.

In general, these double-level Al-Al_2O_3-Al devices require lower clock voltages and are less sensitive with respect to clock waveforms than single-level metallization devices of similar geometry. Since the electrodes on both metallization levels are coplanar and of equal area with respect to the silicon substrate, novel clocking waveforms may be used to enhance the charge transfer efficiency. Figure 4 shows both the normal four-phase clocking and a new double clocking technique.[7] Consider the normal clocking method for a four-phase system, as shown in Figure 4(a). Each phase has a separate, distinct clock waveform which generates feedthrough. In the system shown in Figure 4(b), however, the clock phases are on for twice the normal duration; therefore, twice the normal amount of charge can be shifted down the register. This not only doubles the size of an output "one" but

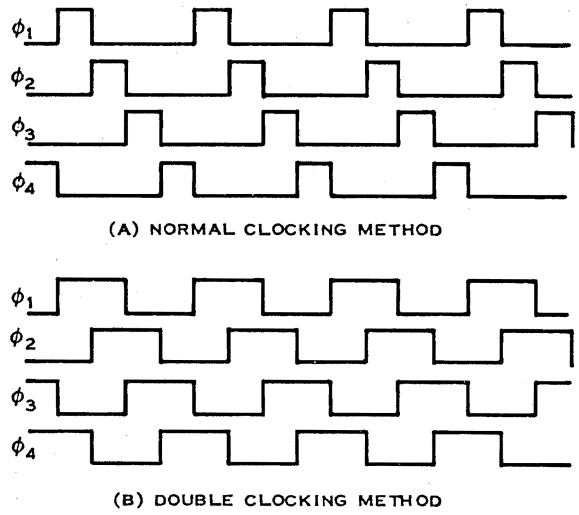

Figure 4. Four-Phase Clocking

also increases the charge transfer efficiency. This increase in charge transfer efficiency occurs because the area under an electrode is void of carriers for only half a clock cycle rather than for three-quarters of a clock cycle. The charge transfer efficiency results described above for the Al-Al_2O_3-Al devices were obtained using the double clocking technique.

Clock feedthrough into the output of a CCD is an important practical consideration that affects ultimate system noise. Although filtering the output signal at $f_c/2$ eliminates most of the clock feedthrough, any variation, or "jitter," on the clock lines results in subharmonics which cannot be eliminated by this method. The generation of the clocking pulses in the double clocking technique allows a considerable decrease in drive circuitry complexity because ϕ_1 and ϕ_3, along with ϕ_2 and ϕ_4, are mirror images of each other. Hence, both ϕ_1 and ϕ_3 can be generated from a single differential driver; the same situation is true for ϕ_2 and ϕ_4. The clock feedthrough suppression possible with the double clocking technique is superior to the normal clocking method since the fact that both ϕ_1 and ϕ_3 (ϕ_2 and ϕ_4) are generated from the same differential clock generators allows complete cancellation of clock feedthrough at the drivers themselves.

III. DISCUSSION

The Al_2O_3 insulation is also thin enough to suppress the channel potential wells in a buried channel structure. The Al-Al_2O_3-Al technique thus provides an attractive alternative to the "resistive sea" approach to buried channel electrode construction. However, in order to perform imaging with an Al-Al_2O_3-Al CCD, backside illumination of the CCD is necessary due to the opaque nature of the aluminum structure. In order to maintain resolution in a backside illuminated CCD structure, the device would have to be thinned to a thickness of approximately the center-to-center spacing of the resolution elements $\approx 30\ \mu m$ (1.2 mils). However, thinning a device to this thickness is also necessary for either a front or backside illuminated CCD in the near infrared where the absorption coefficient of radiation is quite low in Si ($\approx 5\ cm^{-1}$ at 1-μm wavelength). While thinning imposes additional fabricational difficulties, the backside illumination of an imager would optimize the sensitivity from two standpoints: (a) there is no metal on the backside to reflect the incident illumination and (b) optimum antireflection coatings (such as SiO) may be used on the backside. Antireflection coatings on the front side of a CCD are less than optimum since the CCD requires $\approx 1{,}200$ Å of gate insulator with a nonideal index of refraction to operate electrically. Furthermore, any polysilicon or glass overcoat layers will further reduce the quantum efficiency of the device.

Another option opened with a thinned CCD is the possibility of operating in the electron-bombarded silicon (EBS) mode. Theoretical calculations indicate that an EBS mode CCD operating at room temperature should be approximately 5 to 10 times more sensitive than a cooled (210K) CCD without the EBS stage. Thus, the ideal CCD area imager fabrication technique appears to be a backside illuminated, thinned, buried channel, anodized aluminum double-level metallization structure.

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