DESIGN AND PERFORMANCE OF CHARGE-COUPLED DEVICE TIME-DIVISION ANALOG MULTIPLEXERS*

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ABSTRACT. The charge-coupled device (CCD) possesses unique features which offer a new approach to time-division analog multiplexing in an integrated circuit format. The parallel-to-serial transfer capability permits simultaneous sampling of parallel signal channels with a single gate pulse. The ability of the CCD to store charge packets permits analog data to be sampled and stored in the device, and subsequently to be shifted out of the device serially with no intervening analog-to-digital conversion. The basic structure and operation of CCD time-division analog multiplexers is described and examples of specific design approaches, including those for integrated output circuits, are presented. The multiplexer operation is studied with respect to relevant performance factors such as charge transfer efficiency, dynamic range, attenuation, and interchannel crosstalk. The theoretical performance of CCD multiplexers in terms of interchannel crosstalk is given particular attention. A design technique is described which substantially decreases this crosstalk, by providing parallel channel inputs at alternate element positions along the CCD. The resulting structure is referred as the isolation-element multiplexer. Experimental results are presented for a 16-channel, isolation-element (n-channel) CCD analog multiplexer. Charge transfer efficiency values as a function of frequency and temperature are given for these prototype devices and measured noise levels are reported. A brief description of typical clock waveforms is given to familiarize the system designer with the support circuitry required.

I. INTRODUCTION

In the fields of communication, sonar, infrared imaging, and radar, a large number of electronic systems depend on pulse multiplexing techniques to process sensor information to a more suitable and efficient format before transmission. By far the best known and most widely used pulse multiplexing schemes are frequency-division and time-division. Multiplexing by time-division simplifies the system since relatively simple synchronous control replaces modulators, demodulators, carrier generators, and band-pass filters normally employed in frequency-division systems.[1] Hence, time-division multiplexing systems offer distinct advantages in systems application where simplicity, reliability, and economics are of utmost importance.

The charge-coupled device (CCD) possesses unique features which offer a new approach in implementing time-division analog multiplexing in integrated circuit form. The mode of operation of a CCD multiplexer is pulse-amplitude modulation. The CCD can sample and store analog data with no intervening analog-to-digital conversion. Input signals in all channels may be sampled simultaneously with a single gate pulse. Stored analog data in the CCD can be shifted sequentially out of the device by simple clock-controlled digital logic circuits. These features in conjunction with the advantages of integrated circuitry make it likely that CCDs will have a major impact in time-division multiplexing systems, paralleling the recent development of CCDs for other analog signal processing applications.[2,3]

The purpose of this paper is to describe the design and performance of a CCD time-division analog multiplexer. Section II discusses the CCD time-division analog multiplexer with respect to its principal of operation, structure, charge transfer efficiency, attenuation, interchannel crosstalk, dynamic range and noise. Experimental results are presented in Section III.

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II. CCD TIME-DIVISION MULTIPLEXERS

A. PRINCIPLES OF OPERATION

A schematic presentation of a time-division multiplexer is depicted in Figure 1(a). The function of a CCD multiplexer is to replace the circuitry within the dashed line. As indicated, this multiplexer converts N parallel input channel signals into a single-channel pulse-amplitude-modulated output. The input signals are sampled simultaneously. This eliminates the need for exact timing of synchronized pulse generators to determine the exact time slot in which each input channel is sampled, as is required in commutator-type systems. The sampled information is stored in the CCD as charge packets which, as depicted in Figure 1(b), are sequentially read out of the CCD and converted to an output signal, V_{out}.

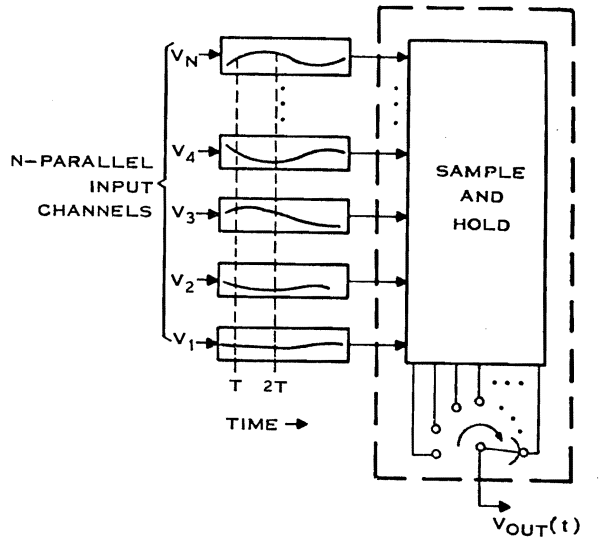
Structurally, a CCD multiplexer is a simple variation on the basic CCD structure, which is a sampled-data analog delay line.[4] This basic structure is illustrated in Figure 2(a), where the delay line elements are shown numbered from the output, and the block labeled S indicates a sampler. In the CCD multiplexer, inputs are applied to the delay line element positions, as depicted in Figure 2(b).

The layout design of a conventional surface-channel CCD analog delay line (n-channel) is shown in Figure 3. As is illustrated, the channel-stop diffusion (p+) is continuous along both outside edges of the phase electrodes (ϕ_1, ϕ_2, and ϕ_3 for a three-phase device). For a CCD multiplexer, a means must be provided for introducing minority carriers to the Si-SiO_2 interface in the delay line in a quantity proportional to the input voltage. Figure 3(b) shows a possible input design, in which input diodes are connected to every element position in the delay line via openings in the channel-stop diffusion. A parallel-to-serial transfer electrode $\phi_{p/s}$ is positioned between the M parallel input diodes and the delay line.

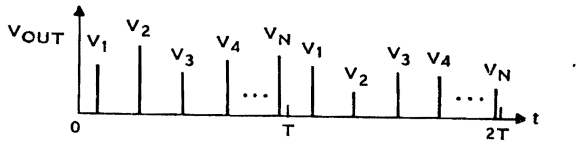
The operation of the input structure can be described by referring to Figure 4, which shows a cross-sectional view across the channel. Charge is transferred into the serial delay line when a potential well, a virtual drain, is created under the ϕ_2 electrodes, and when the $\phi_{p/s}$ electrode (which functions as the gate of an MOS device) is pulsed to a voltage greater than the threshold voltage, V_t, above V_k, the input voltage signal at the k*th* element position. The amount of charge entering the potential well at the k*th* element from the input node at time equal to zero, Q(k,0), is given by

$$Q(k,0) = C_{ox} (\phi_2 - V_t - V_k) \qquad (1)$$

where C_{ox} is the oxide capacitance and ϕ_2 is phase two clock pulse.

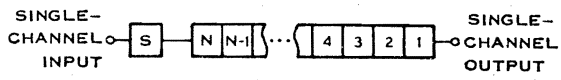


(A) BLOCK DIAGRAM OF A TIME-DIVISION MULTIPLEXER

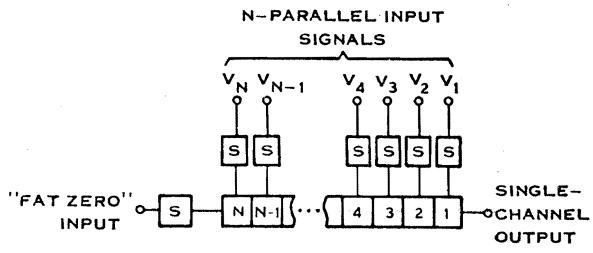


(B) SINGLE-CHANNEL OUTPUT WAVEFORM

Figure 1. Functional Representation of a Time-Division Multiplexer



(A) N-ELEMENT CCD DELAY LINE



(B) N-ELEMENT CCD MULTIPLEXER

Figure 2. Schematic of a CCD Delay Line and Multiplexer

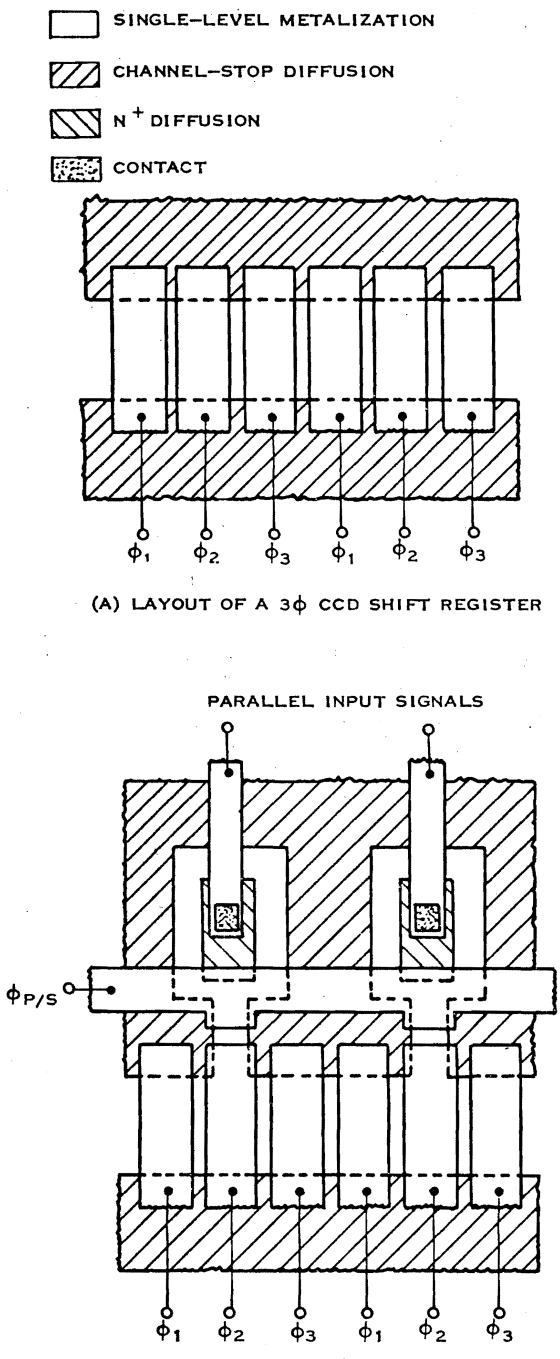


Figure 3. Layout Design of a CCD Delay Line and Multiplexer

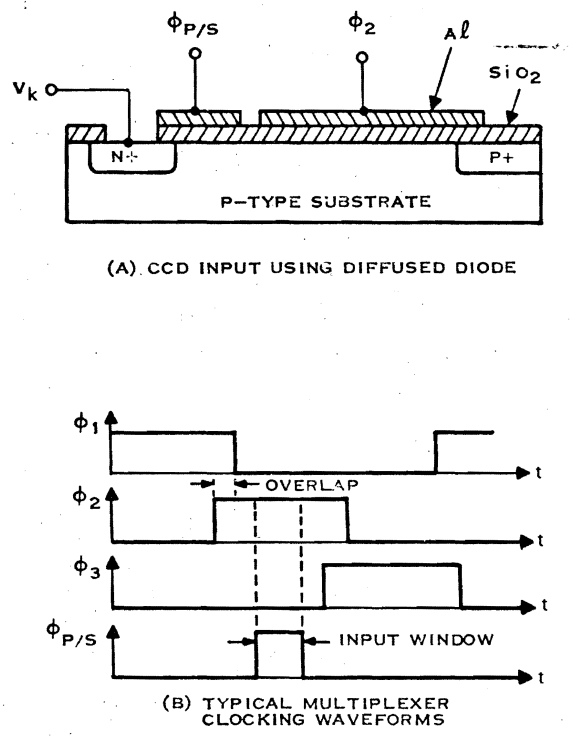


Figure 4. Input Diode Scheme and Clocking Waveform

A charge packet, upon reaching the output, changes the output node voltage by $\Delta V_{o/p}$, given by

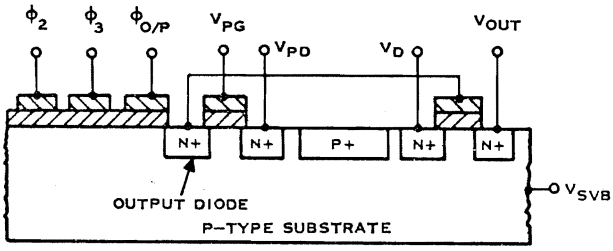
$$\Delta V_{o/p} = \frac{Q(0,k)}{C_{o/p}} \qquad (2)$$

where Q(0,k) is the amount of charge that is remaining in the charge packet initially at the k*th* element, after being shifted to the output node, and $C_{o/p}$ is the total capacitance associated with this node.

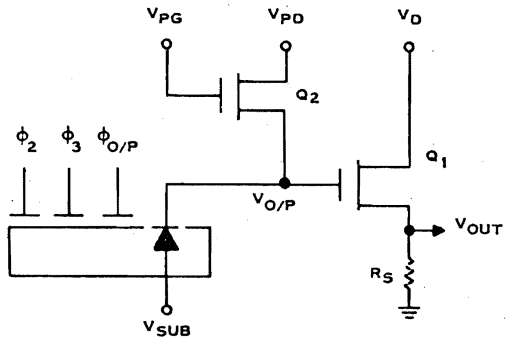
An on-the-chip preamplifier consisting of an MOS precharge device and an MOS source follower, as depicted in Figure 5, can be used to detect the output node voltage fluctuation caused by the arriving charge packet. The precharge terminology is suggested by the fact that the diode is precharged to a given voltage by a clock prior to being partially discharged by the charge packet.

B. CHARGE TRANSFER EFFICIENCY

A key consideration in the performance of a CCD is how efficiently the charge packet is transferred from one element to the next. In general, there is no net loss of charge, but a small fraction of a charge packet is usually left behind with each element transfer. For convenience in the following calculations, the efficiency of the transfer process will be expressed in terms of the quantity ϵ, which is the fractional loss per element into the trailing charge packet. That is, ϵ is the fractional amount of charge that is left in the trailing packet after p transfers, for a p-phase CCD. Charge transfer efficiency, CTE, can be expressed as $1 - \epsilon/p$.



(A) CROSS SECTION VIEW OF PREAMPLIFIER CIRCUIT



(B) PRECHARGE AND SOURCE FOLLOWER DEVICES

Figure 5. Schematic of the Output Preamplifier Circuit

There are many different factors which influence the CTE of a CCD multiplexer. In a surface-channel device, fast interface states are an important loss mechanism. At high frequencies, CTE becomes limited by diffusion time or field-aided-drift velocity effects;[5] the resulting charge loss into trailing packets will eventually become substantial, even in a buried-channel structure.

The gaps between the metal electrodes in the single-level metallization CCD structure cannot be made much smaller than 0.1 mil with conventional integrated circuit photolithography. If the oxide in the gap is exposed (i.e., not covered with a "resistive sea"), the surface potential cannot be effectively controlled there. As a result, "barriers" or "wells" may exist which can degrade the charge transfer efficiency.[6] In the CCD multiplexer structure, the effect of the exposed oxide is greater because the channel stop on one side of the serial portion of the device is interrupted to allow for the parallel inputs. At these points of interruption, an additional gap exists between the serial transfer electrode and the electrode controlling the parallel input. Thus, the charge transfer efficiency of the multiplexer structure can be inferior to that of the serial register with channel stops on both sides, unless either a resistive sea or a very small gap (~0.01 mil) process[7] is used.

In the CCD multiplexer, because of its layout structure, charge transfer inefficiency results in two effects that degrade its performance: nonuniform attenuation and interchannel crosstalk. These effect are discussed in the next two subsections.

C. NONUNIFORM ATTENUATION

As indicated in Figure 2(a) for a CCD delay line, all signal charge packets make the same number of transfers to the output. This is not the case for a CCD multiplexer. This variation from one channel to the next in the number of signal packet transfers can result in nonuniform attenuation of the different signals. The amount of charge in a packet at the k*th*-element position of an N-element multiplexer at time t, Q(k,t), is given by[8]

$$Q(k,t) = \sum_{k'=1}^{N} G(k' - k,t)\, Q(k',0) \qquad (3a)$$

where

$$G(k'-k,t) = \begin{cases} \binom{t}{k'-k} (1-\epsilon)^{k'-k}\ \epsilon^{t-k'+k}, \\ 0 \leqslant k \leqslant k' \leqslant N,\ t \geqslant k' - k \end{cases}$$

$$= 0, \text{ otherwise;} \qquad (3b)$$

and where $Q(k',0)$ is the charge packet in the $k'th$-element position at time equal to zero and $\binom{t}{k'-k}$ is a binomial coefficient. The unit of time is one element transfer period. Since the primary point of interest is at the multiplexer output ($k = 0$), the above expression is simplified to give

$$Q(0,t) = \sum_{k'=0}^{\min[N,t]} \binom{t}{k'} (1-\epsilon)^{k'}\ \epsilon^{t-k'}\ Q(k',0) \qquad (4)$$

where min[N,t] designates the lesser of the quantities N and t. This expression shows that, if a quantity of charge Q(k,0) is introduced into the multiplexer at only a single input, the primary output packet will be of magnitude Q(0,k), where

$$Q(0,k) = (1 - \epsilon)^k\ Q(k,0) \qquad (5)$$

Therefore, a variation in the amount of attenuation exists which is dependent on the location of the input signal. The maximum attenuation is approximately

$$Q(0,N)/Q(N,0) \approx 1 - N\epsilon \qquad (6)$$

When N and ϵ are of such magnitudes that attenuation affects the performance of the multiplexer, each channel can be normalized prior to multiplexing or at the demultiplexer. However, instabilities in the magnitude of ϵ with time may require periodic channel renormalization in exposed-gap CCD structures. Design techniques for greatly reducing the nonuniformity and instability in attenuation caused by the multiplexer will be described in Subsections E and F.

D. INTERCHANNEL CROSSTALK

Signal charge attenuation caused by CTE effects is accompanied by dispersion of the charge distribution within the CCD; this dispersion of multiplexed data appears as interchannel crosstalk. When a quantity of charge, Q(k,0), is injected into the kth element and then shifted to the output ($k = 0$), a fraction of the charge will be left behind not only at the kth element but at all intervening elements. These remaining charge packets give rise to interchannel crosstalk. A method is discussed in this section for reducing interchannel crosstalk to levels acceptable for most system specifications, even when the CTE is low (≈99.9 percent).

Equation (4) may be expanded to determine the principal factors that cause crosstalk:

$$Q(0,k) = (1 - \epsilon)^k\ Q(k,0) + k\epsilon\ (1 - \epsilon)^{k-1}\ Q(k-1,0)$$

$$+ \frac{k(k-1)}{2!}\ \epsilon^2\ (1 - \epsilon)^{k-2}\ Q(k-2,0)$$

$$+ \ldots \qquad (7)$$

The first term of this equation gives the attenuation of the primary charge packet, which is identical in form to the right-hand side of Equation (5). The remaining terms give the charge that is transferred into the primary charge packet as the result of other charge packets introduced between the kth element and the output at time equal to zero. If k is large and ϵ is small, the above can be written as

$$Q(0,k) \approx (1 - k\epsilon) \left[1 + k\epsilon + \frac{(k\epsilon)^2}{2!}\right] Q(k,0) \qquad (8)$$

where all charge packets at time equal to zero are assumed to be identical.

The interchannel crosstalk due to charge transfer inefficiency, ICR, is defined as the ratio of the amount of charge that is lost into the primary packet by other charge packets to that of the primary charge packet when measured at the output. From the above equation, the interchannel crosstalk can be written as

$$ICR \approx k\epsilon + \frac{(k\epsilon)^2}{2!} \qquad (9)$$

where the first term is due to the charge packet initially at position $k - 1$ and the second term is due to the charge packet initially at position $k - 2$. If the $(k - 1)$ input signal is eliminated, the interchannel crosstalk becomes

$$ICR \approx \frac{(k\epsilon)^2}{2!} \qquad (10)$$

Therefore, interchannel crosstalk can be decreased substantially in a CCD multiplexer when only alternate element positions are used for input signals. This

technique provides for an isolation charge packet to exist between consecutive primary signal charge packets.

The interchannel crosstalk for a CCD multiplexer with inputs at every element position and with inputs at alternate element positions as a function of the number of input channels for various CTEs is shown in Figures 6 and 7, respectively. The maximum interchannel crosstalk for an N-element CCD multiplexer with M parallel inputs at alternate element positions exists between the M and (M – 1) input signals. From Equation (10), the maximum crosstalk can be expressed as

$$ICR_{max} \approx 2(M\epsilon)^2 \qquad (11)$$

The design of a CCD multiplexer with inputs at alternate element position is discussed next.

E. ISOLATION-ELEMENT CCD MULTIPLEXER

Figure 8 shows a schematic of a CCD multiplexer with parallel channel inputs at alternate element positions, where there are M input signals and N CCD elements. From an application viewpoint, this device is more accurately described as an M-channel, isolation-element CCD multiplexer. A photomicrograph of a 16-channel, isolation-element (n-channel) CCD multiplexer is shown in Figure 9.

In this design, the channel-stop diffusion was made continuous at element positions which did not have an input diode. There are three electrodes per element position with electrode length of 0.4 mil and

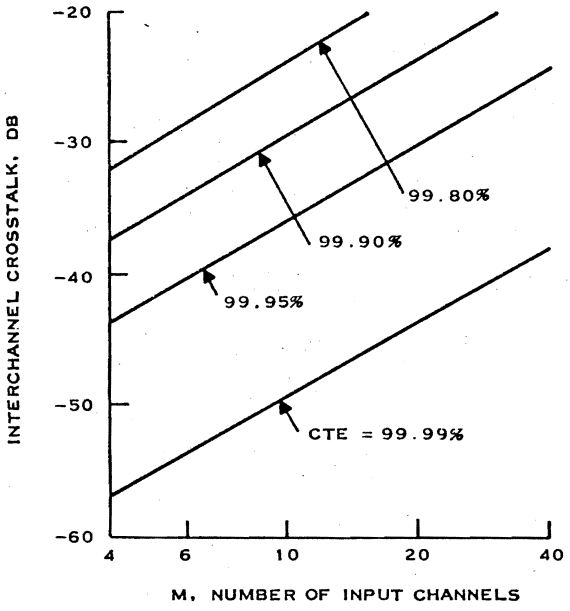


Figure 6. Maximum Theoretical Interchannel Crosstalk: Input at Every Element Position

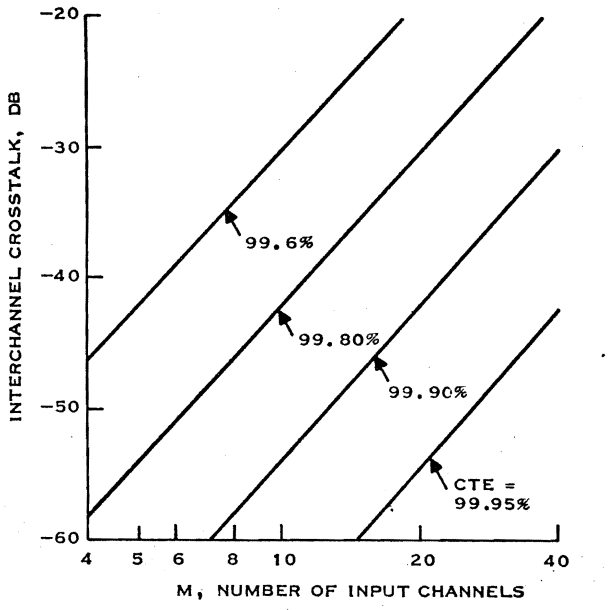


Figure 7. Maximum Theoretical Interchannel Crosstalk: Input at Alternate Element Positions

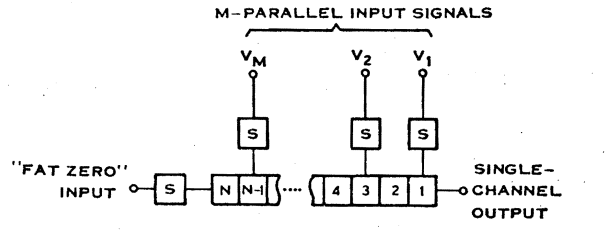


Figure 8. Schematic of an M-Channel, Isolation-Element Multiplexer

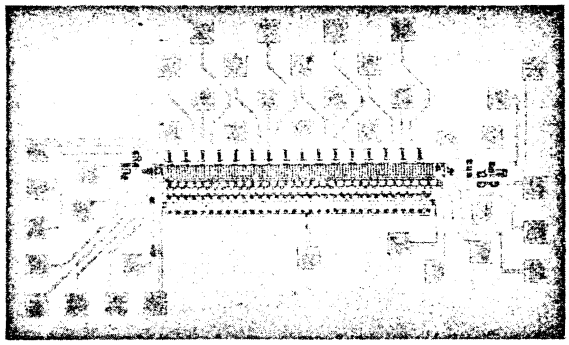


Figure 9. Photomicrograph of a 16-Channel, Isolation-Element CCD Multiplexer

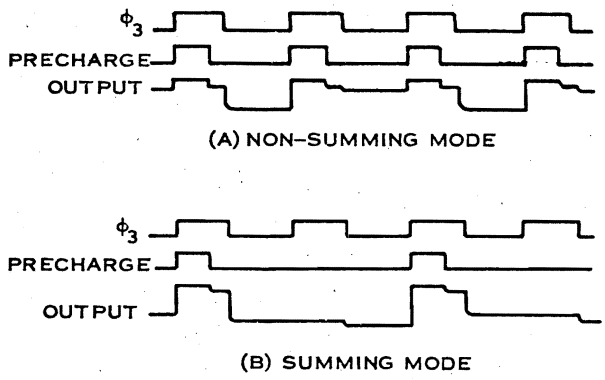


Figure 10. Isolation-Element Multiplexer Timing Diagram

width of 2.0 mils. The gap between the electrodes is typically 0.1 mil. The input diode method is used for the input circuit, while the MOS precharge device and source follower is used for the output amplifier.

The basic operation of the isolation-element multiplexer is identical to the CCD multiplexer with inputs at every element position except for two aspects. The first, as stated above, is that input data is transferred into the multiplexer at only every other element position. The second is that for the same output data rate, the clock frequencies of the phase electrodes must be doubled.

Two methods can be used to obtain the output voltage signal. The first is to monitor the voltage fluctuations of the primary charge packet and to dump the isolation packet. The second is to sum the primary and isolation packets, thereby reducing attenuation resulting from CTE effects. This may be expressed algebraically

$$Q(0,N) \approx [(1 - \epsilon)^N + N\epsilon]\ Q(N,0)$$

$$\approx Q(N,0) \qquad (12)$$

Hence, the isolation-element CCD multiplexer not only reduces interchannel crosstalk, but when operated with summed outputs, reduces attenuation effects.

The clocking waveforms for an M-channel, isolation-element CCD multiplexer are shown in Figure 10. The primary and isolation packets are summed by precharging the output node only immediately before the arrival of the primary charge packet, which occurs at the turnoff of the phase-three electrode, as shown in part (B) of the figure.

F. DUAL ISOLATION-ELEMENT CCD MULTIPLEXER

An extension of the above approach is shown in Figure 11. The primary feature of this scheme is that the clock frequency of the phase electrodes is the same as the output data frequency. As illustrated in this figure, there are two isolation-element multiplexers, A and B, the outputs of which are alternated to a single output node. This design is referred to as the dual isolation-element CCD multiplexer. The inputs are so positioned relative to the outputs that, during serial readout, while a primary packet is arriving at the output of multiplexer A, an isolation packet is arriving at the output of multiplexer B. In a sequence of four steps, illustrated in Figure 12, a

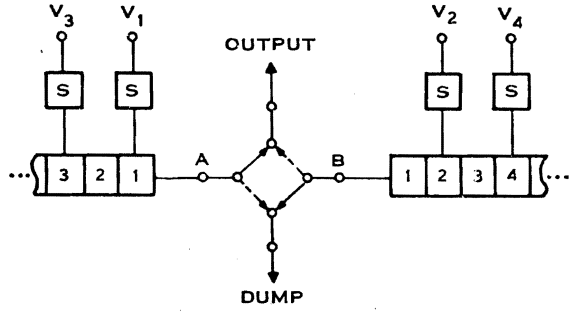


Figure 11. Schematic of a Dual Isolation-Element CCD Multiplexer

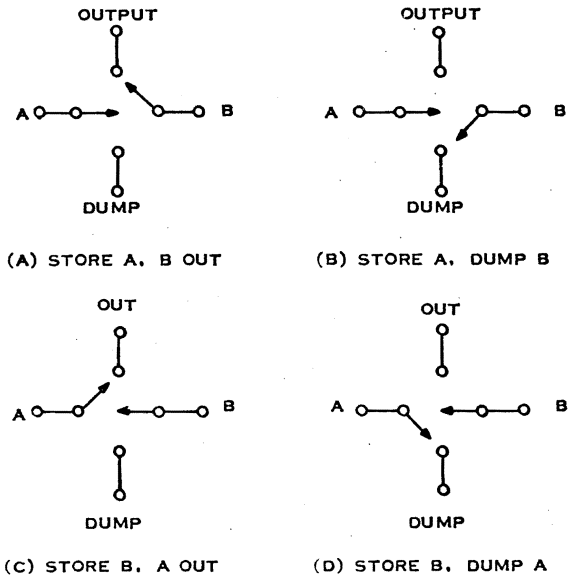
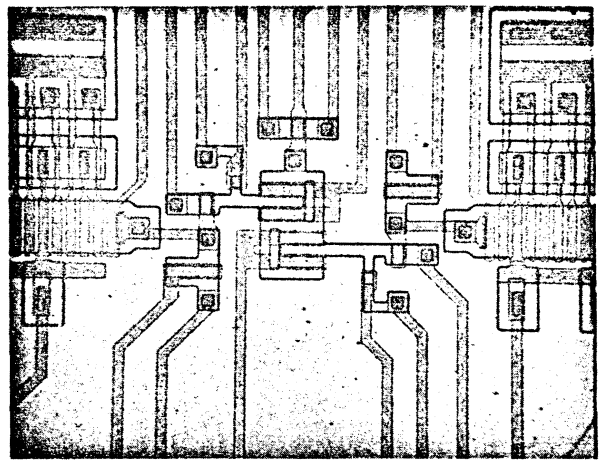


Figure 12. Simplified Operation of the Dual Isolation-Element CCD Multiplexer Commutator



OUTPUT CIRCUIT

Figure 13. Photomicrograph of the Dual Isolation-Element CCD Multiplexer Commutator

primary packet is summed with its isolation packet at the output of each register, and the voltages corresponding to the sums are alternately presented to the commutator output. After an output voltage has been sampled, that charge packet is dumped. In Figures 12(A) and 12(B), the primary and isolation packets are being summed at the output of multiplexer A, while the voltage at the output of multiplexer B is being sampled, and then this charge dumped. In Figures 12(C) and 12(D), the roles of multiplexers A and B are reversed.

A photomicrograph of the commutator on the dual multiplexer is shown in Figure 13 and its equivalent circuit schematic is shown in Figure 14. Operation of the device may be explained by referring to Figure 14(B), which gives the pulse waveforms applied to the commutator. Charge packets are ejected from both multiplexers A and B upon the turnoff (fall) of the ϕ_3 clock pulse. One of the packets will be a primary packet and the other an isolation packet. Suppose the primary packet is ejected by multiplexer A, and the isolation packet by B. The primary packet partially discharges the gate capacitance of Q_{A2} ; the gate of Q_{B2} has already been partially discharged by a primary charge packet, and is now further discharged by the isolation packet. The voltage, V_B, on the gate of

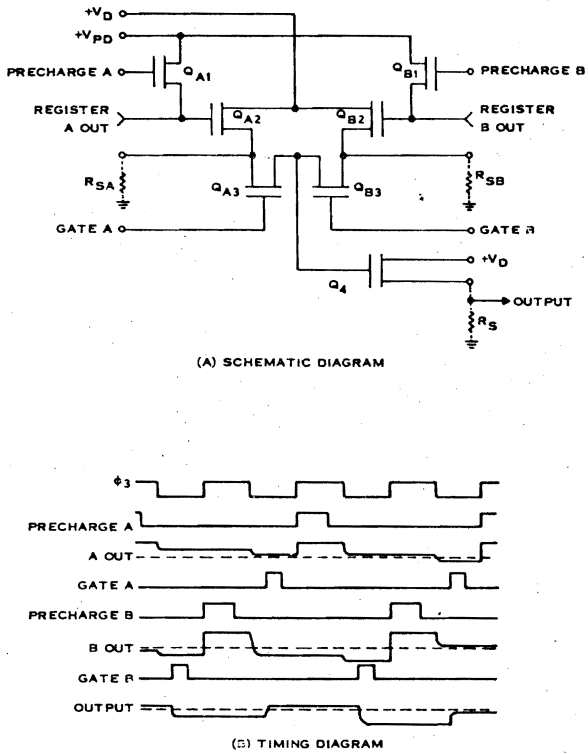


Figure 14. Schematic of the Dual Isolation-Element Multiplexer and Timing Diagram

Q_{B2} is representative of the sum of the charge in this earlier primary packet and that in the present isolation packet. Sample gate B (Q_{B3}) is now pulsed on, bringing the gate of Q_4 to approximately $V_B - V_T$, where V_T is the threshold voltage for the device, since Q_{B2} is operated as a source-follower. The output voltage swings to about $V_B - 2V_T$, and will hold at this voltage after Q_{B3} is turned off. A precharge (positive) pulse is now applied to the gate of Q_{B1}, restoring the output node of multiplexer B to its initial voltage. Upon the next turnoff of the ϕ_3 clock pulse, a primary pulse is ejected from multiplexer B and an isolation pulse from register A, and the entire sequence is repeated, but with the roles of multiplexers A and B interchanged.

Thus, the output circuitry of the dual isolation-element multiplexer functions both as a commutator and as a sample-and-hold gate. Aside from this circuitry, each half of this multiplexer is identical to the single isolation-element multiplexer described above, and thus will have the same degree of interchannel crosstalk.

G. DYNAMIC RANGE AND NOISE

The dynamic range of a CCD is defined as the range of input signal voltages over which it can be usefully operated as a linear device. Since the analog signal information is converted to charge packets in the CCD, the number of minority carriers contained in these packets is a measure of the upper limit of the input signal. The noise associated with charge packets can be considered as an uncertainty in the number of charge carriers in a given electrode well. This uncertainty places a lower limit on the input signal.

There are a number of sources of noise in a surface-channel CCD analog shift register.[9,10] The significant noise sources will be:

Fat zero noise

Input noise

Preamplifier noise

Fast interface state noise.

Dark current noise will be insignificant for most CCD multiplexers. For example, a 20-channel, alternate-input CCD multiplexer would have to be operated at an output clock rate lower than 500 Hz before dark current noise would be of any consequence, at room temperature.

As has been reported previously,[11] the first three noise sources listed above may all be reduced by proper design and operation to the level associated with presetting a small ($\lesssim$0.2 pF) capacitance, C_{noise}, to a given voltage. That is, the rms number of noise electrons introduced in each case will be about

$$n_{noise} \approx \sqrt{kTC_{noise}}$$

where C_{noise} is the capacitance associated with the particular type of noise source.

This expression, along with that for fast interface state noise, is listed in Table 1. Also listed in the table are calculated noise magnitudes, obtained using parameter values representative of the 16-channel isolation-element multiplexer described above. For convenience, the rms noise levels are also expressed in terms of equivalent input noise voltage for this multiplexer. The total rms noise is calculated to be 520 μV. The rms maximum linear signal voltage for the device was about 3.3 V, referred to the input. Thus, the dynamic range is calculated to be

$$\text{DR (calculated)} = \frac{3.3}{5.2 \times 10^{-4}}$$

$$= 6400{:}1$$

or 76 dB.

An interesting peculiarity of fast interface state noise in a surface-channel CCD multiplexer is worth noting. Whereas the fast interface state noise is correlated at the output of the multiplexer, just as it is at the output of any surface-channel CCD,[12,13] it will be uncorrelated in any given demultiplexed channel. Thus, fast interface state noise at low frequencies will be more significant in CCD multiplexer applications than in, say, CCD imager applications.

III. EXPERIMENTAL RESULTS

The performance of the 16-channel isolation-element CCD multiplexer is discussed in this section, with respect to such operational factors as charge transfer efficiency as a function of frequency and temperature, interchannel crosstalk, charge packet summation, and signal-to-noise ratio.

To measure CTE as a function of frequency and temperature, the parallel-input transfer gate was biased off, and the multiplexer was operated as a simple analog delay line. The CTE was measured using the pulse train technique, wherein a series of large charge packets, or "ones," followed by a series of small packets, or fat zeros, are introduced through the fat

TABLE 1. SIGNIFICANT SOURCES OF NOISE IN SURFACE-CHANNEL CCD MULTIPLEXERS

	Fat Zero Noise [10]	Input Noise [10]	Preamplifier Noise [10]	Fast Interface State Noise [9]	Total Noise
Theoretical Expression	$\approx\sqrt{kTC_{FZ}}$	$\approx\sqrt{kTC_{IN}}$	$\approx\sqrt{kTC_{OUT}}$	$kTN_{SS}\,A_g\,pN2\ln 2$	$[\Sigma(\ )^2]^{1/2}$
Parameters for 16-Channel, Isolation-Element CCD Multiplexer	T = 300 K $C_{FZ} \approx 0.2$ pF	T = 300 K $C_{IN} \approx 0.2$ pF	T = 300 K $C_{OUT} \approx 0.2$ pF	T = 300 K $N_{SS} = 10^{10}$ eV^{-1} cm^{-2} $A_g = 5 \times 10^{-6}$ cm^2 p = 3 N = 32	
Calculated Quantities: RMS Number of Noise Electrons, and Equivalent RMS Input Noise Voltage	285 225 μV	285 225 μV	285 225 μV	425 340 μV	650 520 μV

zero input diode of the multiplexer. The total charge lost from the leading edge of the output pulse train, divided by the charge in a single steady-state one, is set equal to $N\epsilon$.

The measured CTE as a function of clock frequency at room temperature is shown in Figure 15. For comparison purposes, the measured CTE of a CCD delay line having continuous channel-stop diffusions on both sides of the channel, with the same channel and electrode dimensions as the multiplexer, is also shown in this figure. At high frequencies, both sets of data approach the same curve, as carrier diffusion-time loss dominates over the loss caused by potential fluctuations in the interelectrode gap region.

Figure 16 gives the measured CTE as a function of temperature, between −50°C and +60°C. This data was taken at a clock frequency of 1 MHz. Within experimental error, no significant variation in CTE is noted over the temperature range shown.

Attenuation of individual charge packets due to charge transfer inefficiency in the multiplexer was measured by using a dc level applied to the first 10 channels of the 16-channel isolation-element multiplexer. The first 10 channels were biased so as to produce a uniform summed output signal. The remaining six input channels were biased in such a manner as to avoid modifying the fat zero level. The schematic of the arrangement is shown in Figure 17(A). The output waveform is shown in part (B) of this figure. The output precharge device was operated in the summing mode. The bottom two series of voltage pedestals show the voltages corresponding to the primary charge packets and to the sums of the primary and respective isolation charge packets. The upper of

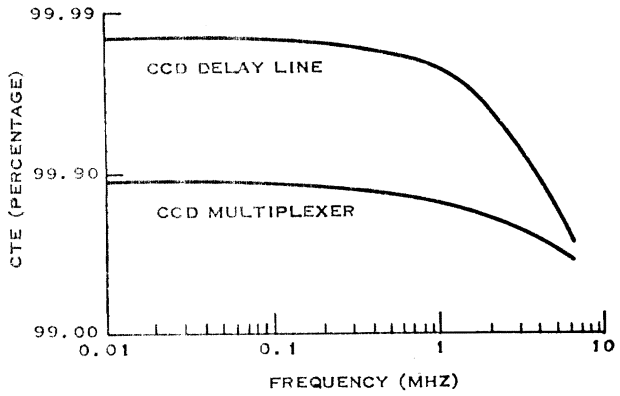


Figure 15. Measured Charge Transfer Efficiency as a Function of Frequency

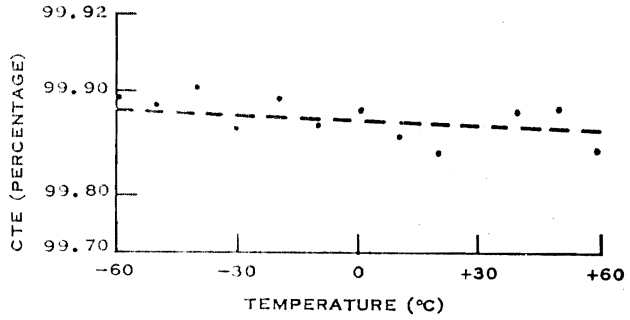


Figure 16. Measured Charge Transfer Efficiency as a Function of Temperature

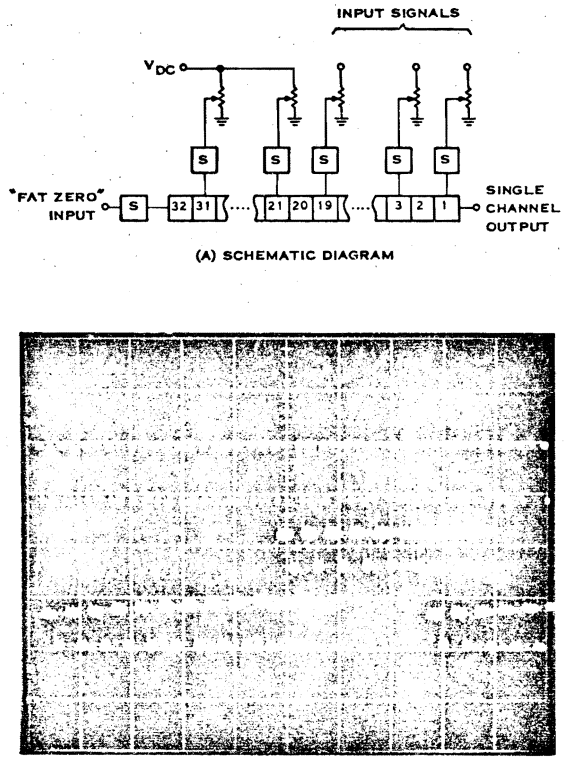


Figure 17. A 16-Channel, Isolation-Element CCD Multiplexer With Ten Input Signals

these two series of voltage pedestals shows the nonuniform attenuation of the primary charge packets as the channel number is increased. The bottom series of pedestals is formed when the isolation charge packets are summed with their respective primary packets at the output node. The resulting waveform illustrates the reduction in nonuniformity of attenuation that may be achieved through summing.

Figure 18 compares calculated with measured crosstalk for two 16-channel isolation-element multiplexers The calculated crosstalk curves are based on CTEs for the two devices measured using the pulse train technique. The agreement between calculation and measurement is evident.

In Subsection II.G, the dynamic range of the 16-channel isolation-element multiplexer was calculated to be about 76 dB. The actual rms output noise

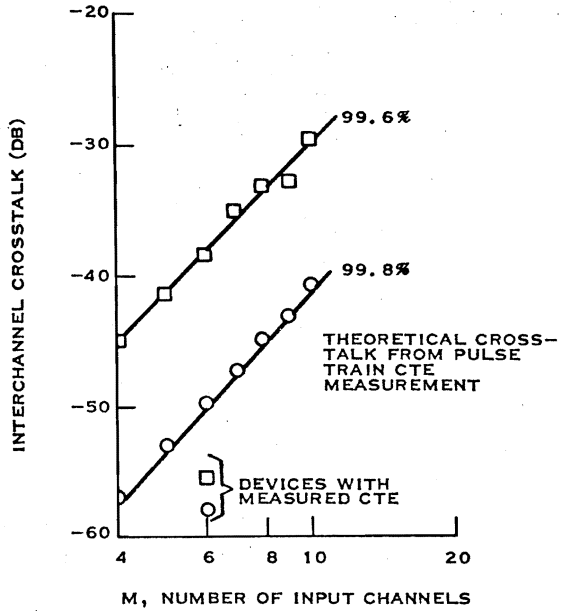


Figure 18. Maximum Theoretical and Measured Interchannel Crosstalk: Input at Alternate Element Positions

level of this device, referred to the input, has been roughly estimated to be about 6 mV, for a dynamic range of about 550:1, or 55 dB. The discrepancy between calculated and measured values may be a result of sampling noise in the output circuitry, or to the fact that the signal input structure on this device does not lend itself to the minimum-noise mode of operation described in Reference 11.

The 16-channel isolation-element CCD multiplexer is presently being evaluated for a prototype 10-channel multiplexing application. For this application, each channel frequency is bandlimited to 25 kHz. The CCD multiplexer sampling frequency, f_s, was chosen to be 100 kHz. Hence, the CCD clock frequency, f_c, is given by

$$f_c = 2\,Mf_s$$

$$= 2\ \text{MHz}$$

which requires a serial transfer frequency of 6 MHz. Figure 19 shows data obtained with the 10-channel multiplexer operated at the above clock frequency. To avoid visual confusion in this figure, time-varying signals were applied at only four of the inputs. The top trace shows the multiplexed output, while the lower traces show the four demultiplexed channels with time-varying waveforms.

Preliminary data obtained with the dual isolation-element CCD multiplexer is shown in Figure 20. The four low-frequency waveforms show the time-varying inputs applied to four of the 16 channels. The high-frequency waveform is that of the multiplexed output of the device. The output clock frequency was 200 kHz.

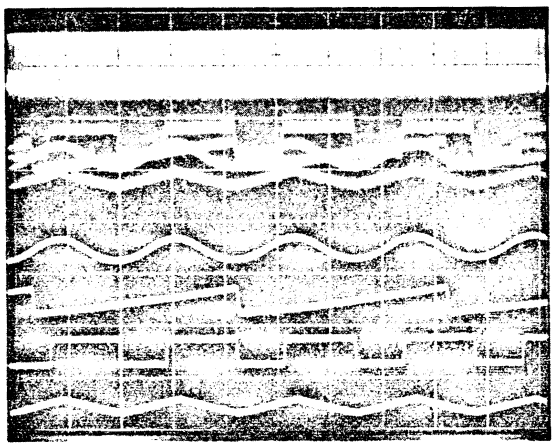


Figure 19. Operation of a 16-Channel, Isolation-Element Multiplexer at a Frequency Rate of 2 MHz

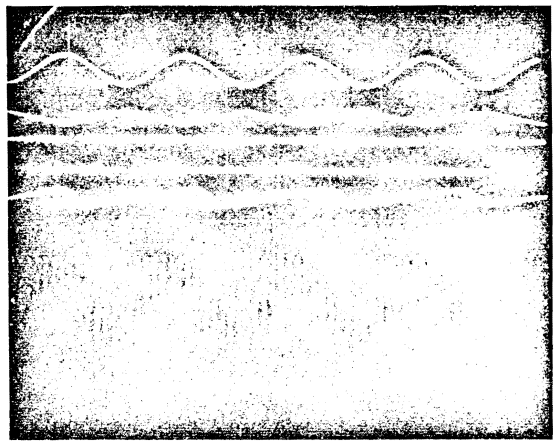


Figure 20. Operation of a Dual Isolation-Element Multiplexer at a Frequency Rate of 200 kHz

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REVERSE SIDE BLANK