A PARALLEL INPUT, HIGH SPEED CCD ANALOG DELAY LINE

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ABSTRACT. A charge coupled device (CCD) analog delay line has been designed with input taps that accept parallel input signals at points along the delay line. These input taps have been designed such that the tap input signal adds to the signal charge transferring through the delay line. Moreover, attention has been given to maximizing the analog signal bandwidth and signal-to-noise ratio of the device.

INTRODUCTION

Charge coupled device (CCD) delay lines are useful in many analog signal delay applications. The device discussed in this report has been designed to accumulate analog signals appearing sequentially at the detector array. Input taps are provided on the delay line to accomplish this time-shifted summation.

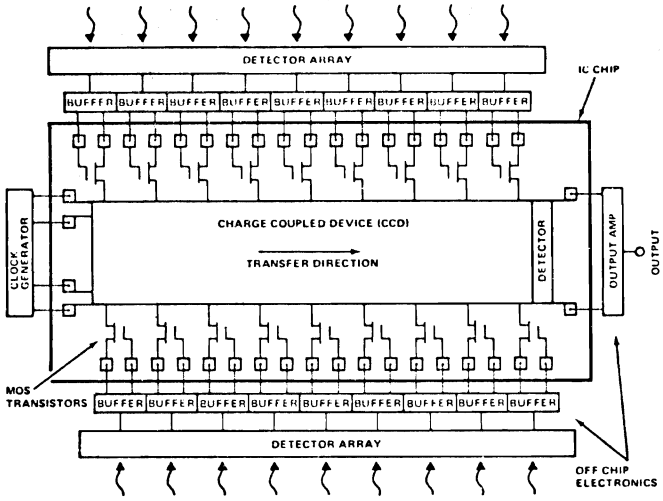

Fig. 1. Analog Delay Line Application

INPUT TAP DESIGN

A number of CCD input tap designs were considered. Emphasis was placed on achieving accurate summation of the input signals. An MOS transistor current source was ultimately selected as the signal injection source. This device can be readily fabricated on the CCD substrate beside the CCD channel. This monolithic structure minimizes the undesirable stray tap capacitance that loads the CCD channel. Mismatches in the MOS transistor threshold voltage of different taps, and nonlinearities of the MOS transistors are reduced by a feedback technique. To accomplish this increased linearization and matching, the source and drain of each MOS tap transistor are separately brought off the chip (through bond wires) and placed in the feedback path of an off-the-chip operational amplifier.

THE CCD DESIGN

The design of the CCD was tailored for wide bandwidth and large signal-to-noise ratio. Minimum line widths (5μ line and spaces) were chosen for the two-phase structure to realize a wide bandwidth. A wide CCD channel (500μ) was designed to maximize the signal charge, thereby reducing the harmful effects of shot noise. The useful width of the channel is constrained in this CCD by the length of time required to fill the channel from the signal insertion tap at the CCD edge. This lateral filling from the signal insertion tap gives rise to a slewing phenomenon in the parallel input CCD delay line which results in the large signal of the delay line being less than the small signal bandwidth. A small signal bandwidth greater than 2 MHz and a signal-to-noise ratio greater than 60 dB is anticipated from this device.

CONCLUSIONS

A useful parallel input analog delay line may be fabricated using monolithic MOS transistor current sources in the feedback loops of off-the-chip operational amplifiers.

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