BURIED CHANNEL CHARGE COUPLED DEVICES FOR INFRARED APPLICATIONS†

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ABSTRACT. Results of experiments with buried channel charge coupled devices (CCD) are presented. The data shows that these have adequate signal and noise characteristics for infrared signal processing applications. An overlapping gate buried channel CCD structure is discussed. It is also shown that the gate controlled diode is a useful device for determining channel depths and leakage currents in the buried channel structure.

INTRODUCTION

Charge coupled devices (CCD) can be used for reading out arrays of infrared detectors. Such integrated CCD detector arrays or monolithic focal plane arrays (MFPA) will allow new high performance missions to be accomplished with infrared sensor systems and, in addition, will permit such systems to be significantly smaller and less expensive.

Using CCD's as in charge coupled imagers to read out the signals from mosaics of infrared detectors has, at first glance, the advantage of providing simplified non-scanned sensors. One major difference between the visible and far infrared spectral bands is the scene contrast. This contrast is 3.7 percent and 1.6 percent per degree centigrade for the 3 to 5 μm and 8 to 14 μm spectral bands, respectively, for 300°K backgrounds. For the sensor to distinguish a temperature difference of 0.1°C, there must be a uniformity between detector elements of about 0.37 percent to 0.16 percent. This uniformity is more than ten times higher than currently processed detectors and silicon CCD's have. Hence, direct (TV-like) CCD readout of infrared staring mosaic sensors is not considered practical at this time, particularly when materials other than silicon are used for both the detector and the CCD.

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This paper deals with the design and processing of CCD's that are used for reading out scanned arrays of infrared detectors. Such devices must have high transfer efficiency at relatively high clock rates, low channel noise, and low surface generation currents. Since in the buried channel CCD the signal charge is stored and transferred underneath the silicon surface, it appears that this type of CCD can best meet the infrared applications requirements.

TIME DELAY AND INTEGRATION

One particularly interesting method of reading out detectors in infrared systems is time delay and integration (TDI), which is illustrated schematically in Figure 1. A linear array of N detectors is read out by clocking the CCD in synchronism with the target motion so that the individual detector signals are added; the result is that the signal to noise ratio (S/N) is enhanced by $\sqrt{N}$, and a bandwidth identical to that of a single detector element is maintained. This mode of readout provides the increased S/N without high bandwidth and detector uniformity requirements, both of which are difficult to achieve.

Figure 2 is a microphotograph of a 64-bit TDI CCD (Hughes CCD-2058) with 32-input pads (on 4-mil centers) that connect to the infrared detectors. The device is tapered so that the relative filling of the CCD buckets remains constant over the length of the register. A typical

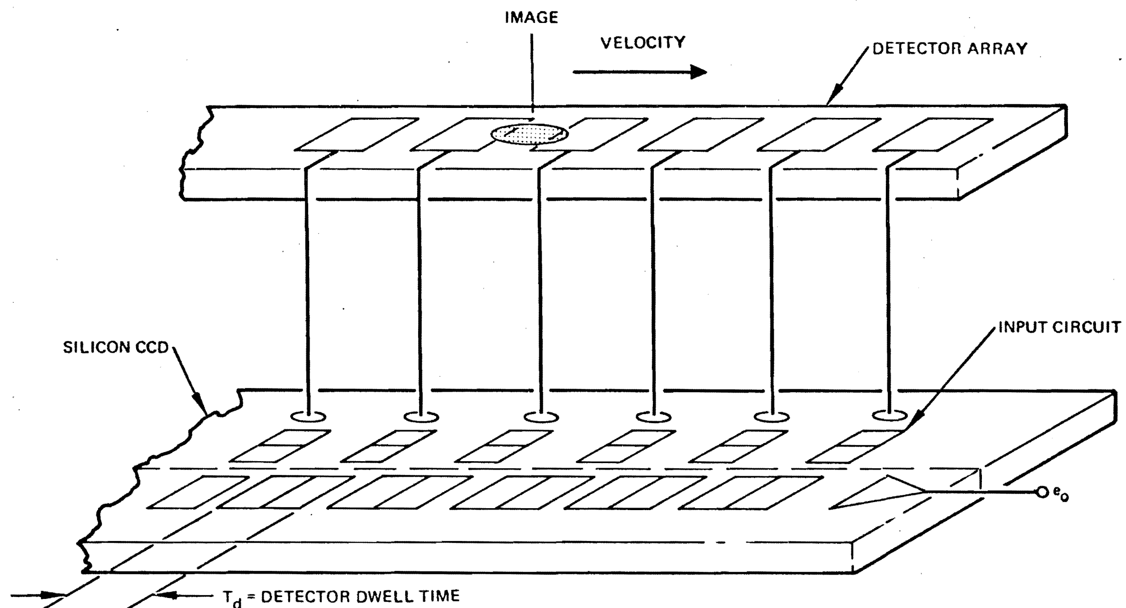

Figure 1. Time delay and integration of infrared detector signals

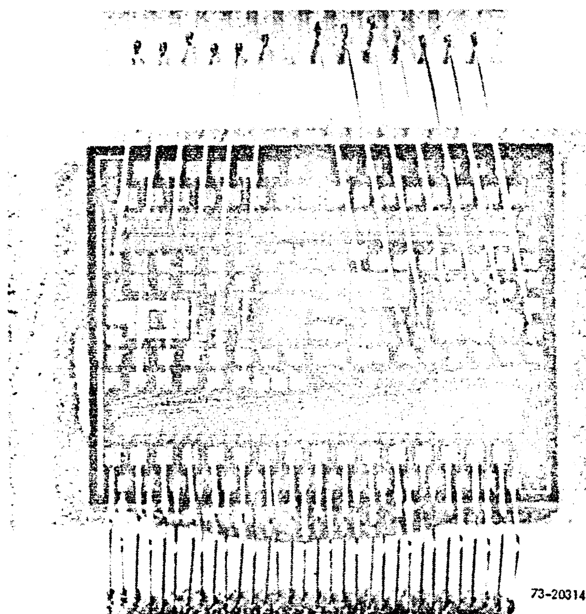

Figure 2. TDI CCD-2058 chip

background charge fat-zero is 20 percent of the saturation charge, which is typically 1×10^{12} charges/cm^2 for a buried channel CCD.

The time delay between taps equals the number of bits n between taps times the CCD clock period T_c [†]. The detector center to center spacing is typically twice the detector width; hence, the tap to tap transit time is $2\tau_d$, where τ_d is the dwell time of a single detector. Synchronization between target and CCD requires that $nT_c = 2\tau_d$. The Nyquist sampling theorem states that the minimum sampling rate is once per detector dwell time, i. e., $\tau_d = T_c$ and, hence, $n = 2$ is the minimum number of bits per tap in the case where the center to center spacing of the detector equals twice the width of the detector.

Figure 3 is an oscilloscope picture of a Hughes CCD-2058 TDI CCD waveform. The integrated output from a series of input pulses is shown in the lower trace, and two of the 32 input signals (inputs 4 and 24) are displayed in the upper traces. Note that the signals are added coherently with minimum pulse dispersion when the input signals are synchronized with the CCD clock frequency.

If the target transit time between taps is not equal to $2T_c$ as required for synchronization, the output pulse is dispersed in time. The output pulse amplitude is then given by the expression

† Table 1 defines the symbols used in this paper.

Table 1. Definition of symbols

Symbol		Definition
k	=	Bolzmann's constant = 1.38×10^{-23} joule/^oK
e	=	electronic charge = 1.6×10^{-19} coulomb
β	=	relative integration time of output coupler
C_o	=	output capacitance of diffusion and MOST
C	=	capacitance of CCD bucket, farads
V	=	applied voltage, volts
g_m	=	transconductance of input MOST, mhos
η	=	detector quantum efficiency
T_c	=	f_c^{-1} = clock period, seconds
T_s	=	f_s^{-1} = transfer gate period, seconds
Q_B	=	background photon flux, photons/cm^2-sec
R_s	=	source resistance, ohms
N_t	=	density of trapping states/cm^2-joule
C_{gs}	=	gate-source capacitance, farads
A_d	=	photodetector collecting area, cm^2
A	=	one-half CCD bit area, cm^2
μ^*	=	surface mobility, cm^2/v-sec
W	=	CCD channel width, cm
L	=	CCD input gate length, cm
T	=	temperature, ^oK
N_b	=	number of CCD bits
N	=	number of detectors
f	=	frequency, Hz
ω	=	$2\pi f$, rad/sec
$Z(f)$	=	sinusoidal signal transfer impedance of CCD, ohms
τ_d	=	detector dwell time, seconds
τ	=	$R_s C_{gs} (1 + g_m R_s)^{-1}$ = time constant, seconds
C_{ox}	=	oxide capacitance, farads/cm^2

Table 1 (Continued)

$$\text{sinc}(x) = \sin(\pi x)/(\pi x)$$

$$Z_o = \beta T_c/C_o = \text{low frequency transfer impedance, ohms}$$

$$G_o = g_m R_S(1 + g_m R_S)^{-1} = \text{gain}$$

$$W_o = Z_o G_o = \text{normalized transfer impedance, ohms}$$

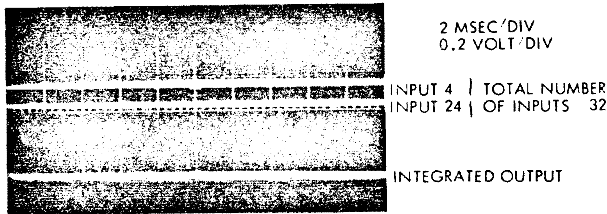

Figure 3. CCD-2058 TDI waveforms

$$a(\alpha) = \sum_{i=1}^{N} a_i[t_o - 2iT_c(1 - \alpha)] \qquad (1)$$

where

$\alpha = \tau_d/T_c$ = de-synchronization parameter

N = number of taps in register

i = detector tap index as counted from output

a_i = input amplitude at i^{th} tap

t_o = constant delay time

If all of the input amplitudes are equal, all taps for which $2i|1 - \alpha| \leq 1$ give an output at time t_o. The taps for which $1 \leq 2i|1 - \alpha| \leq 2$ provide an output to $t_o + T_c$, etc. until the index $i = N$. The condition for no dispersion is $|1 - \alpha| < (2N)^{-1}$. With $N = 32$, this condition gives ±1.6 percent synchronization tolerance for the target dwell time with respect to the clock period.

BURIED CHANNEL CCD

As originally conceived[1, 2], the buried channel CCD consists of a series of electrodes with small (1 μm) interelectrode gaps. To fabricate such a structure with high yield, it is necessary to carefully control the width of the gap. For this reason Hughes has developed a modified overlapping silicon-aluminum electrode[3] (see Figure 4). Conventional photolithographic techniques can be employed in fabricating these overlapping electrodes, and the potential wells are self-aligned. If charge transfer efficiency and charge storage capacity per unit area are to be optimum, it is apparent that the buried polycrystalline electrode should store the charge since it can be made larger than the other electrode, but this complicates the buried channel CCD structure.

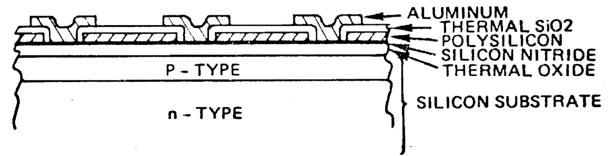

Figure 4. Cross sectional view of overlapping Al-Si gate buried channel CCD

In surface channel CCD's having this structure, the insulator under the aluminum electrode is usually made thicker so that the built-in storage well is under the silicon electrode. Two phase operation is then possible. In the buried channel CCD, in contrast, the role of the electrodes is reversed since they act to reduce the channel potential. Therefore, the charge will be stored where the insulator is thickest. Although a structure that has a thicker insulator under the silicon electrode is clearly suggested, it does not appear feasible from a processing yield viewpoint.

The structure shown in Figure 4, which requires four clocks, has demonstrated high yield. The lightly doped p-type layer

is made with a 2×10^{12} ion/cm^2 boron implant. The gate insulator consists of a sandwich of silicon dioxide underneath silicon nitride. After the polysilicon electrodes are deposited and etched, the wafer is thermally oxidized to form the low pinhole density insulator between the aluminum and the silicon electrodes. The oxidation masking properties of silicon nitride keep the thickness of the insulator in the gap between the silicon electrodes from changing. In the final CCD, both MIS structures are essentially identical except for differences in the electrodes.

When the CCD is functioning in the buried channel mode, the mobile signal charge is always underneath the silicon surface. In this case, the effect of the fast interface states on the CCD noise is primarily that from the shot noise of surface generation currents.

It is important to ascertain that the channel is indeed buried for particular levels of clock voltages and for given amounts of stored charge in the channel. The charge distribution in the potential well has been derived(4) analytically for specific doping profiles. Since the final dopant profile, after various drive-in heat treatments, is difficult to predict, one must measure the actual channel potentials and channel depths to ascertain buried channel operation. This type of measurement can be facilitated by using a gate controlled diode as shown in Figure 5. The following analysis is similar to that of surface channel gate controlled diodes(5).

Essentially the p^+ - n diffused junction is used to gain access to the buried channel. When the reverse bias of the diode is large, the empty channel potential will be less than the p^+ potential, and the channel will be depleted of holes. As the p^+ potential is reduced, holes will begin to flow into the channel when the p^+ potential equals the empty channel potential. As the p^+ potential is further reduced, the channel potential will build until it equals the p^+ potential.

It is possible to infer the channel depth by measuring the capacitance between the gate and channel as a function of the gate voltage for a particular channel potential. Figure 5 shows a typical set of C-V curves. For large negative gate voltages, the channel extends to the surface, and the capacitance is the insulator capacitance C_{ox}. As the negative gate voltage is reduced, the surface potential eventually becomes depleted, and the capacitance is

$$C = \frac{C_{ox} C_D}{C_{ox} + C_D} \qquad (2)$$

where C_D is the capacitance of the depleted silicon between the surface and the channel.

The shelf on each of the curves is of the buried channel region. For more positive gate voltages, the channel becomes depleted and the capacitance decreases to a minimum value characteristic of that in the gate to substrate depletion region. It is therefore possible to directly measure C_D and then to calculate the channel depth d from the relation

$$d = \frac{\epsilon_s A_G}{C_D},$$

where

A_G = gate area = 10^{-3} cm^2

ϵ_s = permittivity of silicon

Figure 5 shows the calculated values of d, which are found to match the theoretical predictions.

It is also interesting to note that the curves for various substrate voltages coincide when a channel is present. The channel depth depends only on the gate to channel voltage. Moreover, it was found from channel to substrate capacitance measurements that the channel to substrate depletion width depends only on the channel to substrate voltage.

The gate controlled diode is useful in determining the various leakage currents I_J of the buried channel CCD as well. These results are also shown in Figure 5. The C-V curves help to explain the leakage current curves. For large negative gate voltages, the surface is not depleted and the leakage current is primarily due to bulk generation-recombination (G-R) centers in

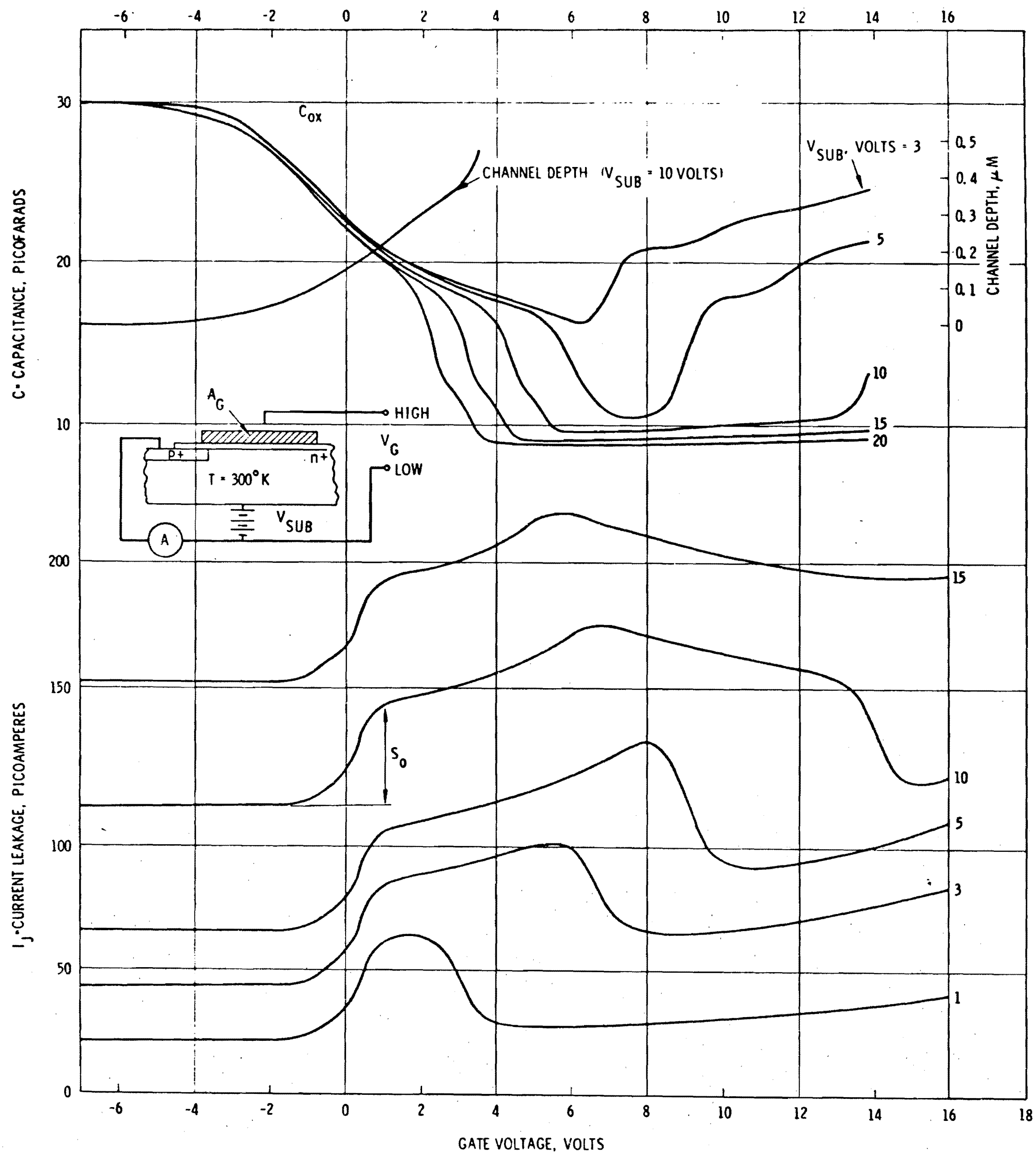

Figure 5. Capacitance, channel depth, and leakage as a function of gate voltage for buried channel gate controlled diode

the substrate to channel depletion layer. Near zero volts, the surface becomes depleted and the current increases because of the surface G-R centers. After depletion, the current continues to increase since the channel is becoming deeper and narrower and thereby exposing more bulk G-R centers. The behavior of the leakage current at more positive voltages depends on the channel potential. At low channel potentials (low V_{SUB}), the surface voltage inverts and becomes n-type. Further increases in the gate voltage do not affect the channel potential because the n inversion layer has a screening effect. Also note that coupling of the gate to the substrate via the n inversion

layer increases the capacitance. The leakage current decreases since the surface is no longer depleted. For higher channel potentials, the channel becomes entirely depleted before the surface potential inverts; this is seen for V_{SUB} = 10 volts in Figure 5. The leakage current exhibits a maximum that is coincident with the drop in gate to channel capacitance. This signifies that the channel disappears. This observation was confirmed when the channel current in a similarly biased transistor disappeared.

It is not clear why the leakage current decreases between the time the channel disappears and the potential at the surface inverts. From the capacitance measurements, it is clear that the gate to substrate capacitance does not change. The decrease therefore cannot be due to a decreasing depletion width.

From the leakage current data, the surface recombination velocity was found to be 30 cm/sec, and the bulk lifetime was approximately 2 μsec. Better values have been obtained by using HCl during gate oxidation and by using phosphorous gettering. Since the CCD devices are often located on the infrared focal plane, which is at nearly 77°K, the required leakage currents are more easily obtained.

CCD SIGNAL AND NOISE

The noise in CCD's has been examined quite extensively[6, 7]. Figure 6 shows the a-c input circuit that is equivalent to a CCD. The input resistor generates the usual Nyquist noise voltage spectral density equal to $(4kTR_s)^{1/2}$. The input MOST channel has a current spectral density equal to $(2/3\ 4kTg_m)^{1/2}$. The fluctuations associated with the charge transfer between bits is caused by the fast trapping states. The variance of the number of holes after $2N_b$ transfers is

$$\mathrm{Var}\ n = 2.8\ kTAN_tN_b \qquad (3)$$

These parameters are defined in Table 1.

There is also an f^{-1} noise of the output MOST device that dominates the other noise sources at low frequencies.

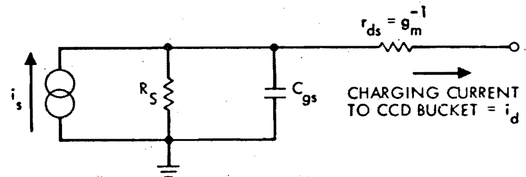

Figure 6. A-c equivalent input circuit

By properly taking into account the effects of the input circuit in Figure 6 and the sampler, the output integrator, and the signal gain, one can show that the output voltage spectral density (volts/ $\sqrt{\mathrm{Hz}}$) due to these sources is:

Nyquist Noise:

$$v_J = W_o \left(\frac{4kT}{R_s}\right)^{1/2} \left[1 + \frac{2}{3\ g_m R_s}\right]^{1/2} \left|F_1(f)\right| \qquad (4)$$

Fast Trapping State Noise:

$$v_s = eZ_o\ (5.6\ kTAN_tN_bf_c)^{1/2} \left|F_3(f)\right| \qquad (5)$$

Channel Thermal Noise:

$$v_c = 4\tau f_c Z_o\ (8/3kTg_m)^{1/2} \left|F_2(f)\right| \qquad (6)$$

Output MOST Noise:

$$v_f = v_o / \sqrt{f} \qquad (7)$$

The parameters are defined in Table 1. The spectral shape functions F_1 and F_2 are both given by the expression

$$\left|F(f)\right|^2 = \mathrm{sinc}^2\ (\beta f T_c) \sum_{\ell=-\infty}^{\infty} u(f + \ell f_c) \qquad (8)$$

F_1 is found by inserting $u = u_1$

where

$$u_1(f) = \text{sinc}^2(fT_s)\left[1 + (\omega\tau)^2\right]^{-1}, \qquad (9)$$

and F_2 is found by inserting $u = u_2$

where

$$u_2(f) = \sin^2(\pi f T_s)\left[1 + (\omega\tau)^2\right]^{-1} \qquad (10)$$

The third spectral shape function $F_3(f)$ is given by

$$\left|F_3(f)\right|^2 = \text{sinc}^2(\beta f T_c)\left[1 - \cos(\omega T_c)\right] \qquad (11)$$

The total noise spectral density at the CCD output is the square root of the sum of the squares of the individual spectra. The formulas have been found to agree well with measured data for the inputs to the types of circuits shown in Figure 6.

The transconductance g_m in these expressions is calculated in references 8 and 9.

Noise spectra of several CCD's have been measured and compared with values obtained by using the theoretical expressions above. Figure 7 shows one spectrum; the data was taken when the CCD's were operating at 77°K and with three different clock frequencies. The low frequency noise spectral density is dominated by the 1/f noise in the output MOST. Above about 100 Hz, the fast surface state noise dominates. The characteristic peaking in the spectrum at one-half the clock frequency is apparent in this data[10, 11]. The equivalent surface state density in the data is $N_t \cong 5 \times 10^{10}/\text{cm}^2\text{-ev}$. Lower values have been observed. As predicted by the theoretical expression for v_s, the spectral density is proportional to the inverse square root of the clock frequency.

The associated signal spectrum of the CCD with the type of circuit given in Figure 6 is shown in Figure 8 for the same device at the same temperature and clock frequencies. The input resistance R_s was 1.4×10^5 ohms in this experiment.

Another noise spectrum, which is referenced to the CCD input, is shown in Figure 9 for a clock frequency f_c = 2.4 mHz. The associated signal response is shown in Figure 10. Both sets of data were taken at T = 300°K.

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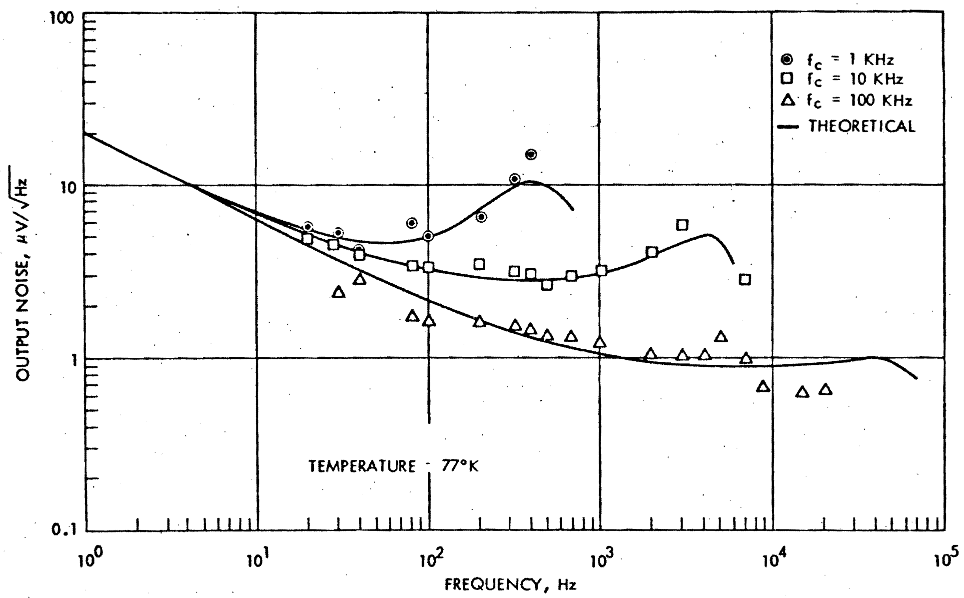

Figure 7. Output voltage noise spectrum of buried channel CCD-2054 No. 72

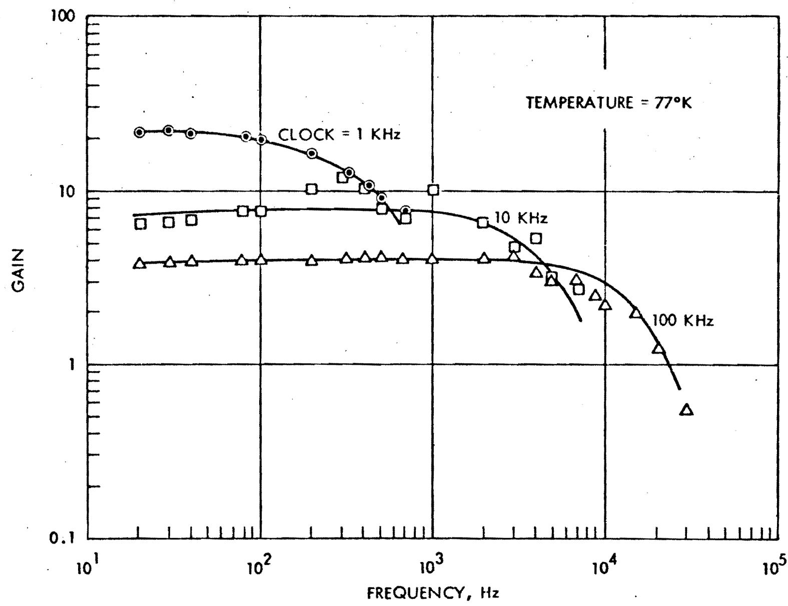

Figure 8. Signal gain as a function of frequency for buried channel CCD-2054 No. 72

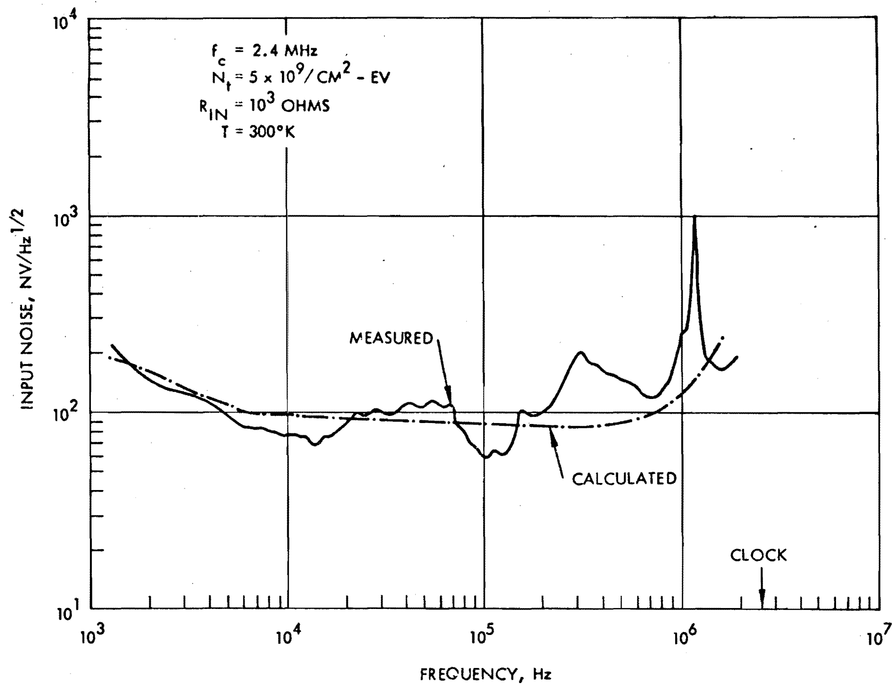

Figure 9. Buried channel CCD noise spectrum for CCD-2504 SG-16 No. 75

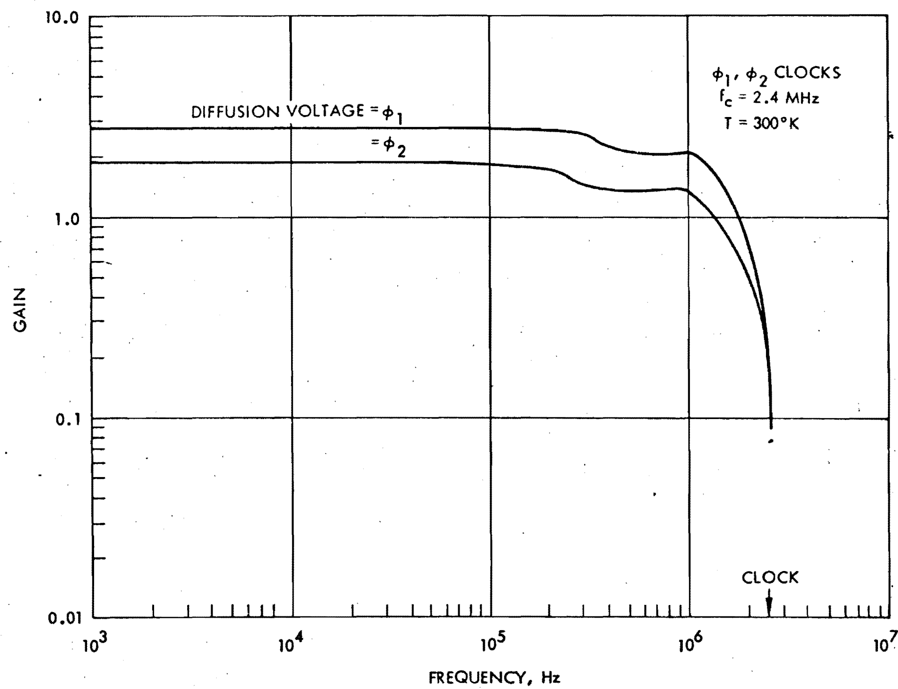

Figure 10. Measured voltage gain as a function of frequency for CCD-2504 SG-16

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