DARK-CURRENT AND STORAGE-TIME CONSIDERATIONS IN CHARGED-COUPLED DEVICES*

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ABSTRACT Room temperature operation of charge-coupled devices used in imaging and signal-processing applications often places strict requirements on the allowable dark current. This has focused attention on the need for achieving low and uniform dark currents. The various sources of dark current and their relative importance are reviewed; a convenient method for material and process characterization with regard to dark current is outlined. This permits the determination of parameters, which provide important feedback information to the device processor. The effects of plastic deformation caused by thermal stressing which can occur during processing of the slice and the fixed-pattern "noise" resulting from nonuniformities in the dark current are discussed. Finally, the level of dark current attainable with the present state of the art is reviewed and projections for the near future are made.

I. INTRODUCTION

Since its entry into the family of semiconductor devices in 1971, the silicon charge-coupled device (CCD) has been investigated extensively. This stems from the basic simplicity of the device and the many possible applications (some unique to the CCD itself) for this device. One application in particular, that of imaging, has received considerable attention as a result of the unique advantages of the CCD as an imager.

The operation of the charge-coupled device is dynamic and involves the formation of potential energy wells for the minority carriers, the intentional and controlled introduction of minority carriers into these wells, and their transfer to other potential wells, as dictated by the signal-processing requirements. The "dark current" that has been frequently mentioned[1-5] is the attempt of the device to achieve an equilibrium condition by generating minority carriers to fill the potential wells. That is, a filled well represents thermal equilibrium and, if the well is not completely filled, a dark current results which eventually fills the well. Obviously, if the dark current is very appreciable, the integration time of an imager is limited. Likewise, the storage time in CCD memories is restricted.

Fortunately, the properties of silicon, together with the advanced state of development of silicon device processing technology, permit the realization of dark current levels low enough for many CCD applications. On the other hand, operation of both low-light-level imagers and low-level-signal processors without device cooling places very stringent demands on the allowable dark current level. That is, in the CCD imager mode of operation, the imager first integrates for a period of time to collect carriers generated by the scene focused on the imager; then the collected carriers are shifted out. Any nonuniformity in the dark current results in fixed-pattern "noise." In the case of signal-processing applications, the clocks usually operate continuously and the nonuniformity in dark current does not present as great a problem. However, the magnitude of the current must be low enough so as not to degrade the dynamic range because of shot noise. These considerations have focused attention on the need for achieving very low dark currents in order to realize large dynamic range, long storage time, and minimal noise, in particular fixed-pattern "noise." This paper examines the important considerations involved in minimizing the dark current in charge-coupled devices and applies to both surface-channel and buried-channel structures.

Section II discusses the different sources of dark current in silicon CCDs, their relative importance, and the relevant parameters to consider in minimizing the dark current. The characterization of the material and processing and the types of monitoring devices useful for this purpose are reviewed in Section III, while Section IV discusses an often overlooked factor in

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MOS device processing, namely plastic deformation. Section V calls attention to the undesirable consequences of nonuniformities in dark current. In the final section, the present state of the art for attaining low dark currents is examined, and projections for the near future made.

II. SOURCES OF DARK CURRENT

The dark current which continuously supplies undesired minority carriers has six possible sources:

(1) Generation of carriers via generation-recombination centers in the depletion region.[6,7]

(2) Generation of carriers via surface states at the $Si\text{-}SiO_2$ interface.[6,7]

(3) Avalanching at the channel-stop boundary.[8]

(4) Diffusion of minority carriers out of the neutral region of the bulk.[6,7]

(5) Processing errors (metal precipitates, oxide pinholes, photolithographic defects, defective material or junctions, etc.).

(6) Tunneling between bands.

Source (6) is negligible and can be disregarded. Source (5) is notorious in that it frequently manifests itself as localized dark-current "spikes" or "hot spots," and its cause is often difficult to isolate. The localized variations are particularly harmful, as they contribute fixed-pattern "noise" which is discussed in Section V. Unless the device operating temperature exceeds ≅80°C, source (4) is not important. Whether or not avalanching at the channel-stop boundary (source 3) is present depends on the channel-stop doping concentration and profile, the gate-oxide thickness, and the applied voltage between the transfer electrode and the substrate during CCD operation.

How the avalanching can occur can be better understood by referring to Figure 1(a) which shows the boundary between the region where charge transfer occurs (under the gate oxide) and the channel-stop region. The transfer electrode is shown overlying both regions. The channel-stop region (P+) extends under the gate oxide a few microns because of the lateral diffusion. If the surface potential in the channel-stop region beneath the gate electrode exceeds the breakdown voltage of the material during CCD operation, there will be avalanching and a resulting dark current. The breakdown surface potential decreases with increasing doping concentration. On the other hand, the applied gate voltage necessary to achieve the breakdown surface potential increases with

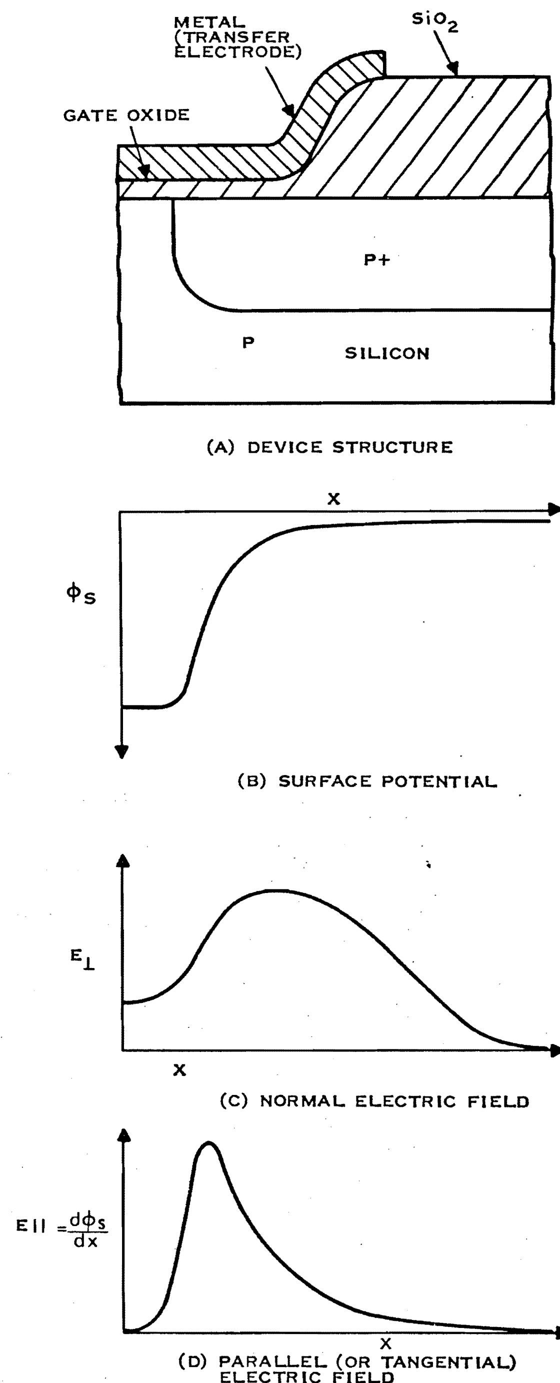


Figure 1. Electric Fields at the Edge of the Channel-Stop Region

increasing doping concentration. Of interest then is the maximum allowable gate-to-substrate voltage, V_{max}, versus doping concentration which is

$$V_{max} = \phi_{SA} + \sqrt{2\phi_{SA} V_o} \tag{1}$$

$$V_o = \frac{K_s \epsilon_o q N}{C_o^2} \tag{2}$$

where

K_s = dielectric constant of the semiconductor

N = doping concentration

C_o = insulator capacitance per unit area

ϕ_{SA} = breakdown surface potential.

In Figure 2, V_{max} is plotted as a function of doping concentration for an oxide thickness of 1200 Å. The avalanche breakdown voltage for a one-sided step junction is used to approximate the breakdown surface potential in Equation 1.[6] As shown in Figure 2, for N $\lesssim 3 \times 10^{17}$ cm^{-3}, gate-to-substrate voltages as high as 30 to 35 volts may be used in CCD operation. For N $> 3 \times 10^{17}$ cm^{-3}, V_{max} drops off because the tunneling mechanism dominates the breakdown-voltage characteristic.

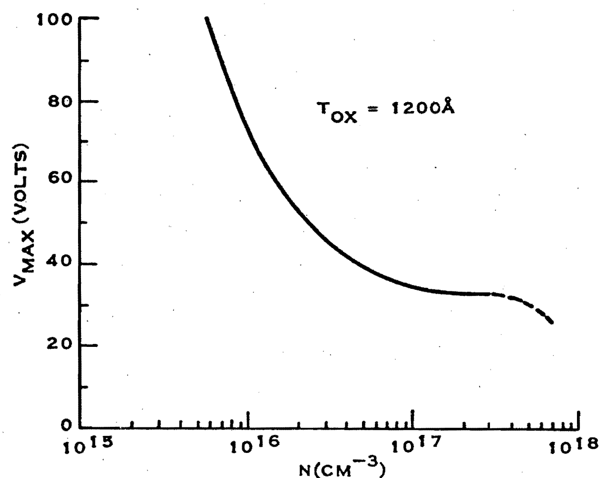


Figure 2. V_{max} as a Function of Doping Concentration, N, for 1200 Å Gate-Oxide Thickness

The foregoing discussion treated the case where avalanching occurs when the magnitude of the surface potential exceeds the breakdown voltage of the material at the edge of the channel-stop region. In this case, the perpendicular component of the electric field [Figure 1(c)] at the surface exceeds the value necessary for avalanching. In addition, one must be concerned with the slope of the surface potential parallel to the surface at the edge of the channel-stop region, as shown in Figure 1(d). This slope results in a tangential electric field (parallel to the surface) whose peak value at the edge of the channel-stop region depends on the doping profile at the edge of the channel-stop region, the oxide thickness, and applied voltage.

Calculations of the surface potential and peak tangential electric field can be performed for a given set of conditions to ascertain if the tangential electric field approaches the critical electrical field that results in breakdown. These calculations involve the numerical solution of Poisson's equation at the edge of the channel-stop region. As an example, calculations for a junction depth of 1.5 microns, a Gaussian channel-stop diffusion profile, and an applied voltage of 20 volts indicate peak tangential electric fields of 6×10^4, 1.0×10^5, and 1.3×10^5 volts/cm for surface doping concentrations of 2×10^{16}, 2×10^{17}, and 2×10^{18} cm^{-3}, respectively. These fields can be compared with the critical fields of 4×10^5, 7×10^5, and 10^6 volts/cm, respectively, which are obtained using the one-sided step-junction approximation.[6] This indicates that the tangential field should pose no problems for the above set of conditions and has been verified experimentally. It should be noted that these calculated tangential fields are less than those obtained by Amelio.[8] However, in this case, because of the assumption of an abrupt doping profile, higher peak tangential fields were obtained.

Thus, of the six possible sources of dark current, carrier generation in the depletion region (Source 1) and carrier generation via surface states at the silicon dioxide-silicon interface (Source 2) are the dominant sources. The dark current, J_D, can then be written as:[7]

$$J_D = \frac{q n_i W}{2\tau} + \frac{q n_i s_o}{2} \tag{3}$$

where

n_i = intrinsic carrier concentration

W = depletion region width

τ = bulk lifetime

s_o = surface recombination velocity when the surface is depleted.

The surface states within energy kT/q of the middle of the bandgap are most important in generating minority carriers so that[7]

$$s_o \cong N_{ss} \pi kT \sigma V_{th}, \qquad (4)$$

where

N_{ss} = the number of surface states per cm^2 per eV

T = temperature (°K)

σ = capture cross-section for electrons or holes, whichever is smaller

V_{th} = thermal velocity of the electrons.

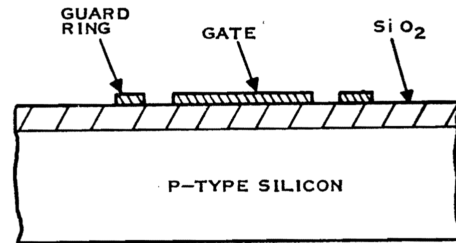
The intrinsic concentration, n_i, varies with temperature as $e^{-Eg/kT}$ where Eg is the bandgap and is 1.12 eV at room temperature. As a result, the dark current possesses a strong temperature dependence and decreases by a factor of 2 for every 10°C drop in temperature. Obviously, the dark current can be minimized by sufficient cooling of the CCD. However, many applications exist in which cooling is impractical.

As seen in Equation 3, J_D depends on the material and processing through the parameters W, τ and s_o. The depletion width is set by the substrate resistivity and the applied gate-to-substrate voltage. The bulk lifetime is dependent on substrate resistivity and processing, while the surface recombination velocity is controlled by crystal orientation and processing. The 1-0-0 orientation is preferred, as it is well known that this orientation yields the lowest fast-surface-state density.[9]

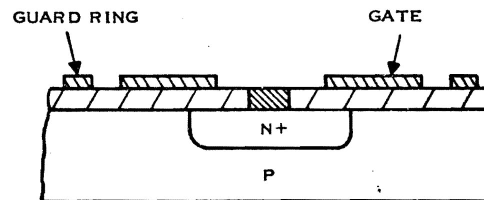
The lowest possible dark current can be realized by choosing only material with good bulk lifetime, and by processing the material carefully to preserve τ and minimize s_o. To this end, it is necessary to characterize the charge-coupled devices to determine τ and s_o. Such information aids in isolating the cause of excessive dark current and in determining the steps to be taken to correct the problem. In addition, the device performance can be linked more closely with the material and processing parameters.

III. MATERIAL AND PROCESS CHARACTERIZATION

To characterize the material and processing with respect to the dark current in a convenient and meaningful way, it is most important to have the proper monitoring devices located on the chip adjacent to the CCD structures. Two types of structures particularly suited for this purpose are the MOS capacitor and the gate-controlled diode.[10] Cross-sections of these devices are shown in Figure 3. Guard rings are included in order to ensure that the surface space charge region is terminated properly at the edge of the gate electrode. MOS capacitance-voltage, pulsed MOS capacitance storage time, and gate-controlled diode measurements on these structures permit the determination of τ and s_o as well as the fixed positive charge, Q_{ss}, at the SiO_2-Si interface, oxide thickness, bulk and channel-stop dopings, and storage time.



(A) MOS CAPACITOR



(B) GATE–CONTROLLED DIODE

Figure 3. Structures of Devices Useful for CCD Material and Process Characterization

The MOS capacitor structure is well understood and, from capacitance-voltage measurements, the procedure is relatively simple for obtaining the oxide thickness, Q_{ss}, and bulk doping.[6] Such a structure over the channel-stop doping region can be used as well for determining the channel-stop doping near the surface.

The MOS capacitor can also be used for measuring the storage time, t_F, that is the time required to fill the potential well beneath the gate electrode. The storage time is determined by applying a step voltage to an MOS capacitor. This drives the

device into a deeply depleted, nonequilibrium condition with zero charge in the inversion layer. The time required to reach equilibrium (that is, to fill the potential well) is called the storage (or filling) time. The capacitance of the device is plotted as a function of time, and the storage time determined from the time required to reach the equilibrium capacitance value. This parameter, t_F, determines the maximum integration time of a CCD imager, or the storage time of a CCD memory.

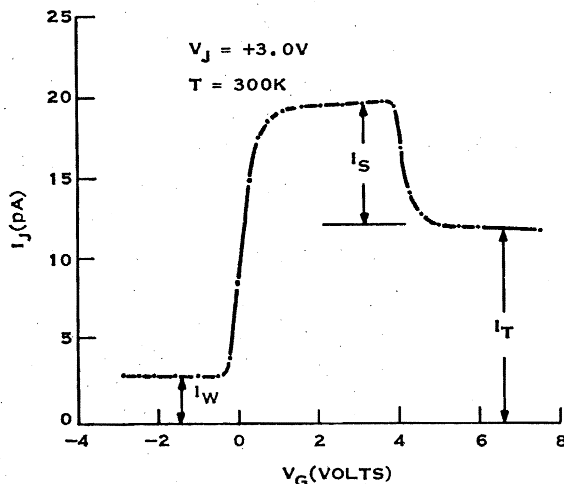


Figure 4. Reverse-Bias Junction Current Versus Gate Voltage Measured on a Gate-Controlled Diode

Analysis of the capacitance versus time curve to determine the respective contributions of the bulk and surface to the dark current is known as the Zerbst analysis[11] and is quite cumbersome and lengthy. Since the analysis uses the second time derivative of the capacitance, the data must be extremely accurate and the data reduction must be done very carefully. A more desirable structure for separating bulk and surface contributions to the dark current is the gate-controlled diode (Figure 3).[10] A simple measurement of reverse-bias current, as a function of gate voltage, yields the desired information. An example of data from such measurement is shown in Figure 4. The reverse-bias junction voltage is held constant while the gate voltage is varied. In this example, the substrate is p-type. For negative gate voltages, the surface beneath the gate is accumulated, and the measured reverse-bias junction current, I_w, originates by carrier generation in the junction depletion region. The bulk lifetime beneath the diffused junction, τ_D, may then be determined, using

$$I_w = \frac{qn_i W A_J}{2\tau_D} \quad (5)$$

where A_J is the area of the junction. The depletion width is a function of the bulk doping and junction voltage and can easily be determined since the bulk doping is known from the capacitance-voltage measurements on the MOS capacitor monitoring device.

As can be seen in Figure 4, when the gate voltage is increased above the flatband voltage (−1 V), the junction current rises. This is because the surface beneath the gate is now depleted, and additional current is generated in this depletion region as well as by the fast surface states beneath the gate at the SiO_2 interface. If the gate voltage is increased further, a point is reached at which the surface becomes inverted. At this point, the junction current decreases abruptly because the surface states are filled with trapped carriers when the surface is inverted and are no longer capable of generating current. This decrease in current, I_s, represents the fast-surface-state contribution to the total junction current and can be expressed as

$$I_s = \frac{qn_i \, s_o \, A_G}{2} \quad (6)$$

where A_G is the area of the gate. With this expression, the surface-recombination velocity can be easily determined.

When the gate voltage is sufficient to invert the surface, the junction current originates from both the depletion region beneath the diffused junction and the depletion region beneath the gate. Then the total current is given as

$$I_T = \frac{qn_i W A_D}{2\tau_D} + \frac{qn_i W A_G}{2\tau_G} \quad (7)$$

where τ_G is the bulk lifetime in the region beneath the gate. (The lifetime beneath the diffused junction and the lifetime beneath the gate are not necessarily the same and may not exhibit the same spatial variation on the slice.[12]) The first term in Equation 7 is just the measured junction current when the surface beneath the gate is accumulated (negative gate voltage) so that the lifetime τ_G may be easily determined.

The analysis outlined above for the gate-controlled diode can be applied to the experimental results shown in Figure 4. The values determined from the experimental curve are s_o = 5 cm/sec, τ_D = 52 microseconds, and τ_G = 30 microseconds. Thus, a simple measurement of junction current versus gate voltage on the gate-controlled diode structure allows one to easily obtain the bulk and surface contributions to the dark current. In addition, the lifetime and surface-recombination velocity parameters are easily determined, providing important information for characterizing the material and processing.

IV. EFFECT OF PLASTIC DEFORMATION ON DARK CURRENT

One factor in MOS processing that is frequently overlooked is dislocation generation by plastic deformation of the slice during the high-temperature (>950°C) furnace process steps. If the slice insertion and withdrawal rates are not kept below a certain level, the thermal shock caused by nonuniform rapid heating and cooling of the slice will cause plastic deformation. The resulting dislocations are usually generated most heavily toward the edge of the slice. An example of such dislocations generated by plastic deformation is shown in Figure 5. These dislocations were revealed using the Secco etch[13] on the back surface of the slice. Note the strong increase in dislocation density in going from the center of the slice to the edge. The dark current was mapped on a processed slice having plastic deformation and is shown in Figure 6 as a function of radius measured from the center of the slice.

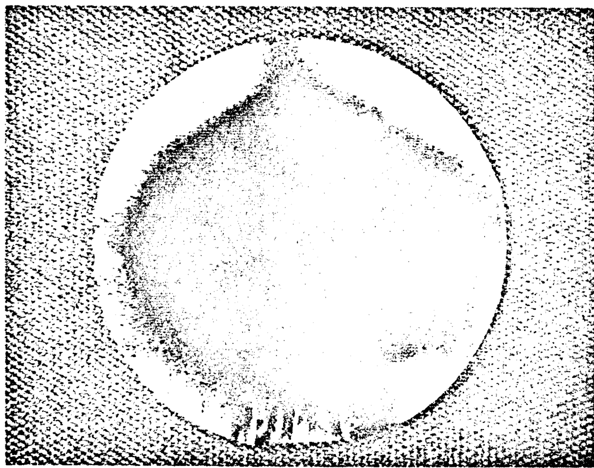


Figure 5. Secco-Etched Slice Showing Dislocations (Light Areas) Generated by Plastic Deformation

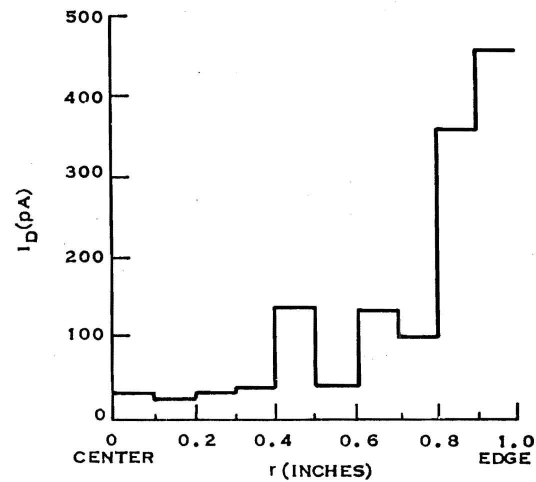


Figure 6. Variation of Dark Current from the Center to the Edge of the Slice

It is well known that the presence of such dislocations as described above increases the dark current (decreases the lifetime) by an amount depending on the material and processing history. In addition, because of the spatial variation of the dislocations, the dark current varies more widely across the slice. This contributes to the fixed-pattern "noise" of a CCD imager, which restricts the integration time and dynamic range.

The effect of plastic deformation on MOS integrated circuit performance has been studied in detail.[14] It is possible to modify the process with no loss in circuit performance so that dislocation generation is minimal. The major process modification consists of using sufficiently low slice insertion and withdrawal rates at the high-temperature furnace process steps. In this case, the measured dark current is lower and does not increase with radius.[14] This approach is desirable for obtaining the lowest possible dark current and minimizing its spatial variation.

V. SPATIAL VARIATIONS IN DARK CURRENT

In Section II and in the preceding section, processing errors and plastic deformation were cited as the major contributors to localized variations in dark current. To fully appreciate the extent to which this

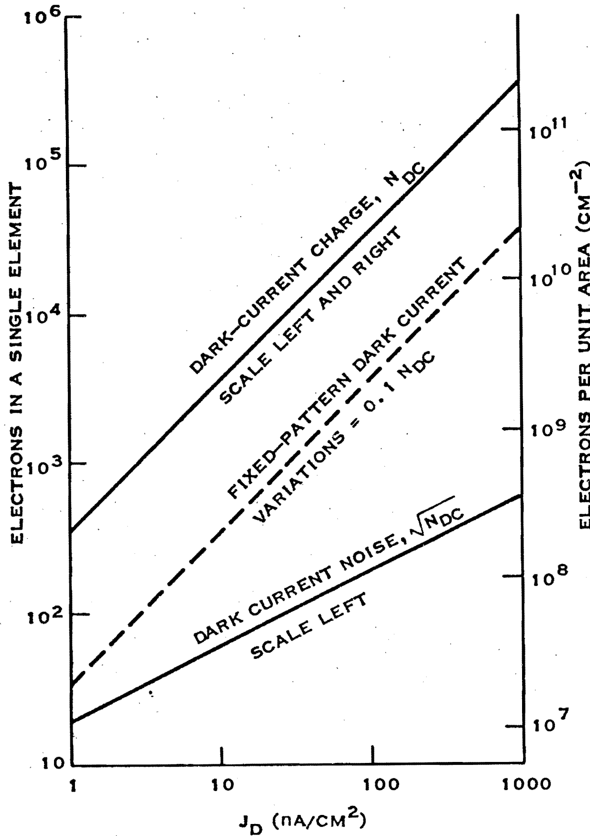


Figure 7. Dark-Current Charge as a Function of Dark-Current Density

variation of the dark current increases the noise, consider Figure 7. The graph shows the charge generated by dark current in an integration time, T_{int}, of 1/30 sec as a function of dark current per unit area. The substrate voltage is assumed to be sufficiently small so that dark current is generated only under the integrating electrodes. The electrode size is taken to be

$$0.3 \times 0.9 \text{ mil}^2 = 1.7 \times 10^{-6}\text{cm}^2$$

The dark current charge, N_{DC}, is given by

$$N_{DC} = 348 \; J_D(\text{nA/cm}^2)\left(\frac{T_{int}}{33 \text{ ms}}\right)\left(\frac{A}{1.7 \times 10^{-6}\text{cm}^2}\right)$$

A perfectly uniform dark current of 20 nanoamperes/cm² results in shot noise of only 84 electrons, whereas the fixed-pattern noise due to dark-current variations of ±5 percent corresponds to 800 electrons. Clearly, the fixed-pattern noise places severe requirements on dark-current uniformity.

VI. STATE OF THE ART AND FUTURE PROJECTIONS FOR MINIMIZING DARK CURRENT (OR MAXIMIZING STORAGE TIME)

To understand more clearly the present state of the art and the difficulties that must be overcome if lower dark currents are to be achieved without the added difficulties associated with device cooling, consider Figures 8 and 9. In Figure 8, the dark current per unit area at room temperature caused by carrier generation via surface states is plotted as a function of surface-recombination velocity using Equation 6. The dark current per unit area at room temperature caused

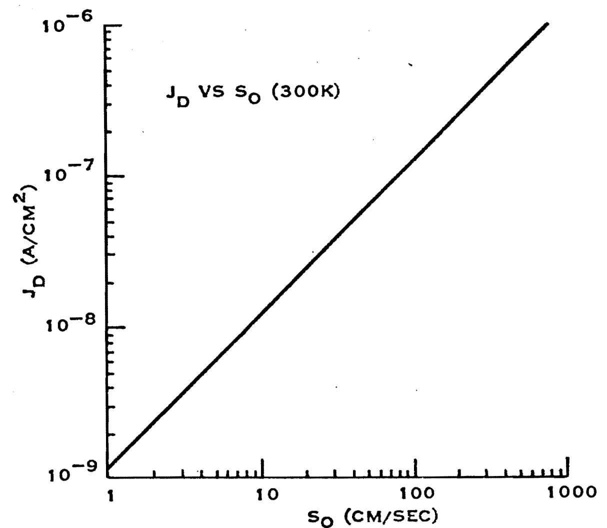


Figure 8. Dark Current as a Function of Surface-Recombination Velocity, Assuming No Bulk Generation

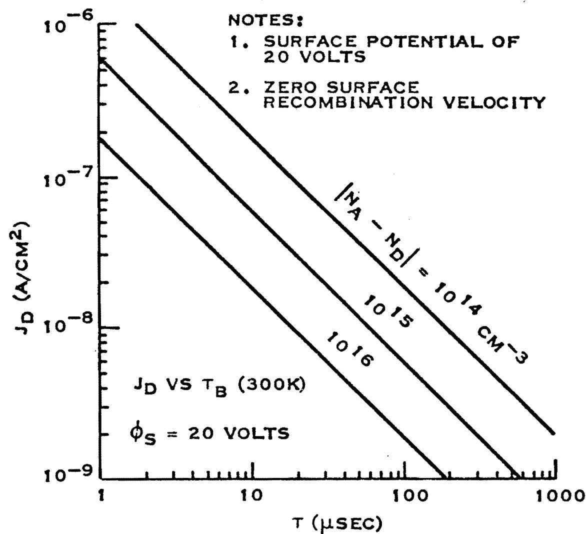


Figure 9. Leakage Current as a Function of Bulk Lifetime

by carrier generation in the depletion region is plotted in Figure 9 as a function of bulk lifetime for various bulk doping concentrations using the expression given by Equation 5. The depletion width is calculated using a value of surface-potential of 20 volts. The available literature indicates that, at present, the semiconductor industry is capable of achieving fairly consistently surface-recombination velocities of 1 to 3 cm/second and post-processing bulk lifetimes in the neighborhood of 100 microseconds. This corresponds to a total dark current of 10 to 20 nanoamperes/cm².

A value of s_0 of 1 to 3 cm/second results in a current of only 1 to 3 nanoamperes/cm², whereas a bulk lifetime value of 100 μs contributes 10 nanoamperes/cm² to the dark current (assuming the bulk concentration to lie in the mid 10^{14} cm^{-3} range). The lower limit on dark current is thus set by the maximum obtainable post-processing bulk lifetime. If dark current is to be reduced further, effort must be concentrated on achieving longer post-processing bulk lifetimes. It is true that a lower dark current can be obtained by increasing the bulk doping concentration. However, in many cases of interest, both analysis and experimental results on CCDs have indicated the need for more lightly doped material (10^{14} to 10^{15} cm^{-3}). Clearly, a longer lifetime is required.

Single-crystal silicon with much longer lifetime can be obtained quite readily; however, as soon as this material is subjected to the high temperatures required in processing, the lifetime is always degraded to 10 to 100 microseconds. This appears to be an industry-wide problem and is not completely understood at present. Part of the degradation has been traced to contamination of the silicon during processing with lifetime-killing impurities such as gold. Varying degrees of success have been achieved by using a phosphorus-gettering step in the processing. Lifetimes as long as 200 to 500 microseconds have been reported on N-type, 10-ohm-cm float-zone silicon that has been phosphorus gettered.[11] If the lifetime can be extended to ≅ 500 microseconds, dark current levels as low as 2 to 4 nanoamperes/cm² can be realized for bulk dopings in the 10^{14} to 10^{15} cm^{-3} range. Until a complete understanding of the degradation problem is attained and a way is found to preserve bulk lifetime during processing, it appears that in the near future one cannot expect to attain dark-current levels lower than 1 to 10 nanoamperes/cm² at room temperature. Even at this level, the achievement of a uniform current over large areas will be a difficult task. If uniform dark currents lower than 1 to 10 nanoamperes/cm² are required, cooling of the device will be mandatory.

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REFERENCES

1. D. F. Barbe, *Report of NRL Progress*, pp. 1-11, March 1972.
2. M.F. Tompsett, *J. Vac. Sci. Technology* 9, 1166 (1972).
3. D.D. Buss, D.R. Collins, W.H. Bailey, and C.R. Reeves, *IEEE J. Solid-State Circuits* SC-8, 138 (1973).
4. G.F. Amelio, W.J. Bertram, Jr., and M.F. Tompsett, *IEEE Trans. Elec. Devices* ED-18, 986 (1971).
5. C.H. Sequin et al., *IEEE Trans. Elec. Devices* ED-20, 244 (1973).
6. S.M. Sze, *Physics of Semiconductor Devices*, Wiley-Interscience, New York, 1969.
7. A.S. Grove, *Physics and Technology of Semiconductor Devices* John Wiley and Sons, Inc., New York, 1967.
8. G.F. Amelio, *Bell System Technical Journal* 51, 705 (1972).
9. P.V. Gray and D.M. Brown, *Appl. Phys. Letters* 8, 31 (1966).
10. A.S. Grove and D.J. Fitzgerald, *Solid-State Electronics*, 9, 783 (1966).
11. D.K. Schroder and J. Guldberg, *Solid-State Electronics*, 14, 1285 (1971).
12. A.F. Tasch, Jr. (to be published).
13. F. Secco d'Aragona, Jr., *J. Electrochem. Soc.* 119, 948 (1972).
14. A.F. Tasch, Jr., D.D. Buss, H.R. Huff, T.E. Hartman, and V.R. Porter in *Proc. of the Second International Symposium on Silicon Materials Science and Technology*, Electro-Chemical Society, May (1973).

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