POLYSILICON-ALUMINUM GATE CCD

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ABSTRACT. The performance of experimental two-phase charge-coupled shift registers constructed using polysilicon gates overlapped by aluminum gates is described. Shift registers with 64, 128, and 500 stages have been built and operated with clock frequencies up to 20 MHz. The effect upon transfer efficiency of various structural and materials parameters has been investigated including substrate orientation, resistivity, and conductivity type; channel width and channel length; and method of channel confinement. Operation of the devices with and without fat zero has been studied as well as operation in the complete charge-transfer mode and the bias charge, or bucket-brigade mode.

I. INTRODUCTION

This paper describes the construction and performance of charge-coupled devices in the form of polysilicon gates overlapped by aluminum that have been proposed and developed at RCA Laboratories. Although such charge-coupling structures can be used effectively for both surface-channel and buried-channel CCD's our discussion here will be limited specifically to our work on two-phase surface-channel CCD's.

The sealed-channel polysilicon-aluminum structures described are the most compact structures that can be fabricated with more or less conventional layout rules. The self-aligning-gate construction of these devices allows fabrication of charge-coupled structures with gate separation comparable to the thickness of the channel oxides, as well as having the channel oxide always covered by one of the metallizations. The important advantage of the silicon-gate process is that it also provides a very simple method for the construction of two-phase CCD's. The two-phase CCD's described in this paper employ two thicknesses of channel oxide for the formation of the asymmetrical potential wells needed for the unidirectional flow of signal.

II. CONSTRUCTION OF TWO-PHASE CHARGE-COUPLED DEVICES

A. DIRECTIONALITY OF SIGNAL FLOW

The charge-coupled devices initially described by Boyle and Smith (ref. 1) require three or more phase clocks to obtain the directionality of the signal flow. However, for most applications higher packing density and better performance may be achieved with two-phase charge-coupled structures. The asymmetrical potential wells or barriers in the surface potential, needed to provide the directionality of the information flow for the two-phase operation, can be achieved by incorporating one of the following features into the CCD structure:

(1) Two thicknesses of the channel oxide,
(2) dc offset voltage between two adjacent gates powered by the same phase voltage,
(3) two levels of fixed charge in the channel oxide, or
(4) ion-implanted barriers.

The first three of the above can be conveniently implemented by self-aligned, closely-spaced structures in the form of polysilicon gates overlapped by aluminum gates (ref. 2-5). In this section we will describe specifically the construction of two-phase CCD's with two different thicknesses of channel oxide for polysilicon and aluminum gates that were used as the test

devices in the experimental part of this study. However, in view of this self-aligning characteristic of this structure and the available two-layer metallization, basically the same construction can be used to implement two-phase CCD's employing a dc offset voltage between the adjacent polysilicon and aluminum gates powered by the same phase-voltage pulse train. The externally introduced dc offset voltage, however, can also be replaced by a difference in fixed charge in the channel oxide between the polysilicon and the aluminum gate.

B. FABRICATION OF POLYSILICON-ALUMINUM GATE CCD'S.

1. Basic Process. The basic fabrication procedure for the polysilicon-aluminum two-phase CCD is illustrated in Fig. 1. The process is essentially the same as standard silicon-gate processing currently in use by many MOS IC manufacturers. After source/drain diffusions and the definition of some type of channel confinement structure [Fig. 1(a)], the channel oxide is grown and polysilicon is deposited and defined [Fig. 1(b)]. Then, as shown in Fig. 1(c), a thermal oxide is grown over the polysilicon. This provides the insulation for the polysilicon gates and simultaneously grows a thicker gate oxide in the gaps between the polysilicon gates. Finally, as shown in Fig. 1(d), contact openings are made to the diffusions and polysilicon, and aluminum gates are defined.

Note that the gap between adjacent polysilicon and aluminum gates is determined by the thickness of the oxide covering the polysilicon gates [i.e., $\sim$ 2000Å]. Another advantage of this structure is the self-aligning feature of the aluminum gates over the polysilicon gates. Alignment is required only to ensure that the aluminum overlaps the polysilicon on both sides. This also provides a structure that has no exposed channel oxide and is therefore free of any stability problems resulting from the accumulation of ionic charge on such exposed oxides to which single-level-metal structures are susceptible.

2. Process Variations. We have constructed and studied the operation of a variety of p-channel as well as n-channel two-phase CCD's made on substrates with low and high resistivities. Initial test devices were made using n-type substrates with 1.0 ohm-cm resistivity and (111) orientation. Subsequently, most of our p-channel and

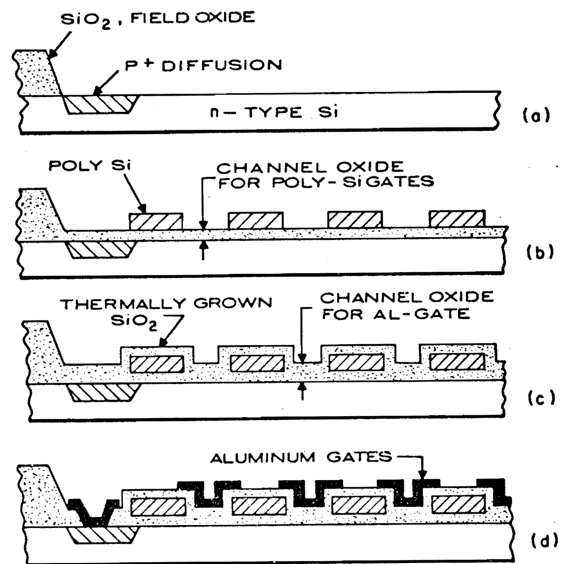


Fig. 1. Construction of two-phase charge-coupled devices in the form of polysilicon gates overlapped by aluminum gates.

n-channel CCD's were made on substrates with (100) orientation. This included devices made using n-type substrates with resistivities of 1.0 and 10 ohm-cm, as well as p-type substrates with resistivities of 1.0 and 30 ohm-cm.

For devices made on 1.0 ohm-cm, n-type substrates the channel confinement (defining the width of the channel) was obtained by means of thick-field oxide (12,000 Å SiO_2) for the substrates with (100) orientation. A diffusion guard ring, however, was used to obtain the channel confinement for the p-channel devices made on the 10 ohm-cm substrates.

The n-channel CCD's were made using thick-field oxide for channel confinement in the case of 1.0 ohm-cm substrates and polysilicon field-shield for the case of 1.0 and 30 ohm-cm substrates.

We have used boron deposition, following the standard thick-oxide PMOS process, for the fabrication of p^+-diffusions for the p-channel CCD's. The n^+ diffusions for the

n-channel devices as well as the n^+-diffusion guard rings for the high-resistivity p-channel CCD's were prepared using phosphoroxychloride as the diffusion source.

C. DESIGN OF TWO-PHASE CCD's

Typical surface potential profiles for two thicknesses of channel oxide are shown in Fig. 2 (b) and (c) for the complete charge transfer (C-C) mode and the bucket brigade (B-B) mode, respectively. (For more complete discussion of the C-C and B-B modes of operation of two-phase CCD's, see ref. 5). Since the charge-transfer losses for the C-C mode are typically ten times smaller than for the B-B mode, an important design consideration is to avoid the B-B mode. Thus, the oxide thickness and the substrate doping for the structure shown in Figure 2(a) were chosen so that the C-C mode of operation can be assured over a wide range of substrate bias voltages.

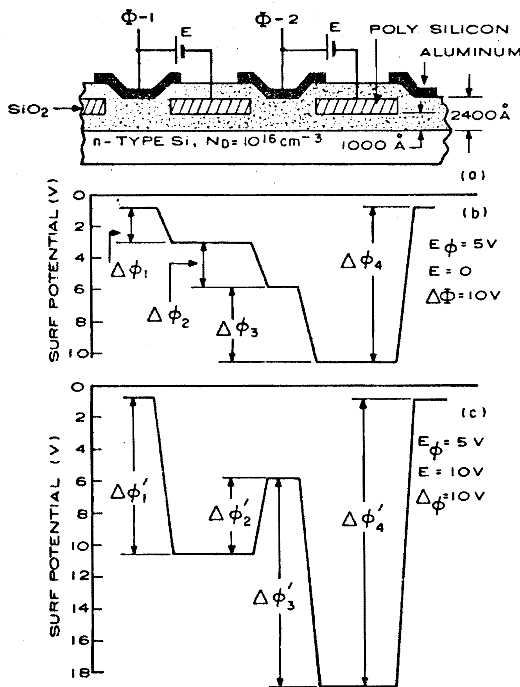


Fig. 2. (a) Surface potential profiles for 2-phase charge-coupled structure; (b) operating in the C-C mode; and (c) in the B-B mode.

The required thickness of channel oxide under the aluminum gates as a function of substrate doping is illustrated in Figure 3 for a two-phase p-channel CCD with a 1000 Å thick oxide under the polysilicon gates. The solid curve was calculated to give 5 V signal wells when the device is operated with 5 V substrate bias and 10 V clock pulses. The upper dotted line in Figure 3 shows the maximum substrate bias voltage for the C-C mode of operation for an oxide thickness under the aluminum gate indicated by the solid line at that doping level. The lower dotted line indicates the minimum substrate bias to insure a -1 volt surface potential under the aluminum gates.

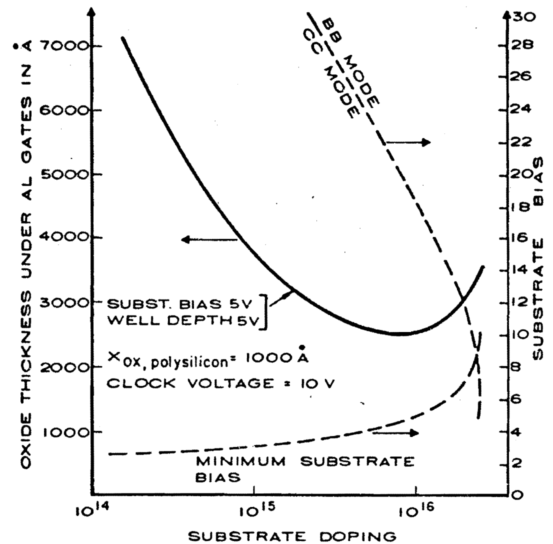


Fig. 3: Solid Curve: Gate oxide required to achieve 5 V wells as a function of substrate doping (assuming 5 V substrate bias, 10 V clocks and 1000 Å thick oxide under polysilicon.) Top dotted curve: Maximum substrate bias (right ordinate) which results in C-C mode for the aluminum gate oxide thickness determined by the solid curve. Bottom dotted curve: Minimum substrate bias to provide -1 V surface potential under aluminum gates.

D. DESCRIPTION OF EXPERIMENTAL DEVICES

1. 64- and 128-Stage Shift Registers. A cross-sectional view along the channel of the 64- and 128-stage registers is illustrated in Fig 4(a) on the next page. As is shown, the input structure consists of a source diffusion S-1 and input gates G-1 and G-2. Although not shown in the Figure, separate electrical access has been provided to the polysilicon and aluminum electrodes of each phase, i.e., ϕ-1 (poly) ϕ-1 (Al), ϕ-2 (poly), and ϕ-2 (Al). The output can be detected as the current flow out of the drain diffusion D-1 or as a voltage change resulting from the charge signal introduced on the floating diffusion that, in turn, controls the gate voltage of a 3-mil wide output MOS device with a source S-2 and drain D-2. The electrodes G-3 and G-4 are externally available for controlling the signal flow in and out of the floating diffusion. The center-to-center spacing of 1.2 mils/stage represents the minimum that can be achieved with 0.2-mil spaces between lines and 0.1-mil overlap between the polysilicon and aluminum gates.

The channel confinement (channel stops) along the width of the CCD structures was obtained by a variety of methods including 12,000 Å field oxide, diffused n^+-channel stops, and polysilicon field-shield. Most of the devices studied were 5.0 mils wide. However, to study the effect of the width of the CCD channel on the performance of the registers, special CCD arrays were made having the same layout as is shown in Figs. 4a, but with 0.5- and 1.0-mil-wide channels.

2. 500-Stage Shift Registers. The 500-stage device was constructed with a 0.8-mil per stage dimension incorporating a 0.3-mil (in the direction of charge transfer) polysilicon gate with a 0.1-mil gap. The alignment tolerance between aluminum and polysilicon remained at 0.1-mil. This reduces the overall device length to about 400 mils resulting in a chip size of 100 x 455 mils. The design incorporates two parallel channels, one 1.0-mil wide, the other 5.0 mils wide, driven by the same phase electrodes, but with separate inputs and outputs. The electrode arrangement of the 500-stage register is similar to the 128-stage device. The electrical input stage consists of a source diffusion S-1 and two control gates G-1 and G-2. As with the 128-stage device, the output can be detected as the current flow out of the drain diffusion D-1. On the 500-stage device, the floating-diffusion voltage is the input to an inverter in which both transistors have a 0.4-mil channel length and 3-mils width. (See Fig. 4 b).

IV. PERFORMANCE OF EXPERIMENTAL DEVICES

A. TRANSFER LOSSES FOR p-CHANNEL 64 AND 128 STAGE REGISTERS

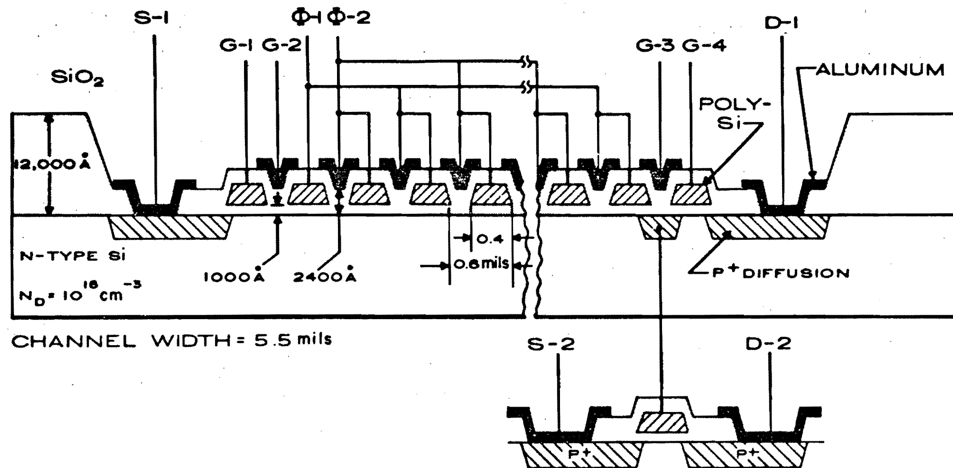
1. Devices with (111) Substrates. The measurements of the transfer loss as function of clock frequency are shown in Fig 5 for devices fabricated on 1.0 ohm-cm n-type substrates with (111) orientation. The dotted curve B represents the best fit to the data of the calculated fast-interface-state trapping losses according to the following equation:

$$\varepsilon_S = \frac{(kT/q)N_{SS}}{N_{SIG}} \ln(1 + \frac{f}{f_o}). \qquad (1)$$

From this data we estimate fast-interface-state densities of $N_{SS} = 1.2 \times 10^{11} (cm^2\text{-}eV)^{-1}$ for the devices made on silicon with (111) orientation. According to these measurements, the transfer loss with fat zero also decreases as a function of clock frequency for both the C-C and the B-B modes. The dotted curve on the right represents the calculated transfer loss for free-charge transfer for a 0.4-mil-long storage gates assuming self-induced drift dominates transfer for the first 99%, with a characteristic time t_o = 0.75 nsec, and thermal diffusion dominates thereafter with a time constant of 64 nsec appropriate for L = 0.4 mil (ref. 6).

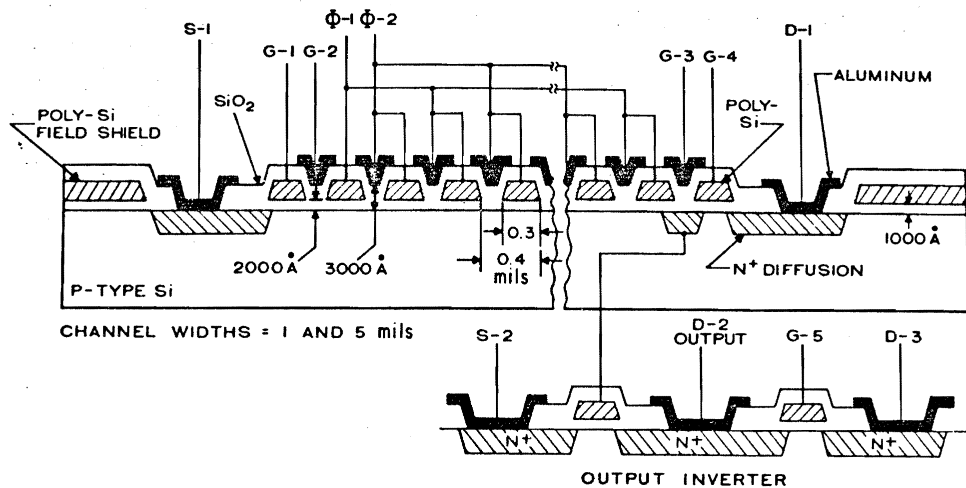
2. Devices with (100) Substrates. The variation of transfer loss curves for the C-C mode for registers made on 1.0 ohm-cm n-type substrates with (100) orientation are shown in Fig. 6. Here again, the best fit to data points for curve C indicates N_{SS} = $2.9 \times 10^{10} (cm^2\text{-}eV)^{-1}$. Curve A shows the transfer loss for a 0.5-mil-wide register and 50% fat zero. Curve B shows the transfer loss for a 0.5-mil register with 30% fat zero.

The transfer loss for registers made on (100) substrates operated in the B-B mode with two different barrier heights is shown in Fig. 7. The most interesting result of



128 STAGE SHIFT REGISTER

(a)



500 STAGE SHIFT REGISTER

(b)

Fig. 4. Cross-sectional views of registers along the channel for 64- and 128-stage registers, and 500-stage registers.

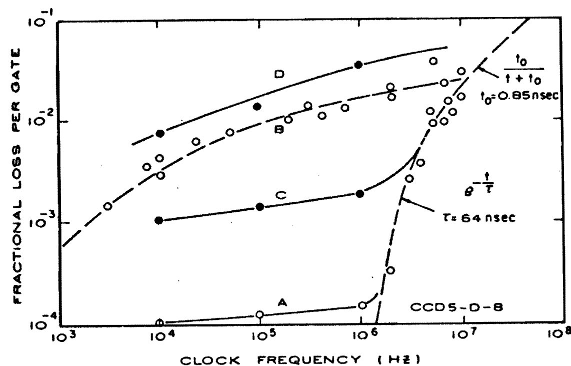


Fig. 5. Fractional loss per transfer vs. clock frequency for 128-stage registers made on (111) substrates.
Curve A: C-C mode (E_ϕ = 20 V, E = -5V, $\Delta\phi$ = 10 V) with 10% fat zero;
Curve B: C-C mode with no fat zero.
Curve C: B-B mode (E_ϕ = 10 V, E = 5 V, $\Delta\phi$ = 10 V) with 10% fat zero;
Curve D: B-B mode with no fat zero.

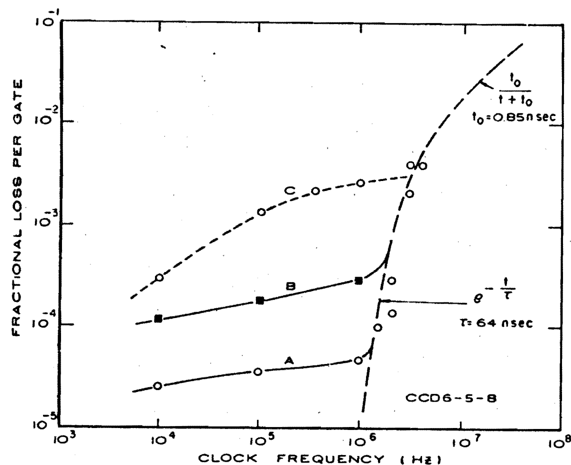


Fig. 6. Fractional loss vs. clock frequency for 64-stage registers made on (100) substrates operating in C-C mode (E_ϕ = 5 V, E = 0 V, $\Delta\phi$ = 10 V). Curve A: 5.0-mil-wide with 50% fat zero; Curve B: 0.5-mil-wide with 30% fat zero; Curve C: 5.0-mil-wide with no fat zero.

these measurements is that the registers operated in the B-B mode with relatively small barriers have transfer losses that decreased as the clock frequency was reduced.

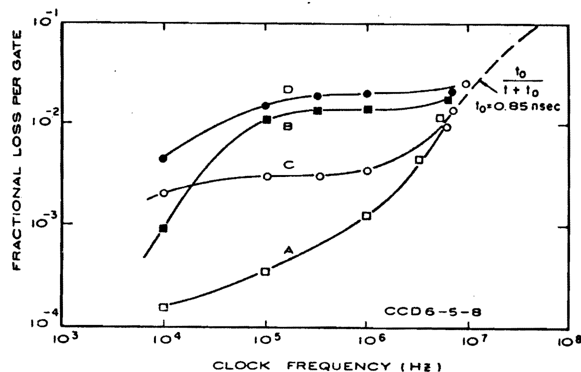


Fig. 7. Fractional loss vs. clock frequency for 5-mil-wide 64-stage registers made on (100) substrate operating in the B-B modes. Curve A: E_ϕ = 5V, E = 5 V, $\Delta\phi$ = 10 V, and 10% fat zero; Curve B: Same as A, but with no fat zero; Curve C: E_ϕ = 5 V, E = 10 V, $\Delta\phi$ = 10 V, and 10% fat zero; Curve D: Same as C but with no fat zero.

Figure 8 shows how the transfer loss as a function of fat zero varies with the channel width for C-C mode of operation. The curves on this figure illustrate the edge-effect that becomes more important in the case of the narrower devices.

B. TRANSFER LOSSES FOR N-CHANNEL 500-STAGE REGISTERS

The 500-stage shift-registers were fabricated on 1.0 and 30 ohm-cm p-type substrates with (100) orientation. The construction of these devices is illustrated in Figure 4(b). These devices were operated with separate d-c bias voltages provided for the polysilicon phase gates and for the aluminum phase gates. The inverter-amplifier output was found to be satisfactory for clock frequencies from 5.0 to 10 MHz. For clock frequency of 10 MHz and above the experimental data were obtained by shunting the load device (D-2 to D-3) with a 1-kohm resistor. The measured transfered loss for 1.0- and 5.0-mil-wide 500-stage two-phase

registers made on 1.0- and 30-ohm-cm n-type substrates with (100) orientation are shown in Fig. 9 for operation with about 30% fat zero.

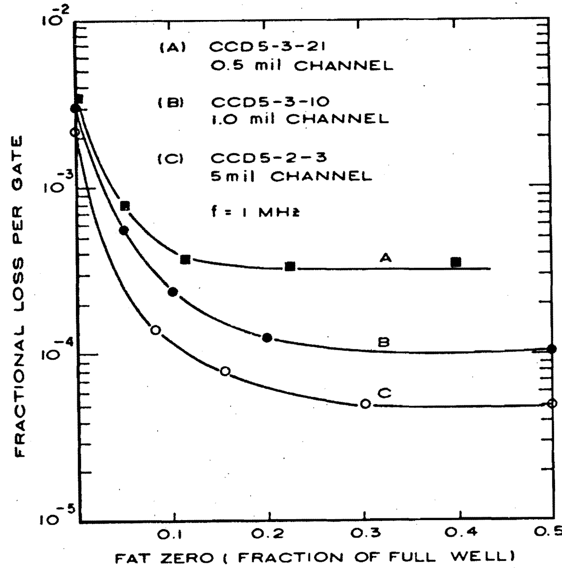


Fig. 8. Fractional loss per transfer at 1 MHz vs. amount of fat zero for 0.5-, 1.0, and 5.0-mil-wide registers made on (100) substrates are shown as Curves A, B, and C, respectively.

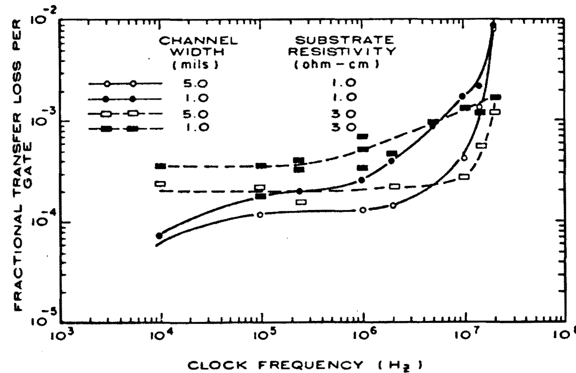


Fig. 9. Transfer loss vs. clock frequency for 500-stage registers operating with 30% fat zero.

C. EFFECT OF SUBSTRATE ON PERFORMANCE

The curves of transfer loss versus clock frequency for 64 and 128 stage registers made on low and high resistivity n-type as well as p-type substrates are shown in Fig. 10. The data shown in this figure was obtained for no fat zero operation in order to clearly measure the intrinsic speed limitations (due to free-charge transfer) of these devices. The transfer loss data for operation with 20% fat zero for various two-phase registers operating with 1.0-MHz clock frequency is summarized in Table I. These low-frequency performance limitations for fat zero operation can be explained by edge effects and other losses connected with charge trapping by the fast-interface states.

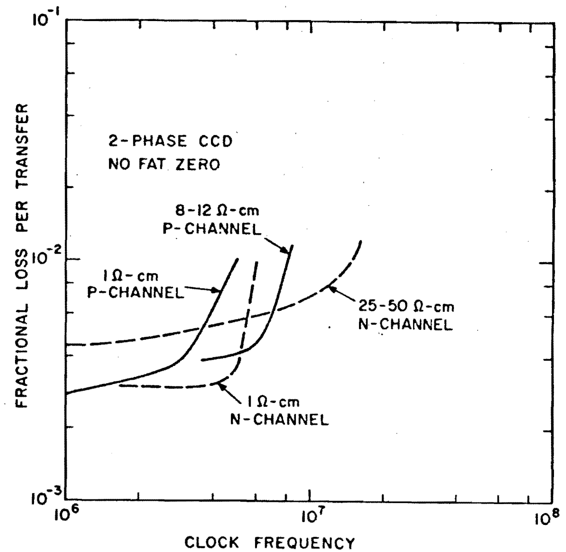


Fig. 10. Transfer loss vs. frequency for devices operating without fat zero. The frequency at which the loss per transfer increases abruptly indicates the onset of significant incomplete free-charge transfer.

IV. DISCUSSION OF EXPERIMENTAL RESULTS

A. FAST INTERFACE STATE LOSSES

For operation with no fat zero the transfer losses occurring in the flat

TABLE I
Performance of the Tested Two-Phase CCD Registers at 1.0 MHz Clock Frequency

No.	Substrate			Channel Confinement	Channel Width [mils(μm)]	Transfer Loss Per Gate With 20-30% Fat Zero	N_{ss} (cm^2-eV^{-1})
	Type	Resistivity (ohm-cm)	Orientation				
1	n	1.0	111	Thick Oxide	5.0(125)	1.2×10^{-4}	1.2×10^{11}
2	n	1.0	100	Thick Oxide	5.0(125)	5.0×10^{-5}	2.9×10^{10}
3	n	1.0	100	Thick Oxide	1.0(25)	1.0×10^{-4}	-
4	n	1.0	100	Thick Oxide	0.5(12.5)	3.5×10^{-4}	-
5	n	8-12	100	Diffusion Guard Ring	5.0(125)	2.0×10^{-4}	-
6	p	1.0	100	Thick Oxide	5.0(125)	$< 10^{-4}$	-
7	p	1.0	100	Thick Oxide	0.5(12.5)	2.0×10^{-4}	-
8	p	25-50	100	Poly-Si Field Shield	5.0(125)	3.0×10^{-4}	-
9	p	25-50	100	Poly-Si Field Shield	0.5(12.5)	1.2×10^{-3}	-
10	p	1.0	100	Poly-Si Field Shield	5.0(125)	1.2×10^{-4}	-
11	p	1.0	100	Poly-Si Field Shield	1.0(25)	2.5×10^{-4}	-
12	p	30	100	Poly-Si Field Shield	5.0(125)	1.8×10^{-4}	-
13	p	30	100	Poly-Si Field Shield	1.0(25)	4.0×10^{-4}	-

DEVICES 1 to 9 were 64- and 128-stage registers with 0.4 mil (10 μm) polysilicon gates and 0.2 mil (5 μm) aluminum gates.
DEVICES 10 to 13 were 500-stage registers with 0.3 mil (7.5 μm) polysilicon gates and 0.1 mil (2.5 μm) aluminum gates.

portion of the loss vs. frequency curve were found to be consistent with our model for interface state losses as expressed by Eq. (1) (ref. 4,7,8). A more complete expression for the carriers lost into fast state per unit area including the effect of a large fat zero is:

$$N_{LOSS} = \left(\frac{n_s/n_{s,o}}{n_s/n_{s,o} + 1} \right) \frac{kT}{q} N_{SS} \ln \left(1 + \frac{f}{k_1 n_{s,o}} \right) \quad (2)$$

where n_s is the signal charge density and $n_{s,o}$ is the fat zero charge density. Eq.(2) is similar to Eq. (1) except that the prefactor indicates that the losses approach zero as the signal level goes to zero.

However, experimental measurements indicate that losses at intermediate frequencies when operating with fat zero are higher than that predicted by Eq. (2). This is because the model has assumed a potential well with steep walls so that the background charge, or fat zero, is spread uniformly in all regions and is present at every point where signal charge, when present, resides. However, actual potential wells have sloping sides and there is a region along the edges that does not benefit from the presence of fat zero. In this edge region the conduction band charge is very low and the quasi-Fermi level tends toward the center of the gap. In this case, the simplified theory predicts a fractional loss per transfer given by

$$\varepsilon_{s,\ parallel} = 3.9 \times 10^{-4} \left(\frac{1}{W_{mils}} \right) \times \left(\frac{N_{SS}}{10^{10}} \right) \left(\frac{10^{15}}{N_D} \right)^{1/2} \quad (3)$$

for clock frequency of 1.0 MHz, signal of 4V, and oxide thickness of 1000Å; where W_{mils} is the channel width in mils and N_D is the substrate doping. (For details see ref. 9).

The curves in Figure 11 showing the expected edge-effect loss according to Eq. (3) are in general agreement with the indicated experimental points.

The charge trapping by the fast interface states due to the edge-effect appear to offer the only reasonable model for the relatively flat regions of the transfer loss curves in Figures 5,6, and 7.

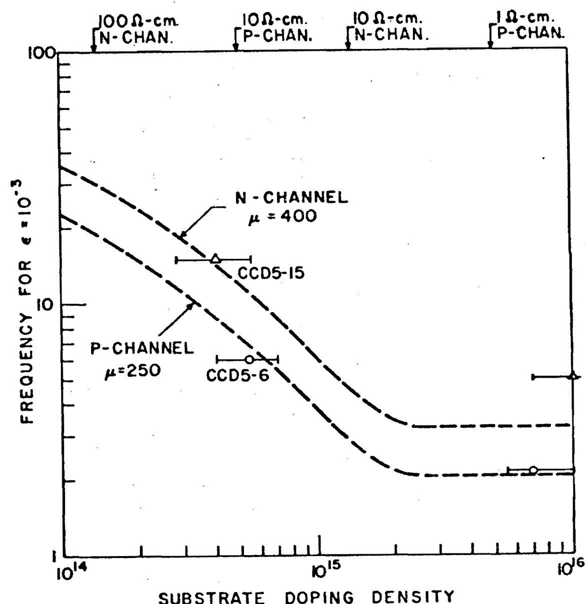


Fig. 11. Frequency at $\varepsilon = 10^{-3}$ vs. substrate doping for both n- and p-channel devices with 0.4 mil gate lengths.

B. FREE CHARGE LOSSES

The knee of the transfer loss curves above which the transfer losses increase sharply with clock frequency are in good agreement with the expected response due to the drift-aiding fringing fields (ref. 6, 10) especially for the devices made on low-doped substrates. The calculated frequencies at which the transfer for the 128 stage register due to the drift-aiding fringing field, or thermal diffusion in the limiting case for highly doped substrates, correspond to $\varepsilon = 10^{-3}$ are shown as dotted lines in Figure 12. (For more details see ref. 9). Also shown in Fig. 12 are experimentally observed points for four different 128-stage shift registers with differing resistivities and channel types. Aside from the 10^{16} doped n-channel, the agreement with the free charge transfer predictions is excellent.

The free-charge transfer analysis (ref 6) predicts a L^{-2} frequency dependence for devices with low substrate resistivities in which case charge transfer is initially dominated by a highly nonlinear self-induced drift and then by thermal diffusion for very low charge density. However, for operation with a large fat zero, the effective charge

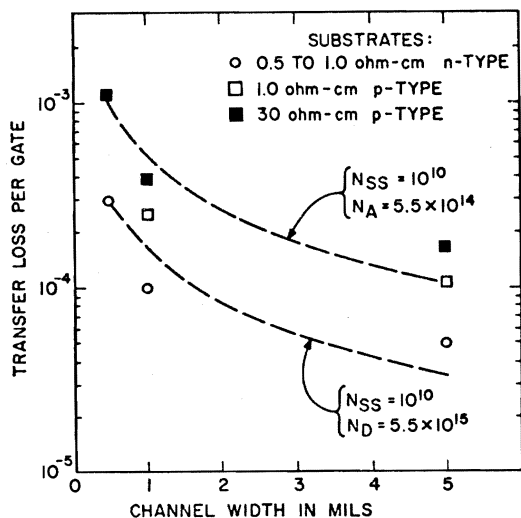


Fig. 12. Calculated and experimentally measured edge effect losses.

transfer loss must be computed as the difference between the charge left behind the signal packet as compared to the charge left behind the fat zero packet. In this case the nonlinear charge transfer due to the self-induced drift results in a L^{-4} frequency dependence which is again very good agreement with our data for the n-channel devices made on 1.0 ohm-cm substrates. The polysilicon gate length for the 64- and 128-stage devices is 0.4 mil while the gate length for the 500-stage unit is 0.3 mil. Hence, one would expect an increase of about three times in the frequency where free charge losses become significant. This should be compared with a frequency of 5.0 MHz measured for the 1.0 ohm-cm n-channel device with 0.4 mil gates in Fig. 12 with the frequency of 15 MHz corresponding to $\varepsilon = 10^{-3}$ for the 5.0 mil wide register on 1.0 ohm-cm substrate having 0.3 mil gates in Figure 9.

V. CONCLUSIONS

The performance of the developed two-phase charge-coupled devices in the form of polysilicon gates overlapped by aluminum gates has been demonstrated by fabricating and testing 64-, 128-, and 500-stage registers. The devices studied included a variety of 0.5-, 1.0-, and 5.0-mil-wide two-phase registers with p- and n-channels made on low- and high-resistivity substrates. The method of channel confinement employed included thick-field-oxide, diffusion guard rings, and polysilicon field shield.

The best overall performance has been achieved with 5-mil-wide n-channel devices made on substrates with (100) orientation. For operation at clock frequencies of 1.0 MHz and below, the devices made on 1.0-ohm-cm substrates had a charge-transfer loss of less than 10^{-4} per transfer; and devices made on 30-ohm-cm substrates exhibited a transfer loss of 10^{-3} at clock frequencies of 20 MHz.

The experimental results were found to be consistent with the free charge transfer theory (ref. 6), predicting increased speed as the substrate doping and gate length decreases. An additional speed-performance trade-off due to rounding of the potential wells, i.e., the so-called edge effect, has been experimentally demonstrated. The edge effect loss becomes more pronounced in devices with narrower channels and in devices made with lower substrate doping. On the basis of experimental data, an edge-effect loss model was developed that predicts that the *simultaneous* achievement of speeds in excess of 15 MHz, channel widths of less than 1.0 mil and transfer efficiencies greater than 99.9% (for gate lengths of 0.4 mils) is unattainable for surface channel charge-coupled devices with interface-state densities greater than 10^{10} $(cm^2\text{-}eV)^{-1}$. Therefore, shorter gate lengths and/or lower interface-state densities are required to exceed the above performance with surface channel devices.

The fast interface state densities estimated from the experimental work for p-channel devices made on 1.0 ohm-cm substrates were 1.2×10^{11} and 2.9×10^{10} $(cm^2\text{-}eV)^{-1}$ for substrate orientations of (111) and (100), respectively.

A comparison of the complete charge-transfer mode (C - C mode) and the bias-charge or bucket-brigade mode (B - B mode of operation of the registers showed that at 1.0 MHz clock frequency the complete charge-transfer mode is greater than 10 times more efficient than the bias charge mode. At higher clock

frequencies, such as 10 MHz, the two modes of operation were found to have about the same charge-transfer efficiency. Both of these results were obtained with fat-zero operation. For operation without fat zero, the charge-trapping-like transfer losses for the B-B mode were found to be larger than for the C-C mode. This effect was clearly demonstrated in registers made on (100) substrates.

VI. ACKNOWLEDGMENTS

This work was supported by NASA Contracts 10983 and 11861, Langley Research Center, Hampton, Va. P. J. Hayes was the contract monitor. The authors are also grateful for the contributions of W. Romito who fabricated the devices, J. Sarace who provided processing assistance, and P. Levine who assisted with measurements.

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