FEASIBILITY STUDY OF PbTe AND $Pb_{0.76}Sn_{0.24}Te$ INFRARED CHARGE COUPLED IMAGER*

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ABSTRACT

The feasibility of using MIS structures of PbTe and $Pb_{0.76}Sn_{0.24}Te$ for infrared charge coupled imaging in the 3 to 5 and the 8 to 14 microns regions have been examined. First, the storage capacity, dark current and storage time of the MIS capacitors of these two semiconductors were calculated at T=85°K based on the MOS theory developed for Si. P-type semiconductors of doping density $5\times10^{16}cm^{-3}$ and a minority carrier lifetime of 10^{-7} sec were used. Four types of insulators were considered : SiO_2, Al_2O_3, Ta_2O_5 and TiO_2. TiO_2 was found to be better suited for CCI applications because of its high dielectric constant. Based on these MIS results, the feasibility of IRCCI for 300°K scene was examined. The background photon flux was used to produce a 50% fat zero which determined the exposure time. It was assumed that 10% of the storage time can be used for CCI operation. At a clock frequency of 2 MHz and without considering the transfer inefficiency,20,000 transfers can be made in PbTe CCI within this usable storage time. However, only 20 transfers can be made in $Pb_{0.76}Sn_{0.24}Te$ CCI. The 300°K background current was calculated and was found to be approximately 3000 times larger than the signal current for a 0.1°K temperature resolution for both semiconductors. Preliminary experimental studies of PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS capacitors were also made using Hg drops as metal contacts on MIS samples consisting of Al_2O_3 or SiO_2 layers e-gun evaporated on thin film semiconductors. C-V measurements indicated that accumulation, depletion and inversion layers existed at the interface and can be controlled by the gate voltage in a manner qualitatively similar to that of Si MOS. However, measured and calculated C-V characteristics have not been in close agreement.

It is concluded that PbTe IRCCI is feasible. For $Pb_{0.76}Sn_{0.24}Te$, CCI is questionable unless improvement in minority carrier life time to a value significantly above 10^{-7} sec can be achieved.

I. INTRODUCTION

Recent progress[1-5] has confirmed the expectation that Si charge coupled devices[6] will be one of the most important visible imagers. This paper deals with the question if CCD can also be developed for infrared imaging. Several approaches have been mentioned[7] for developing the Infrared Charge Coupled Imager (IRCCI). Some of them are hybrid circuits in which the infrared detectors are combined with Si CCD. This study considered the monolithic approach in which a metal-insulator-semiconductor array of narrow gap semiconductor is used both as the sensor and the transfer device. Its structure is similar to the Si CCD except that a semiconductor of smaller energy gap is used instead of Si. This paper will present the preliminary results of the feasibility study of using MIS structures of two 4-6 narrow gap semiconductors as IRCCI. The semiconductors considered are PbTe for a 3 to 5 microns imager and $Pb_{0.76}Sn_{0.24}Te$ for an 8 to 14 microns imager , both operated at a temperature of T=85°K. Since the MIS properties of these semiconductors have not been studied before, this feasibility study did not examine the aspects of CCI which require information on the interface states, such as the problems of transfer inefficiencies and noises, etc. Instead, the feasibility study was based on the theoretical calculation of the MIS properties of single PbTe and $Pb_{0.76}Sn_{0.24}Te$ capacitors. Experimental studies of these MIS have been started, however, to examine the validity of the theoretical calculations. Their preliminary results will be reported in this paper also.

In Section II, the storage capacity, dark current and storage time of both the PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS were calculated based on the MOS theory developed for Si. Four insulators, SiO_2, Al_2O_3, Ta_2O_5 and TiO_2 were considered. It was found that TiO_2 is better than the others because of its higher dielectric constant. Based on a sample MIS using 1000A of TiO_2, the feasibility of IRCCI for 300°K scene was examined by comparing the transfer time and the storage time for a clock frequency of 2 MHz. The background photon flux was used to produce a 50% fat zero which determined the exposure time. Both the 300°K background current and the signal current of a 0.1°K temperature resolution were calculated. In Section IV, the preliminary results of the experimental study of the PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS using Al_2O_3 and SiO_2 layers as insulators are presented. The measured C-V characteristics will be used as evidence of the existence of accumulation, depletion and inversion layers. They are also compared with the theoretical calculation to examine if the behaviors of the present PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS samples can be well described by the established MOS theory.

II. PROPERTIES OF PbTe AND $Pb_{0.76}Sn_{0.24}Te$ MIS

The basic building block of a charge coupled device is the MIS capacitor. A thorough understanding of its properties is mandatory before the feasibility of the IRCCI can be examined. In this section, the properties of the PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS relevant to the CCI operations will be presented. Specifically, the storage capacity Q_s, dark current I_d and the storage time τ_s were calculated based on the following theories. First, the MIS capacitances for the deep depletion and high frequency inversion states were calculated by the depletion approximation[9,10] which was shown to agree very closely to the exact theory if the gate voltage is considerably higher than the threshold. The storage capacity, Q_S, was calculated from the relation

$$Q_S = V_G \, (C_{HINV} - C_{DD})$$

where V_G= applied gate voltage
C_{HINV} = high frequency inversion capacitance
C_{DD} = deep depletion capacitance

Its basis is shown in Fig. 1. In (a), the normalized MIS capacitance C/C_I is presented as a function of the gate voltage, V_G, for a p type semiconductor. The CCD operation takes place between the deep depletion state and the high frequency inversion state. This region is described in a different way in (b) which presents C/C_I as a function of time. The MIS was originally biased in accumulation, then suddenly switched to deep depletion which is not stable and will be changed to inversion after a period of time, called the storage time τ_S, due to the appearance of minority carriers contributed by the dark currents.[11]

$$\tau_S = \frac{Q_S}{\sum_i I_{di}}$$

The dark currents consist of carriers generated from several sources: one from the depletion region, one from the bulk semiconductor beyond the depletion region, one from the surface generation and recombination and one from the tunneling between the bulk and the surface inversion layer. In this study, the last two components were not considered. The dark current due to the surface generation and recombination was neglected although it contributed a significant portion of dark current in the indirect gap semiconductor, Si. It is believed that in narrow gap semiconductors like PbTe and $Pb_{0.76}Sn_{0.24}Te$, the direct band transition will dominate the generation even at the surface. The dark current due to the tunneling was also neglected because at the bias voltage of interest, the depletion layer width is more than 4000 A which can be seen in Table I and II to be presented later. The tunneling current through this barrier width was much smaller compared with the other two dark currents which are given by the following relations.[11]

I_{gd} = generation within the depletion region

$$= \frac{n_i}{\tau}\sqrt{\frac{\varepsilon_s\ q\phi_s}{2N}}$$

I_{gb} = generation in the bulk semiconductor

$$= \frac{q\ n_i^2}{N\ \tau} L = \frac{q\ n_i^2}{N\ \tau}\sqrt{\mu \frac{kT}{q}\tau}$$

where n_i = intrinsic carrier con centration
τ = minority carrier life time
N = doping density
μ = mobility
L = diffusion length
ϕs = surface potential

In Table I and II, Q_S , x_{dd} , I_d , $\tau_S$of the PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS are presented at a gate voltage of ten volts. x_{dd} is the deep depletion width. Four insulators of two thicknesses, 1000 and 2000 A, were considered. The insulator types and their dielectric constants are the following:

SiO_2 , 3.9 Al_2O_3 , 8.8
Ta_2O_5, 50 TiO_2 , 75

The temperature was 85°K. p type semiconductors of doping density of $5\text{x}10^{16}$ cm^{-3}were used. For PbTe and $Pb_{0.76}Sn_{0.24}Te$, the following semiconductor properties are used.[8,12]

E_g = energy gap in ev
$= 0.181 + 4.52\text{x}10^{-4}\ T - 0.568\ X + 5.8\ X^4$

m_d = density of states effective mass
$= (1.12\ E_g)m_o$

Dielectric constant = 400
μ = mobility = $2\text{x}10^4$ $cm^2/v\text{-}sec$
τ = minority carrier life time
$= 10^{-7}$ sec

where X is the percentage of Sn content. From the Table, it can be seen that for MIS having 2000 A of SiO_2 as an insulating layer, a gate voltage of 10 volts i s not even large enough to reach inversion. In MIS having 1000 A of SiO_2 , 10 volt is not very far above the threshold. Consequently, the Q_S is only $3\text{x}10^9$ electrons/cm^2 for PbTe MIS. This is the result of a large difference in the dielectric constants of the insulator and the semiconductor. In the case of Al_2O_3, although its dielectric constant is higher at 8.8, the increase in Q_S is not dramatic. On the other hand, MIS using either Ta_2O_5 or TiO_2 as insulating layers showed definitely superior properties for CCI applications because their dielectric constants are considerably higher. In these cases, although the dark current was increased somewhat due to the increase of depletion width, the storage capacity is considerably larger which results in longer storage time. Such combination of larger Q_S and longer $\tau_S$is desirable for CCI operation. Consequently, for the feasibility study of IRCCI to be presented in the next section, a MIS capacitor having 1000 A of TiO_2 was used as the standard sample. The storage capacity is approximately $1\text{x}10^{13}$ electrons/cm^2 for both PbTe and $Pb_{0.76}Sn_{0.24}Te$ at a V_G of 10 volt. The storage time is approximately 10^{-1} sec for PbTe and 10^{-4} sec for $Pb_{0.76}Sn_{0.24}Te$.

III. FEASIBILITY OF PbTe AND $Pb_{0.76}Sn_{0.24}Te$ IRCCI

Based on these properties of a single MIS capacitor, the feasibility of PbTe and $Pb_{0.76}Sn_{0.24}Te$ IRCCI for 300°K scene were examined by comparing the transfer time with the storage time and by comparing the background and signal currents. The exposure time was selected such that the 300°K background photons will provide a 50% fat zero. Since the properties of interface states can not be theoretically predicted, the feasibility study did not examine other performances of CCI which require the knowledge of interface states, such as the transfer inefficiency and noise etc.

The IRCCI was assumed to have the following band pass characteristics. The cutoff on the longwavelength side was determined by the photoresponse threshold of the semiconductor. At 85°K, it is 5.66 microns for PbTe and 12.16 microns for $Pb_{0.76}Sn_{0.24}Te$. Infrared filters were used to provide the cutoff on the short wavelength side. Together, the bandpass was from 3.5 to 5.66 microns for PbTe and from 9 to 12.16 microns for $Pb_{0.76}Sn_{0.24}Te$. The photon flux of the 300°K background and of a 0.1°K temperature resolution were calculated from the standard black body formula. It was found that the 300°K background photon flux is much greater than the signal photon flux. In order that the backgound photons not flood the storage capacity, the exposure time must be limited. It was proposed that the 300°K background photons provide a 50% fat zero. Since the storage capacity of the standard MIS sample used in this study is $1\text{x}10^{13}$ electrons/cm^2, the required exposure time is $1.54\text{x}10^{-4}$ sec for PbTe and 9.83×10^{-6} sec for $Pb_{0.76}Sn_{0.24}Te$. Both exposure times are too short for practical applications although it probably is tolerable in the case of PbTe. For PbTe, the storage time is then 425 times longer than the exposure time. For $Pb_{0.76}Sn_{0.24}Te$, it is only six times longer.

It is further assumed that CCI operation can take place only within one tenth of the storage time. Beyond this usable fraction, the dark current will contribute too many minority carriers and smear out the signal carriers. Therefore, the usable storage time is approximately 10^{-2} sec for PbTe and only 10^{-5} sec for $Pb_{0.76}Sn_{0.24}Te$. If a clock frequency of 2 MHz is used, the transfer time per gate is 0.5×10^{-6} sec. Based on the consideration of time allowed for transfer alone, 20,000 transfers can be made within this usable storage time for PbTe. It should be noted that if transfer inefficiency is considered, the signal will deteriorate before this large number of transfers. In the case of $Pb_{0.76}Sn_{0.24}Te$, only 20 transfers can be made which is not enough for practical applications.

At the same clock frequency of 2 MHz, the current due to the 300K background is 1.6 amp/cm^2. The signal current of a 0.1°K temperature resolution of the 300°K scene is 4.8×10^{-3} amp/cm^2 for PbTe and 3.88×10^{-3} amp/cm^2 for $Pb_{0.76}Sn_{0.24}Te$. The ratio of the background current to signal current is therefore approximately 3,000 in both cases. Such a ratio, although quite high, can be handled by different signal processing schemes, such as a.c. coupling or the potentially promising recycling capability of the CCD which might be used to cancel the background.[2]

IV. EXPERIMENTAL STUDIES OF PbTe AND $Pb_{0.76}Sn_{0.24}Te$ MIS

Preliminary experimental investigations of the PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS have also been carried out. MIS capacitors were fabricated using PbTe and $Pb_{0.76}Sn_{0.24}Te$ thin films deposited on either CaF_2 and BaF_2 substrates and Al_2O_3or SiO_2 thin insulator films deposited by the e-gun method. The metal contact was provided by a Hg drop. The semiconductor films were typically 3 to 8 microns thick. They were all p-type with carrier concentrations in the high 10^{17} to low 10^{18}/cm^3 range. Based on the theoretical calculation, in order to obtain a reasonably low threshold voltage around one to two volts, the thickness of Al_2O_3 or $Si\ O_2$ layer should be less than 500A. Thin layers from 100 to 450A have been made. Probably because of the small thickness, considerable leakages were found in these layers. However, in spite of the leakage, capacitance-voltage measurements have been obtained as shown in Figures 2 and 3. Both measurements were made at room temperature using a Bootan 72A capacitance meter. The signal frequency was 1 MHz. In Figure 2, the normalized C/C_I of four gates on a PbTe MIS are shown. The insulating layer was 450A of $Si\ O_2$. The general behaviors of the C-V characteristics are similar to that of Si MOS in their early years of development. The decrease in capacitance when the gate voltage was increased from negative values toward positive values can be interpreted as evidence of the change from accumulation to depletion and then to high frequency inversion. The small peak and slight increase near and above zero gate voltage could be caused by weak inversion. A comparison was made between the measured C/C_I and a theoretical calculation using a carrier concentration of 1×10^{18}/cm^2. The calculated result is presented as a dotted line in the same figure. It can be seen that they are not in close agreement. The same large discrepancy was also found in Figure 3 which presents the C/C_I-V_G characteristics of two Hg gates on a $Pb_{0.76}Sn_{0.24}Te$ MIS capacitor. 100A of Al_2O_3 was used as the insulator. The theoretical C/C_I-V_G characteristics is also presented as a dotted line in the same figure. The lack of close agreement is clearly seen.

In spite of these discrepancies, it is believed that the MOS theory developed for Si should be valid for these semiconductors also. The lack of agreement between measurements and calculations probably is caused by the values of dielectric constants used in the calculation which may not be correct for the sample. For the 4-6 semiconductors, it is possible that their dielectric constants are not as high as 400. For the imperfect and thin insulating layers, the dielectric constants are likely higher than the bulk values of 3.9 and 8.8 for SiO_2 and Al_2O_3, respectively.

V. CONCLUSION

The feasibility of using MIS structures of narrow gap semiconductors PbTe and $Pb_{0.76}Sn_{0.24}Te$ for infrared charge coupled imaging has been studied. Because of the unusually large dielectric constants of these semiconductors, it was found that insulators of large dielectric constants such as TiO_2 and Ta_2O_5 are more suitable than SiO_2 and Al_2O_3. For an insulating layer with a large dielectric constant, adequate storage capacity can be obtained with moderately high gate voltage and an insulating layer thickness not too small. It was found that using 1000A of TiO_2, storage capacity of 1×10^{13} electrons/cm^2 can be obtained at a gate voltage of 10 volts. Assuming that the generation of minority carriers in depletion region and in the bulk semiconductor are the main contributions to the dark current, the storage time was calculated to be approximately 10^{-1} sec for PbTe and 10^{-4} sec for $Pb_{0.76}Sn_{0.24}Te$. Based on these properties, the feasibility of IRCCI using these semiconductors were examined. The exposure time was selected such that the 300°K background photons did not flood the storage capacity. They were used to provide a 50% fat zero. At a clock frequency of 2 MHz, and not considering the limitation imposed by the transfer inefficiency, 20,000 transfers can be made within the usable storage time for PbTe. On the other hand, only 20 transfers can be made in $Pb_{0.76}Sn_{0.24}Te$. It is concluded that PbTe IRCCI is feasible. For $Pb_{0.76}Sn_{0.24}Te$, IRCCI is questionable unless significant material improvements can be made to increase the minority carrier lifetime considerably above 10^{-7} sec.

Preliminary experimental studies of PbTe and $Pb_{0.76}Sn_{0.24}Te$ MIS have also been carried out to examine if MIS of these narrow gap semiconductors follow very well the standard MOS theory. Since the technology of TiO_2 has hardly been developed, e-gun evaporated Al_2O_3 or SiO_2 layers were used in the fabrication of MIS capacitors. The high frequency (1 MHz) C-V characteristics measured at room temperature behaved qualitatively like that of Si MOS indicating that the interface of these MIS showed accumulation, depletion and inversion behaviors very similar to Si MOS. However, measured and calculated C-V characteristics have not been in agreement. This lack of agreement does not imply that the MOS theory is not valid for these semiconductors. Instead, the discrepancy may be caused by the values of dielectric constants used in the calculation. It should be emphasized that the success in experimentally obtaining C-V characteristics qualitatively similar to that of Si MOS indicated that a fruitful experimental study can be carried out to develop MIS of these semiconductors and to realize their potential as IRCCI.

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TABLE I. Properties of PbTe MIS at T=85°K
and a Gate Voltage of 10 volts

Insulator	Thickness (A°)	Q_s (e/cm^2)	Xdd (μ)	Id (amp/cm^2)	τ_s (sec)
SiO_2	1000 2000*	3.07×10^{9} ---	0.422 ---	4.9×10^{-6} ---	1×10^{-4} ---
Al_2O_3	1000 2000	3.94×10^{11} 1.64×10^{10}	0.89 0.47	1.03×10^{-5} 5.5×10^{-6}	6.15×10^{-3} 4.78×10^{-4}
Ta_2O_5	1000 2000	1.14×10^{13} 4.47×10^{12}	2.28 1.78	2.64×10^{-5} 2.06×10^{-5}	6.76×10^{-2} 3.48×10^{-2}
TiO_2	1000 2000	1.62×10^{13} 8×10^{12}	2.49 2.09	2.88×10^{-5} 2.43×10^{-5}	9×10^{-2} 5.29×10^{-2}

* Gate voltage of 10 volts is below threshold of inversion.

P type PbTe, $N_A = 5 \times 10^{16}$ cm^{-3}, minority carrier lifetime = 10^{-7}sec, $\mu = 2 \times 10^{4}$ cm^2/v-sec.

TABLE II. Properties of $Pb_{0.76}Sn_{0.24}Te$ MIS at T=85°K
and a Gate Voltage of 10 volts

Insulator	Thickness (A°)	Q_s (e/cm^2)	Xdd (μ)	Id (amp/cm^2)	τ_s (sec)
SiO_2	1000 2000*	2.86×10^{10} ---	0.42 ---	6.86×10^{-3} ---	6.68×10^{-7} ---
Al_2O_3	1000 2000	5.14×10^{11} 4.87×10^{10}	0.89 0.47	1.19×10^{-2} 7.42×10^{-3}	6.92×10^{-6} 1.05×10^{-6}
Ta_2O_5	1000 2000	1.34×10^{13} 5.23×10^{12}	2.28 1.78	2.71×10^{-2} 2.16×10^{-2}	7.9×10^{-5} 3.88×10^{-5}
TiO_2	1000 2000	2×10^{13} 9.46×10^{12}	2.49 2.09	2.93×10^{-2} 2.5×10^{-2}	1.1×10^{-4} 6.05×10^{-5}

* Gate Voltage of 10 volts is below threshold of inversion.

P type $Pb_{0.76}Sn_{0.24}Te$, $N_A = 5 \times 10^{16}$cm^{-3}, minority carrier lifetime = 10^{-7} sec, $\mu = 2 \times 10^{4}$ cm^2/v-sec.

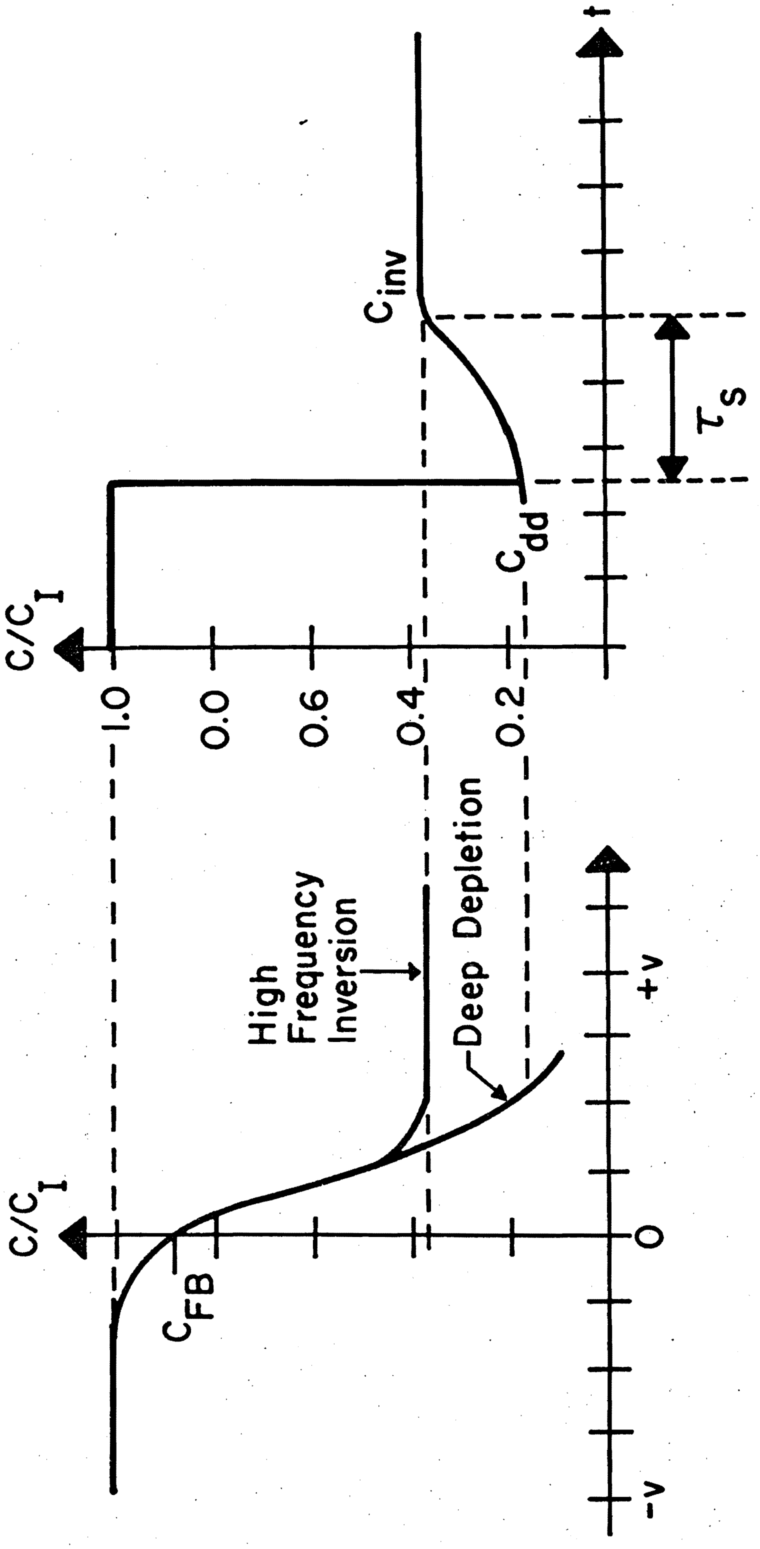

Fig. 1 C-V and C-t Charateristics of a MIS Capacitor

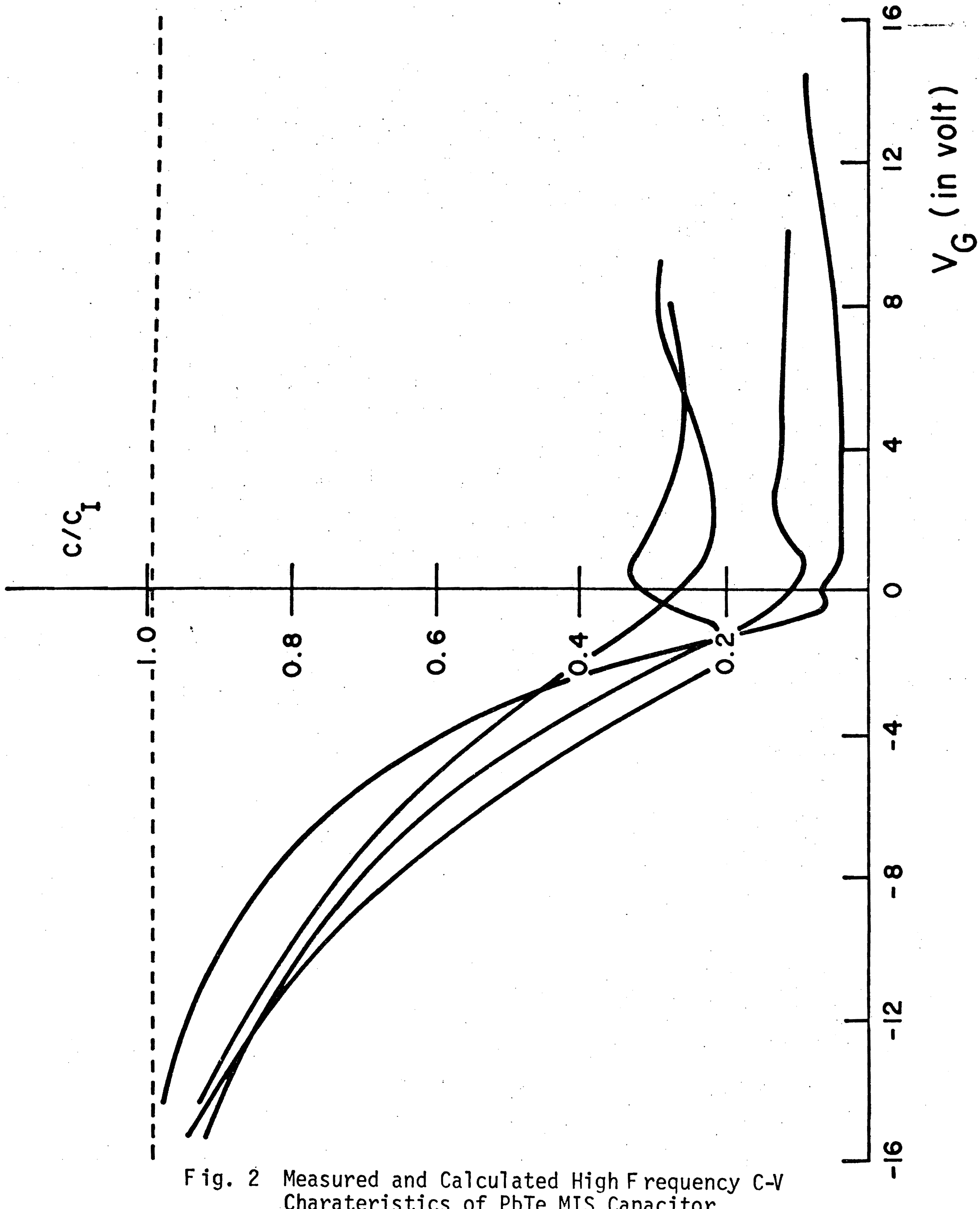

Fig. 2 Measured and Calculated High Frequency C-V Charateristics of PbTe MIS Capacitor
p type PbTe, $N_A = 1 \times 10^{18}/cm^3$
450 A SiO_2, T = 300°K

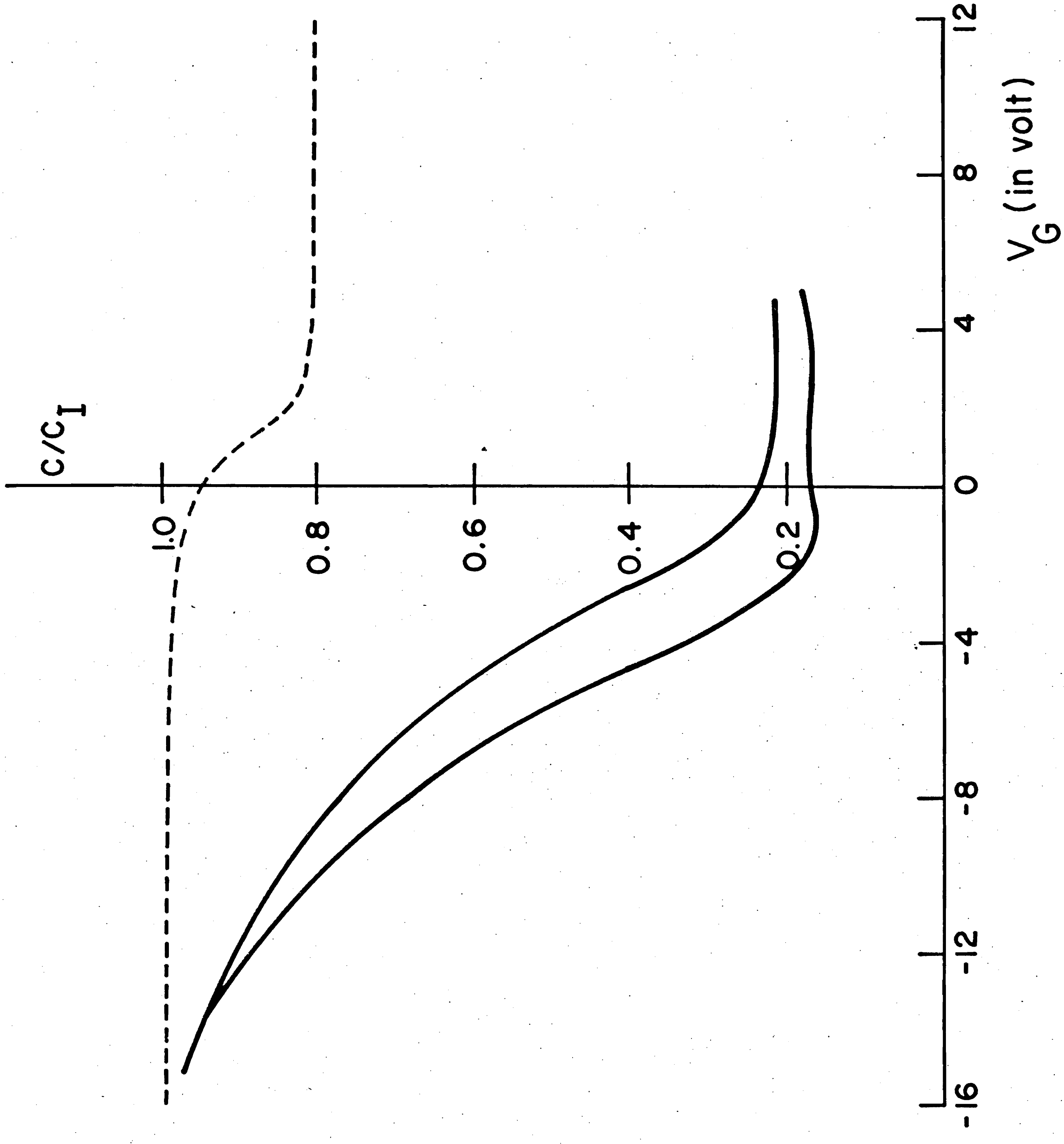

Fig. 3 Measured and Calculated High Frequency C-V Characteristics of $Pb_{0.76}Sn_{0.24}Te$ MIS Capacitor
p type $Pb_{0.76}Sn_{0.24}Te$, $N_A = 1x10^{18}$ /cm^3
100 A Al_2O_3, T = 300°K