A Flexible 14-bit Column-Parallel ADC Concept for Application in Wafer-Scale X-ray CMOS Imagers

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Contents

- Why a column parallel ADC in wafer-scale X-ray image sensors?
- Key specifications
- Converter principle
- Block diagram
- Lay-out
- Critical design aspects
- Extensions to further increase flexibility
- Conclusions

Why a column parallel ADC?

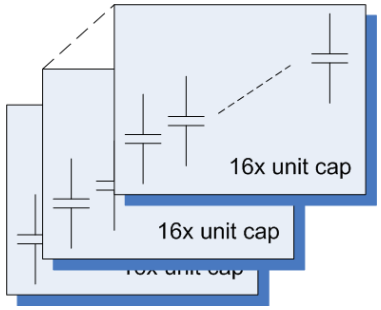
- For reasons of *performance*
  - No sensitive analog off-chip connections needed resulting in less induced crosstalk and noise
  - Parallel conversion of columns resulting in high-speed and high resolution readout of large pixel arrays
- For reasons of *costs*
  - No separate discrete ADCs and PCB area required

Key specifications

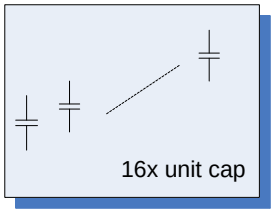
- Technology node: **0.35µm**, four metal, dual poly CMOS
- Dimensions single ADC: **67** (100) **µm** x **2800 µm**
- Conversion time: total 58 cycles with a clock period of 100ns (10MHz clock) results in a conversion time of **5.8µs**
- Conversion gain: **~110µV/DN** @ ADCref 2.8V
- Total noise: 1.6DN / **175μV_{RMS}**
- (Single) ADC current consumption **90µA** @ 3.5V

Converter principle

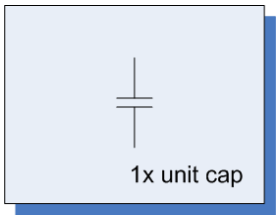
- Principle of ADC is based on a multi-slope thermometer code search methodology: this is a variant of successive approximation
- This architecture has been selected for reasons of size, speed, resolution and power consumption
- 14 bits are determined in 4 scans consisting of repetitive charge redistribution between unit capacitors



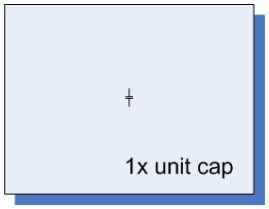
Scan 1, caps charged to Vref



Scan 2, caps charged to 0;1/16Vref;…. ;15/16Vref

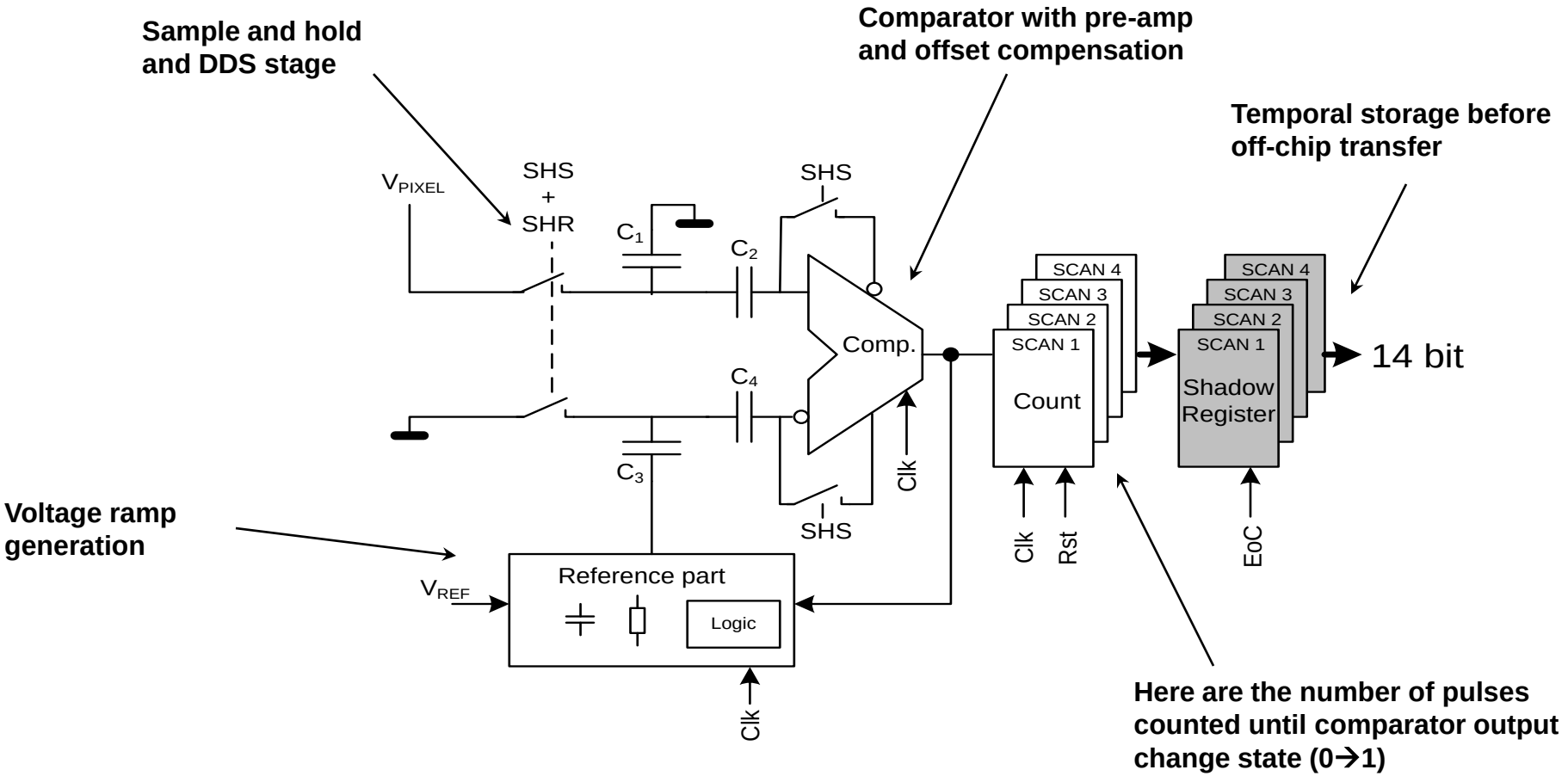


Scan 3, single cap charged to 0;1/16Vref;……. ;15/16Vref



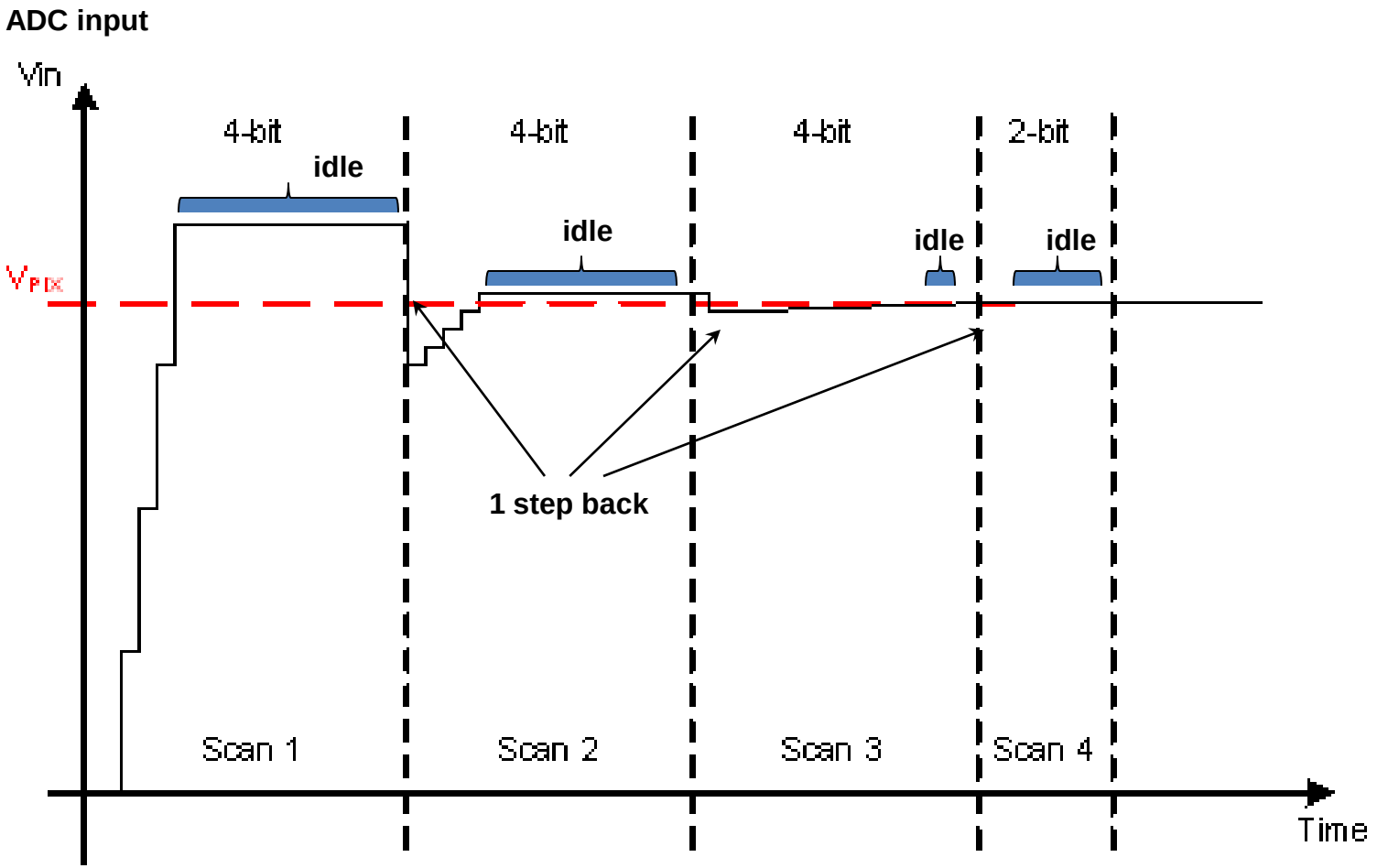
Scan 4, cap charged to 0;1/64Vref;…… ; 3/64Vref

Block diagram 14-bit col parallel ADC

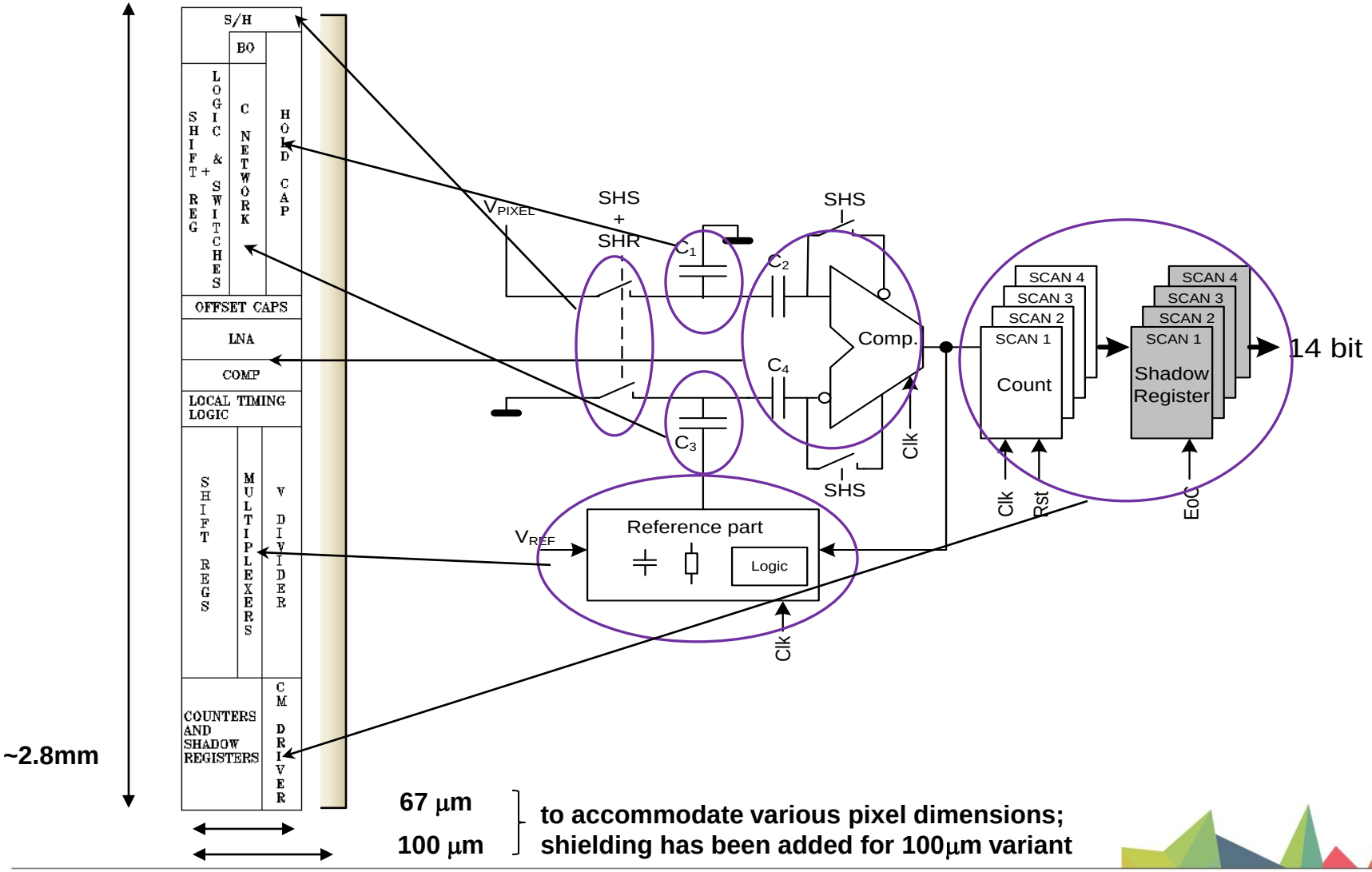


Operating principle based on (capacitor) matching: 14 bit is limit for resolution

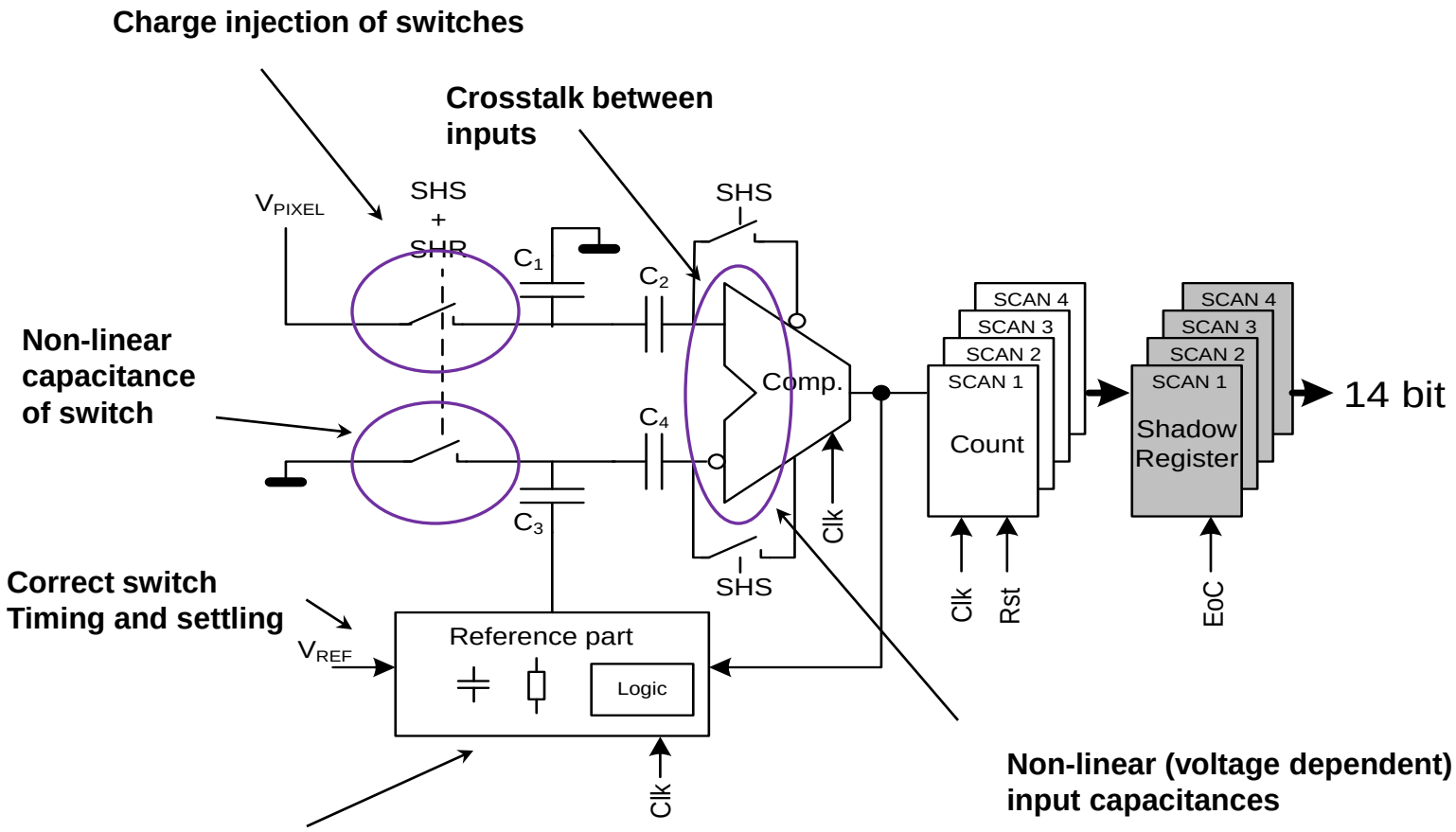
Conversion process

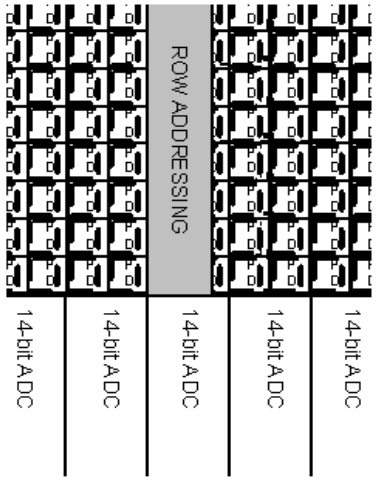


Overall dimensions and block ratios

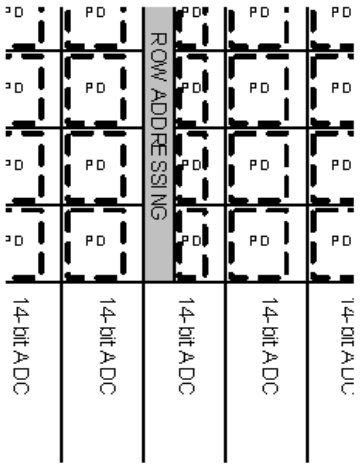


Critical design aspects

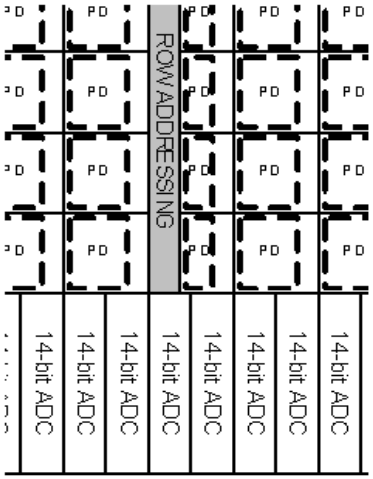




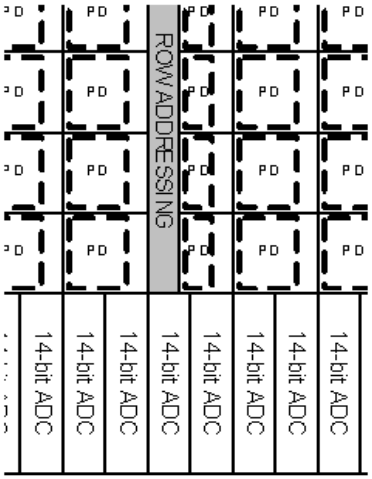
50µm pixel en 100µm ADC



100µm pixel en 100µm ADC



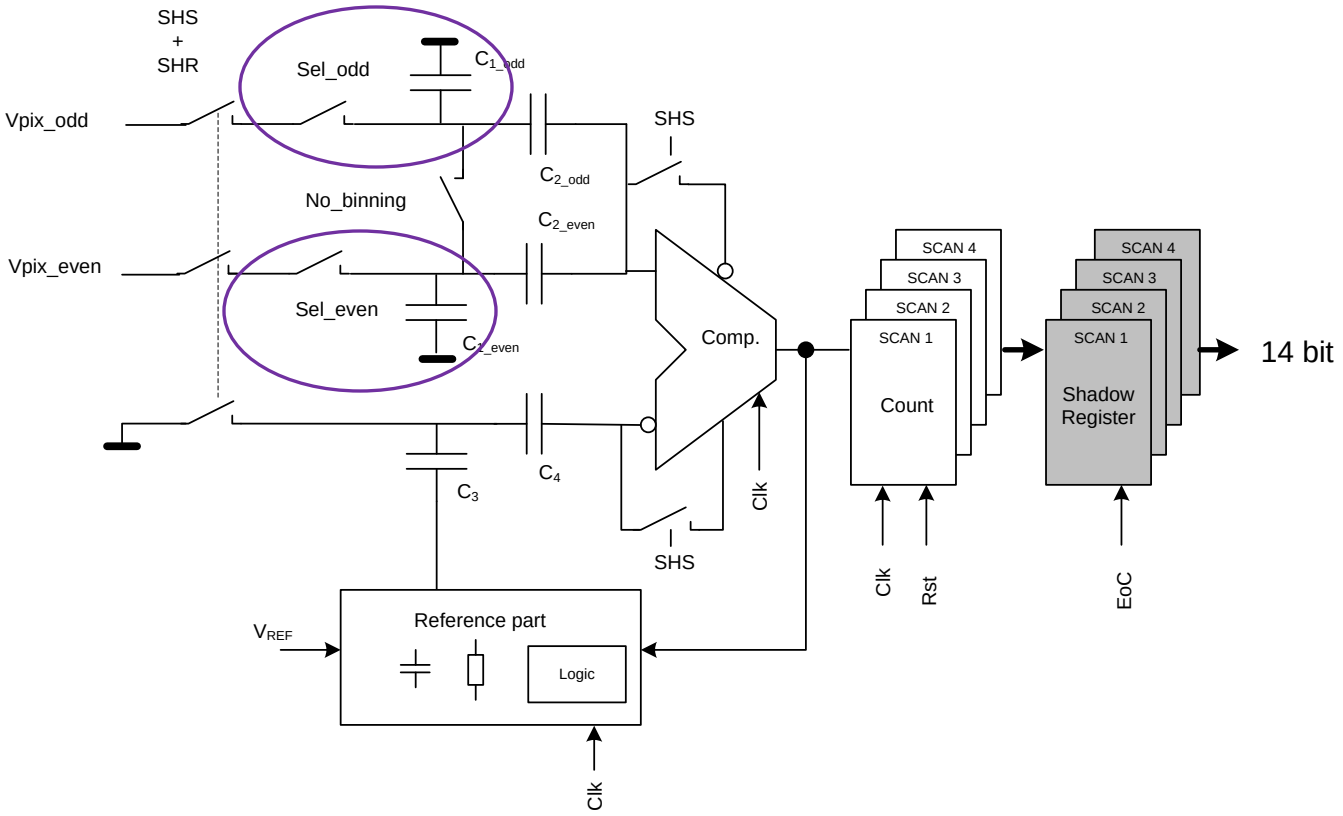
134µm pixel en 67µm ADC



200µm pixel en 100µm ADC

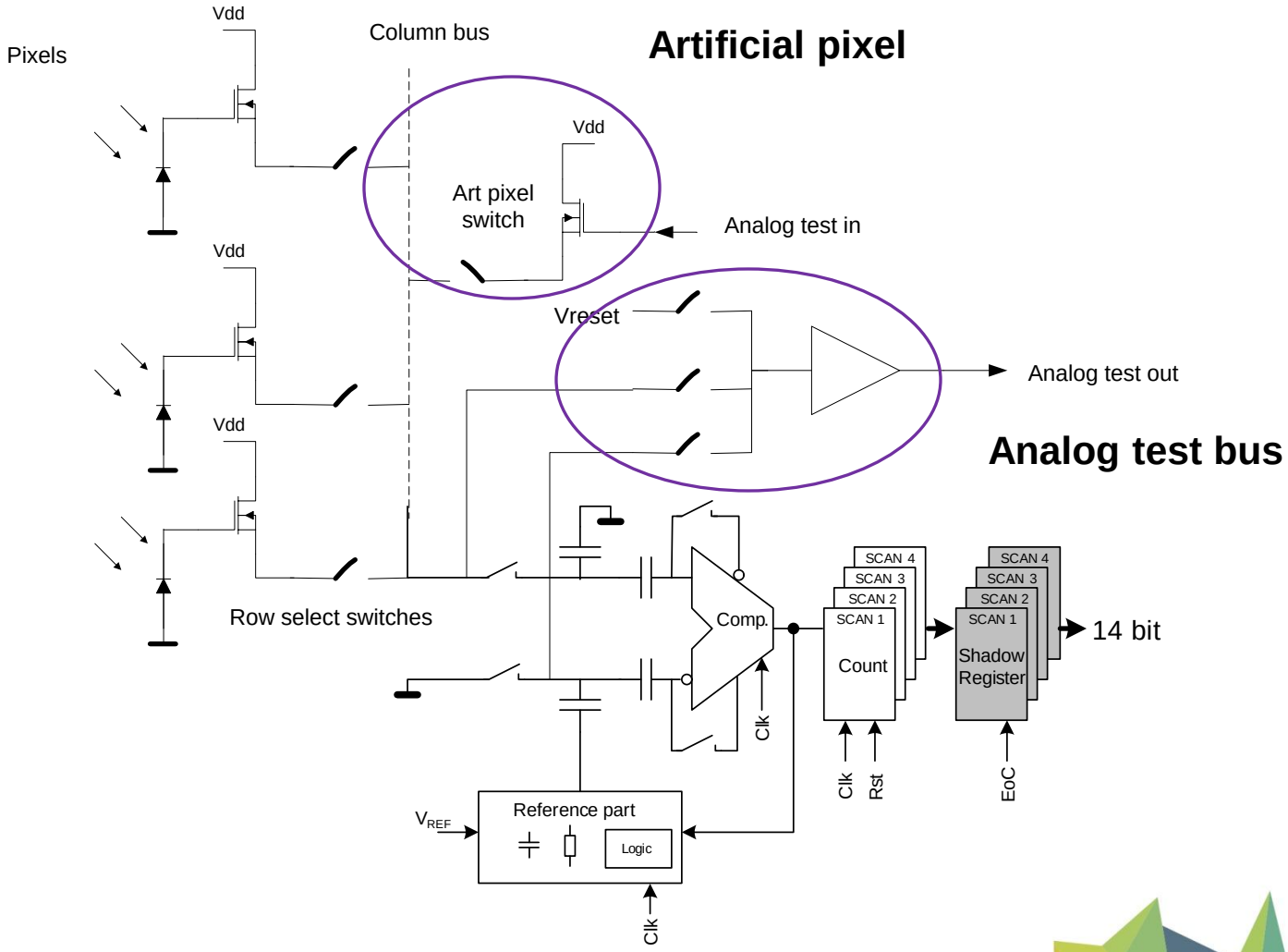
One ADC serves multiple pixel dimensions required for multiple applications

Block diagram binning implementation



1:2 binning is basically averaging the output of two vertically adjacent pixels implemented by using the offset compensation capacitors as capacitive divider

DFT implementations



Conclusions

- An on-chip column-parallel ADC is attractive for cost and performance reasons
- The presented successive approximation ADC concept is power efficient, flexible and serves various applications