

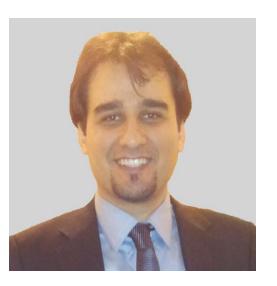


A 2.5pJ/b Readout Circuit for 1000fps Single-bit Quanta Image Sensor

Saleh Masoodian, Arun Rao, Jiaju Ma, Kofi Odame and Eric R. Fossum

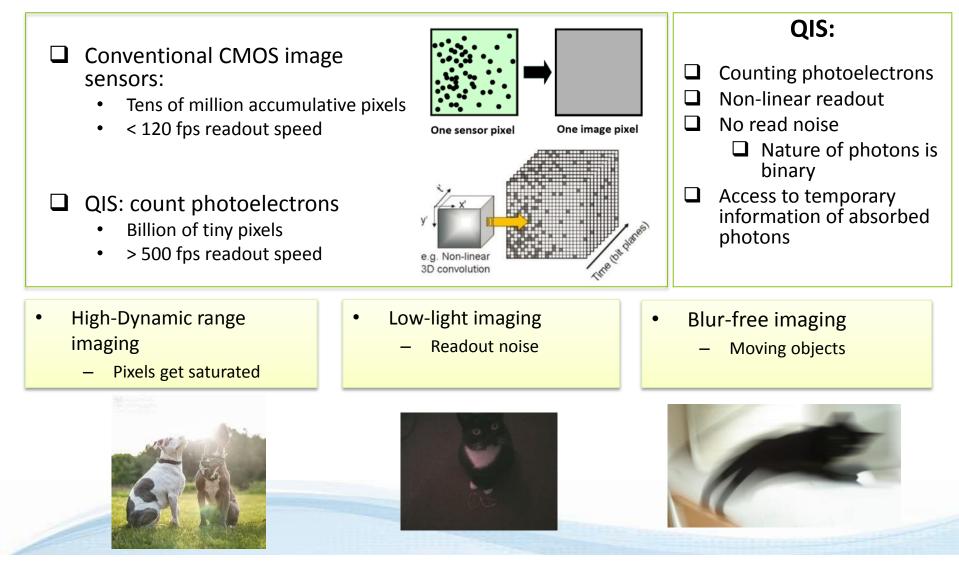
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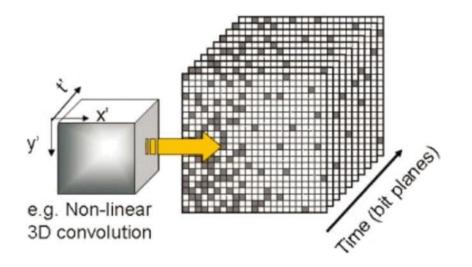
Quanta Image Sensor (QIS)







- Realizing tiny pixel (jot)
- Forming images based on jots data
- Readout
 - □High-speed
 - **Low-power**

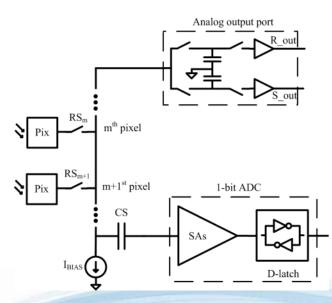


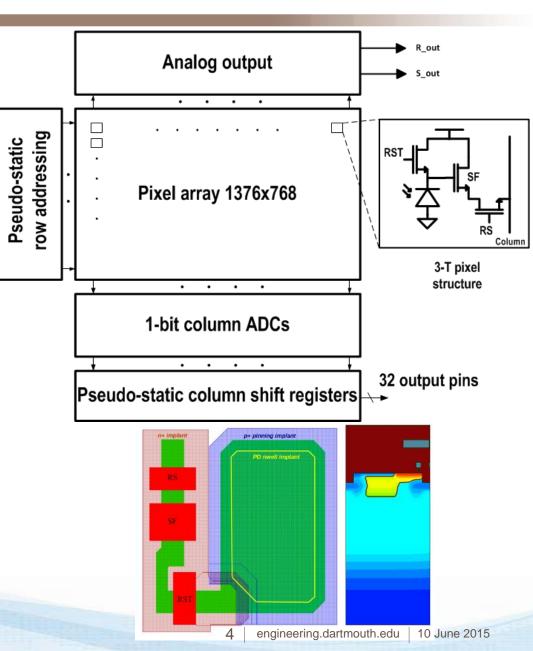
- 10 to 100 time faster
- Giga-pixel resolution



Design

- 1376Hx768V pixel array (1Mpixel)
- 1000 frames/s
- 0.18µm XFAB process
- 1376 parallel ADCs
- Output data rate: 1Gb/s

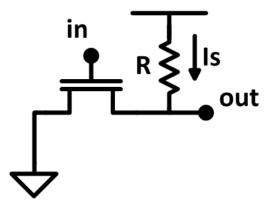




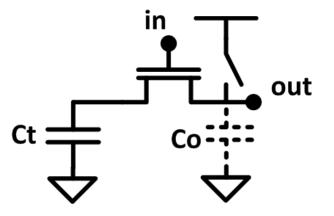


Solution

- Conventional imagers use continuous-time circuits:
 - High static power consumption

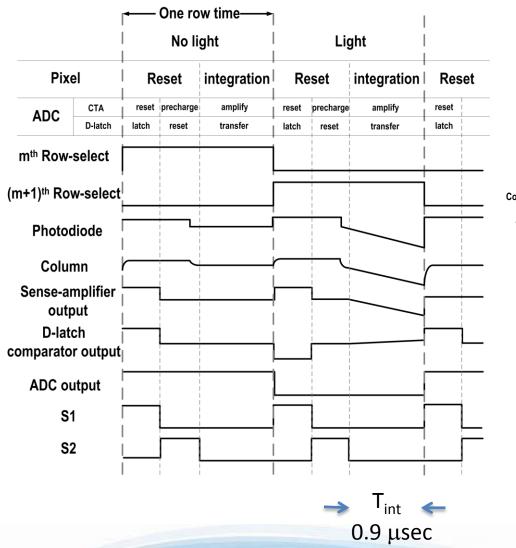


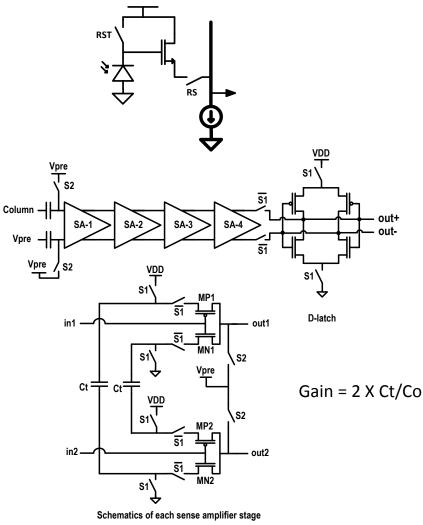
- Charge transfer amplifier technique:
 - No static power consumption





4-Stage Sense Amplifier



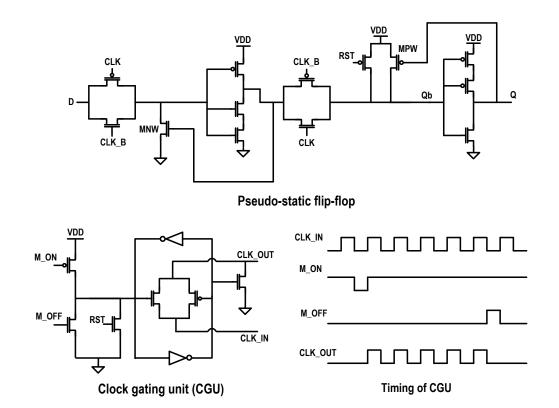


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Pseudo-Static Digital Circuits

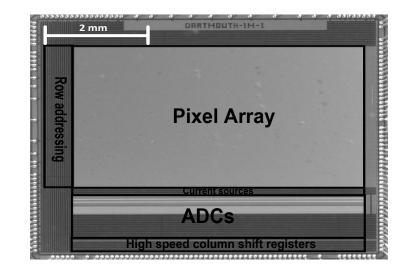
- Pseudo-static flip-flop:
 - Lower power consumption than static flip-flop
 - More reliable than dynamic flip-flop
- Clock gating:
 - Provide clock only for a group of flip-flops



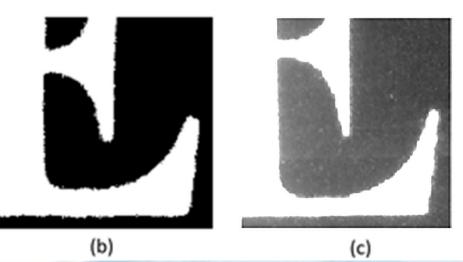


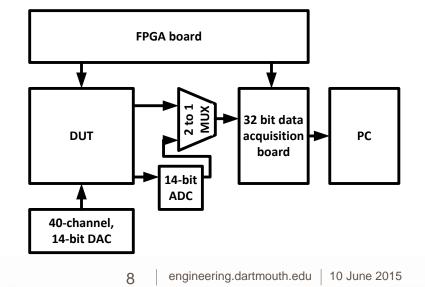
Sensor and Test System





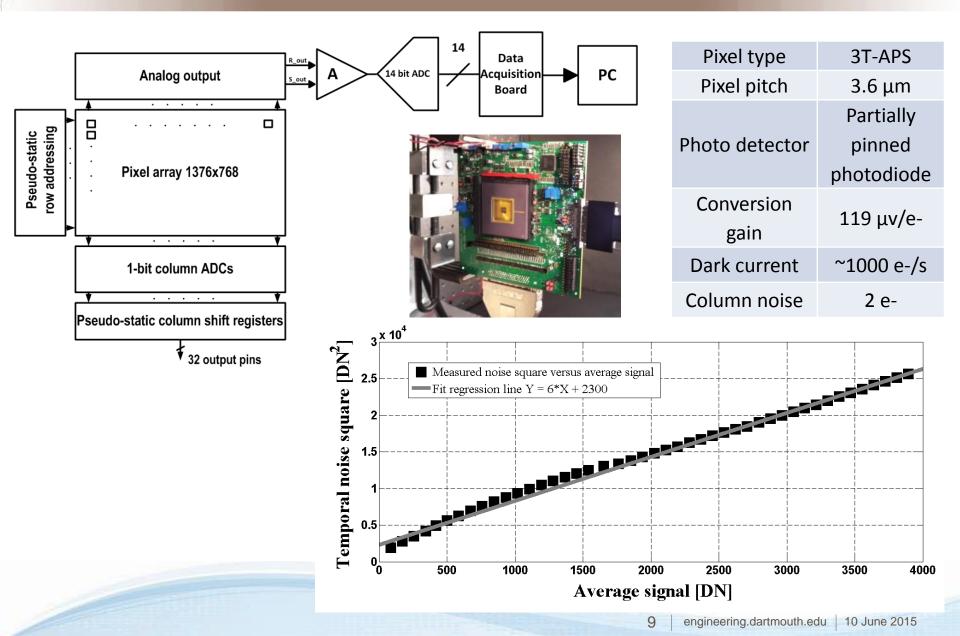
(a)







Pixel Characterization

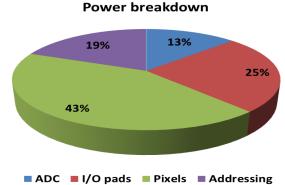




Summary of Test Results

Process		XFAB, 0.18 μm, 6M1P (non- standard implants)		
Supply voltage		1.3 V (core), 2 V (Array),		
		3 V (I/O pads)		
Pixel type		3T-APS		
Pixel pitch		3.6 μm		
Photo detector		Partially pinned photodiode		
Conversion gain		119 μv/e-		
Array		1376 (H) X 768 (V) (WXGA		
		16:9 ratio)		
Field rate		1000 fps		
ADC sampling rate		768 KSa/s		
Readout noise		2 e-		
Output data rate		1 Gb/s		
Package		PGA with 256 pins		
Power	Pixel array	8.6 mW		
	ADCs	2.6 mW		
	Addressing	3.8 mW		
	I/O pads	5 mW		
	Total	20 mW		
FOM _{ADC}		2.5 pJ/b		

	ISSCC11 [1]	ISSCC12 [2]	TED13 [3]	This work
Process (nm)	90	180	180	180
N _{ADC} (bit)	12	12	11	1
<pre>#pixels (Mega)</pre>	17.7	33.2	0.96	1.06
fps	120	120	35	1000
FOM _{ADC} (pJ/b)		16.7	21.6	2.5
FOM _{tot} (pJ/b)	118	52	108	19



T. Toyama, et al., "A 17.7Mpixel 120fps CMOS image sensor with 34.8Gb/s readout," ISSCC Dig. Tech. Papers, pp. 420-422, Feb., 2011.
T. Watabe, et al., "A 33Mpixel 120fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs," ISSCC Dig. Tech. Papers, pp. 388-390, Feb., 2012.
F. Tang, et al., "Low-power CMOS image sensor based on column-parallel single-slope/SAR quantization scheme," IEEE TED, V. 60, No. 8, Aug. 2013.



- QIS addresses some shortcomings of SOA cameras; incl. photon counting, high resolution, post capture pixel definition, HDR, TDI
- One of the challenges: high-speed and low-power readout circuits;
- 1Mega pixel, 1000fps single-bit QIS designed and tested, reasonable power consumption achieved;
- Partial 1Giga pixel, 1000fps pathfinder QIS imager has been designed, in test phase.





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