Detection and Shielding of Photon Emission in Stacked CIS

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Outlines

- Benefits of 3D stacking
- Observation of hot spots in stacked CIS
- Photon emission test structures
- Spatial distribution derivation and verification
- Physical mechanism
- Dependence on device types, sizes, and voltages
- Correlation to impact-ionization substrate current
- Practical metal shield design guidelines
- Summary

Benefits of 3D Stacking

- **From FSI to BSI**
  - Maximize the pixel level fill factor

$$\text{Pixel level fill factor} \equiv \frac{(\text{Unshielded PD area})}{(\text{Pixel area})}$$

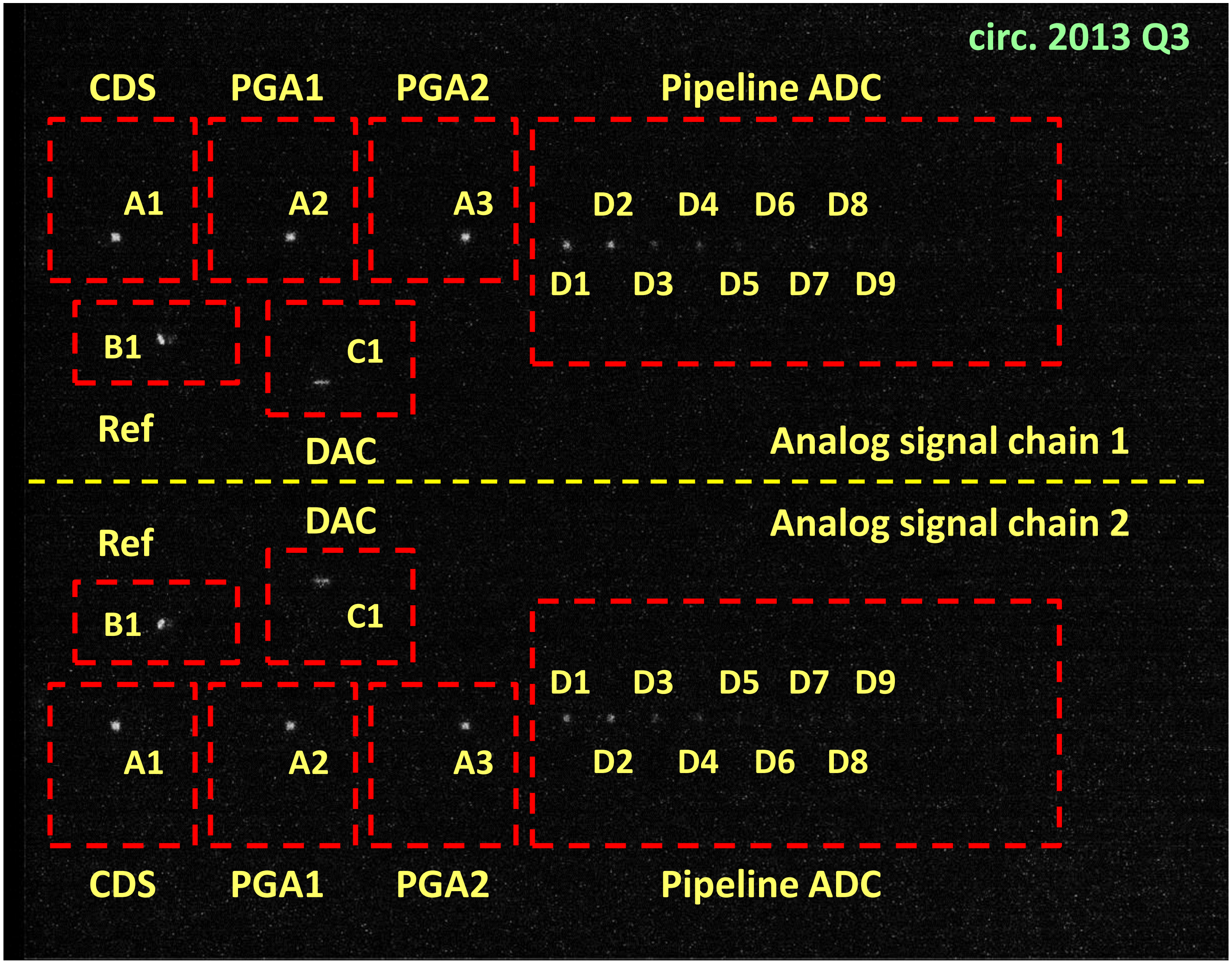
- **3D stacked BSI**
  - Maximize the chip level fill factor
    - ➡ Smaller footprint, lower Z-height, thinner camera modules
  - Decouple the process requirements for CIS & ASIC
    - ➡ Optical and electrical performance can be optimized independently
  - Well adopted by all leading-edge smart phones today

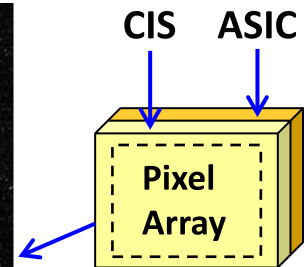
$$\text{Chip level fill factor} \equiv \frac{(\text{Pixel array area})}{(\text{Chip area})}$$

- **Potential future trend**
  - Column- and row-based 3D connection ➡ pixel-based 3D connection
  - Oxide bond with TSV/TOV ➡ oxide and metal bond simultaneously

Hot Spots Found in Test Chip Dark Image

- 1-to-1 correspondence with devices in various functional blocks





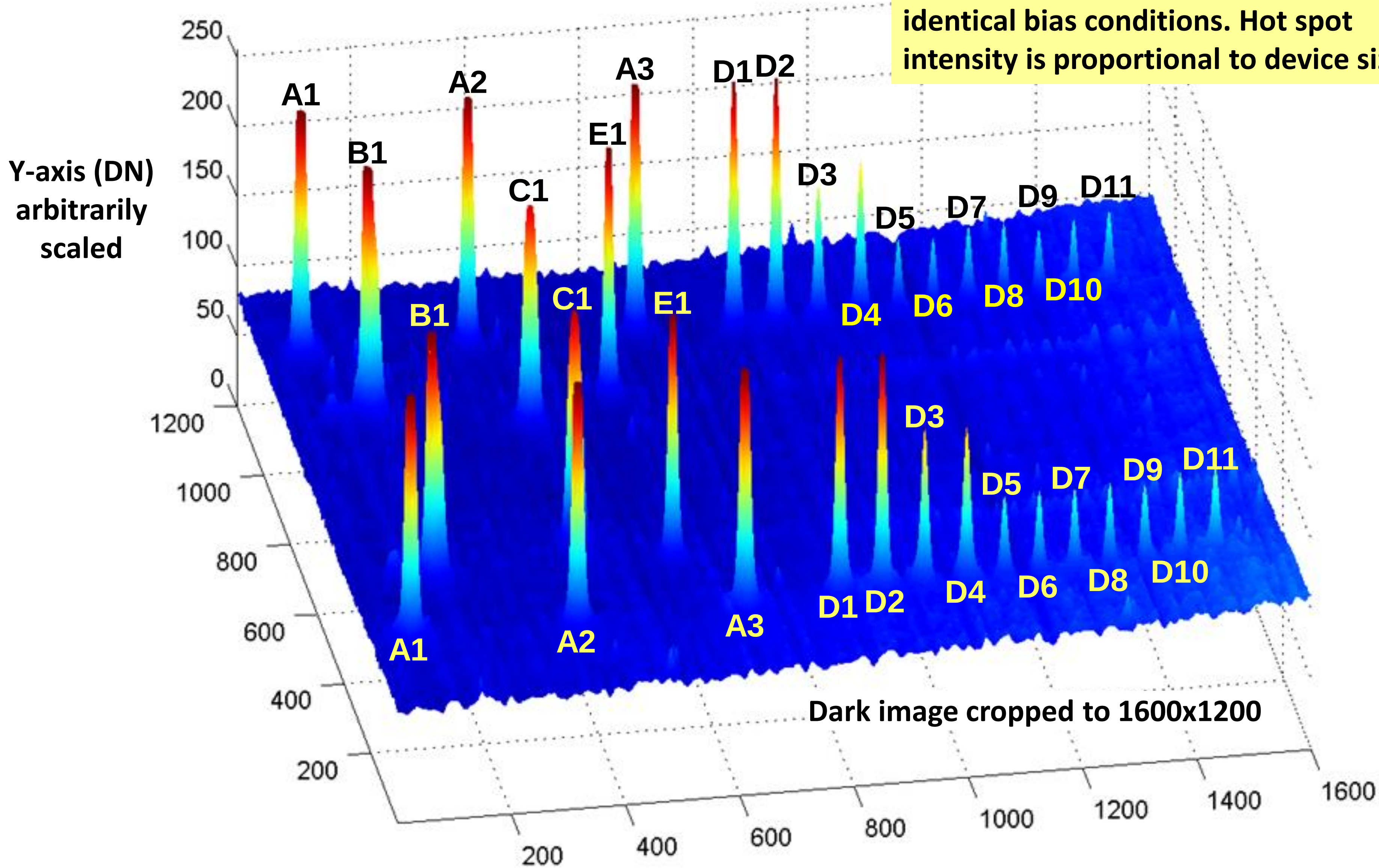
Stacked CIS
CIS: N45BSI, 1P4M
ASIC: N65LP, 1P4M

3MP test chip
1.1u pitch
2x2 shared
1.5T per pixel
Dual signal chains

Dark image
Analog gain=8
Exposure time=4s

Enhanced Hot Spot Intensities

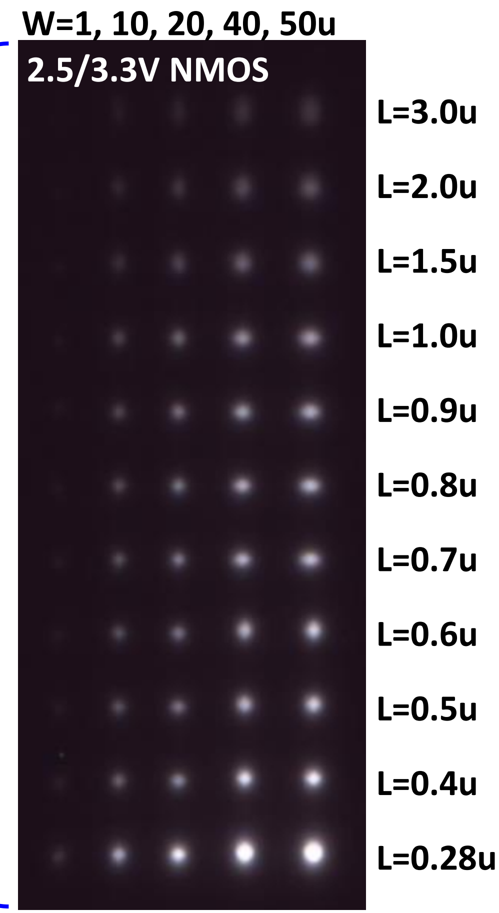
D1~D11 are scaled NMOS with almost identical bias conditions. Hot spot intensity is proportional to device size.



Test Element Group Design

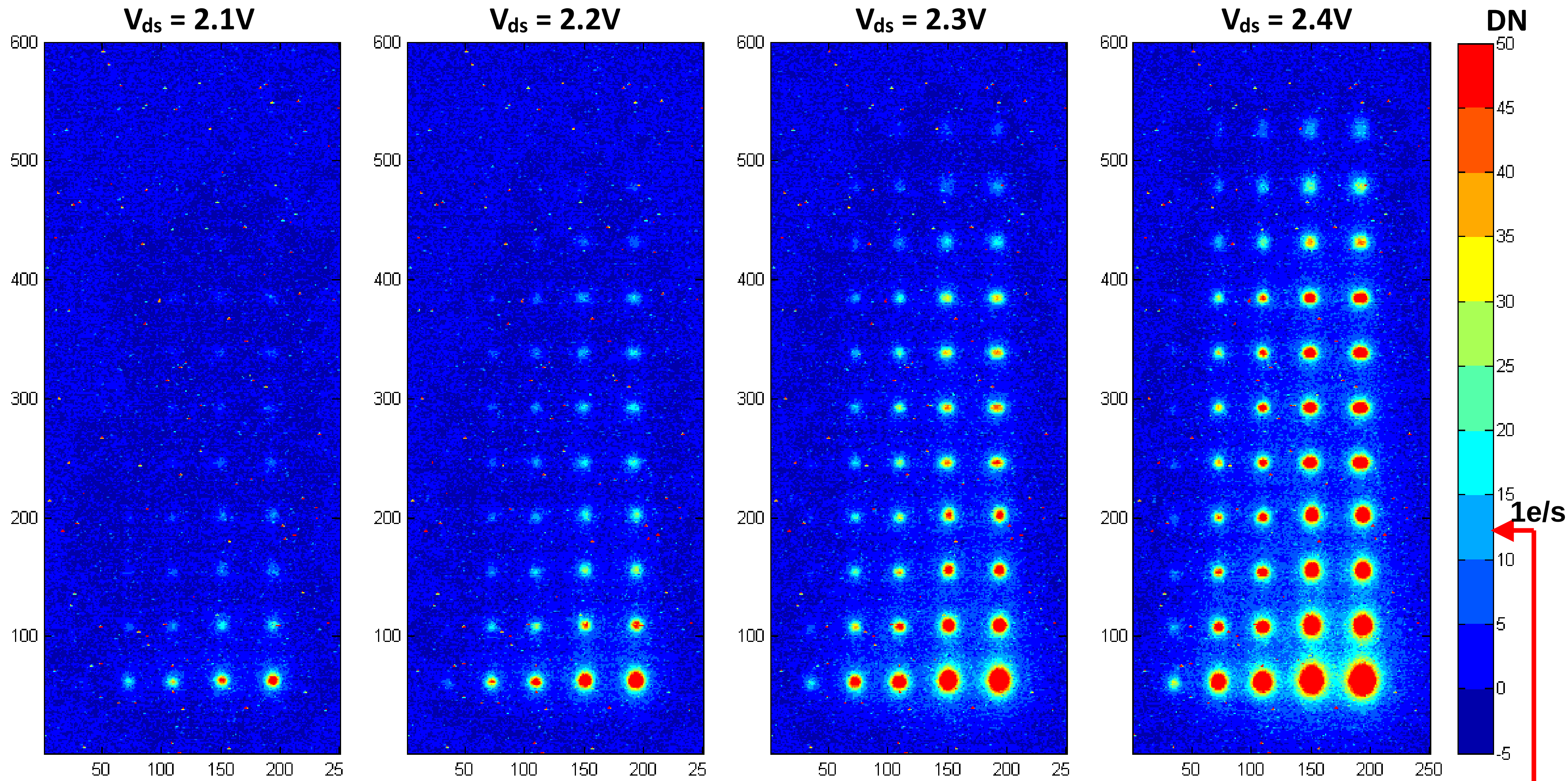
- **Objectives**: systematic study of the photon emission by device types, sizes, bias voltages, operation conditions, without or with various metal shields

	TEG Description	DUT
01	1.2V NMOS, unshielded	55
02	1.2V NMOS, 50u/0.12u, shielded	44
03	1.2V NMOS, 50u/0.06u, shielded	44
04	1.2V PMOS, unshielded	55
05	1.2V PMOS, 50u/0.12u, shielded	44
06	1.2V PMOS, 50u/0.06u, shielded	44
07	2.5/3.3V NMOS, unshielded	55
08	2.5/3.3V NMOS, 50u/0.6u, shielded	44
09	2.5/3.3V NMOS, 50u/0.28u, shielded	44
10	2.5/3.3V PMOS, unshielded	55
11	2.5/3.3V PMOS, 50u/0.6u, shielded	44
12	2.5/3.3V PMOS, 50u/0.28u, shielded	44
13	NPN, PNP BJT	6
14	P+/NW, N+/PW diode	6
15	Miscellaneous	6



A group of 5x11 NMOS that can be turned on 1-by-1 or altogether

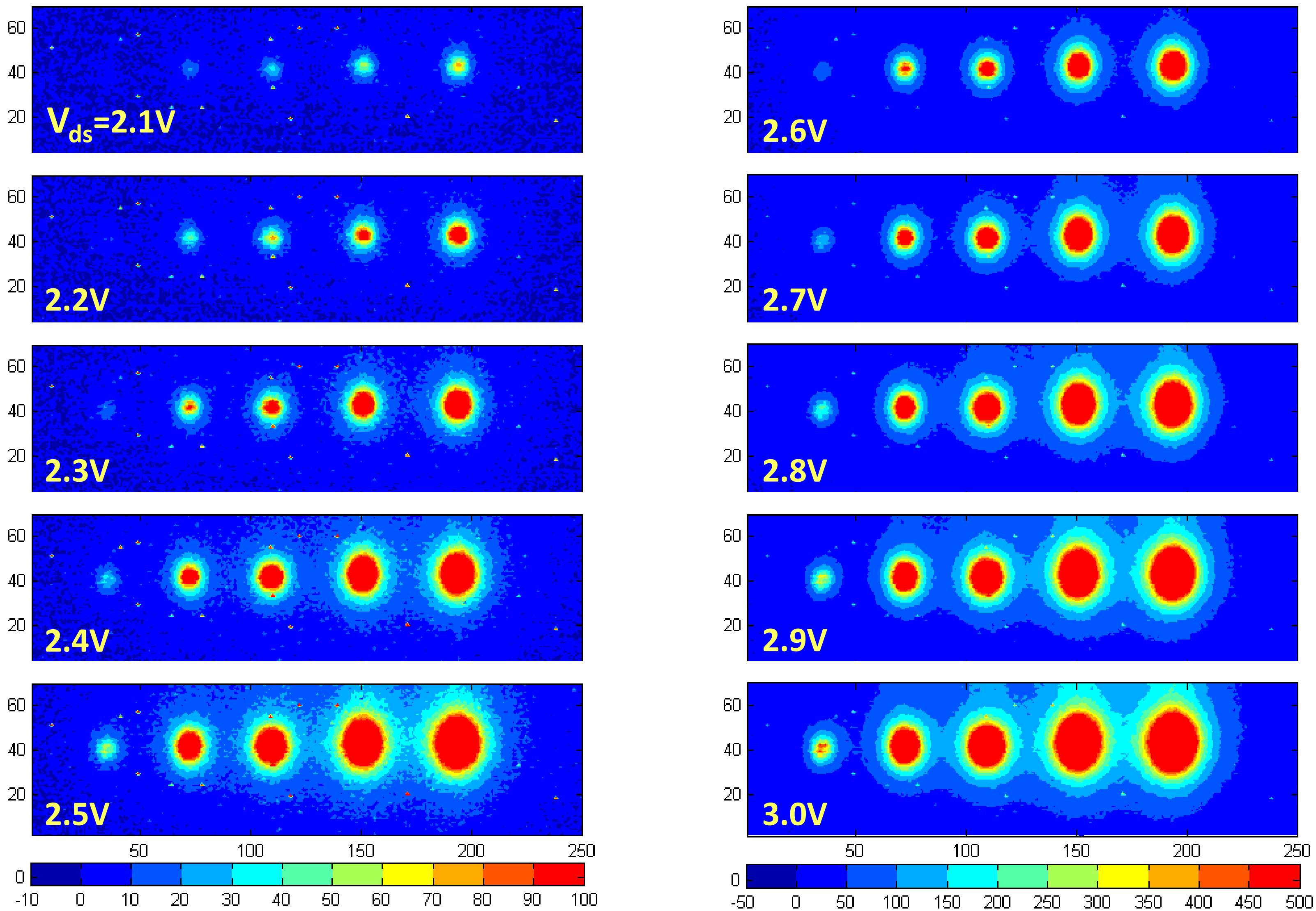
Hot Spot Intensities Strongly Depend on V_{ds}



Exposure time = 4s; 1DN ~ 0.0816e/s; V_{gs}=1.2V
X,Y unit: pixel; Z unit: DN (12b ADC)

Dark current < 1e/s at 25˚C

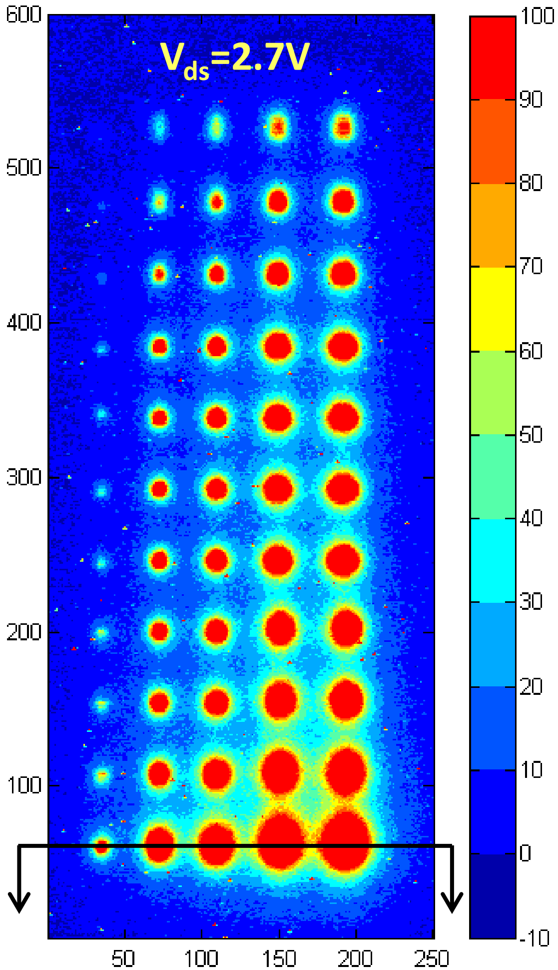
Focus on the Spatial Distribution



NMOS
L=0.28u
W=1, 10, 20, 40, 50u
V_{gs} =1.2V

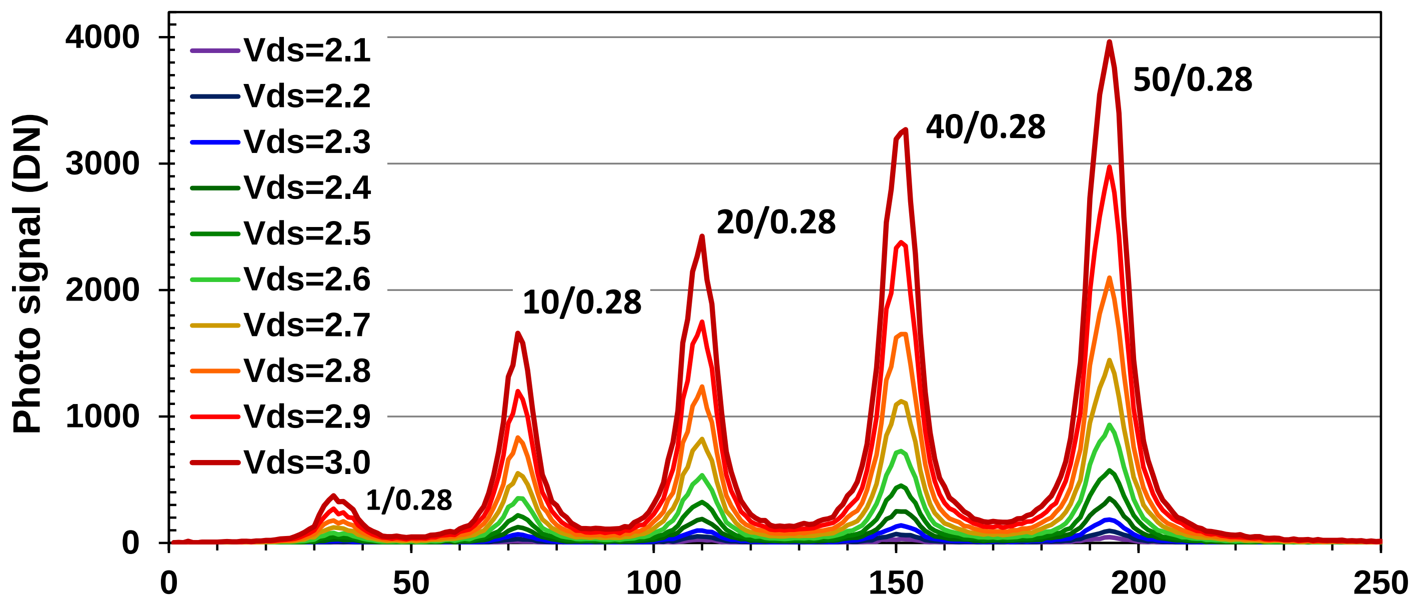
X,Y unit: pixel; Z unit: DN; note the different Z scales on left- & right-hand side.

Spatial Distribution of the Hot Spots



X,Y unit: pixel; Z unit: DN

- **Study the hot spots spatial distribution**
  - 5 DUTs: W = 1u, 10u, 20u, 40u, 50u; L=0.28u
  - Fix V_{gs} with varying V_{ds} or fix V_{ds} with varying V_{gs}



X unit: pixel; Y unit: DN (12b ADC)

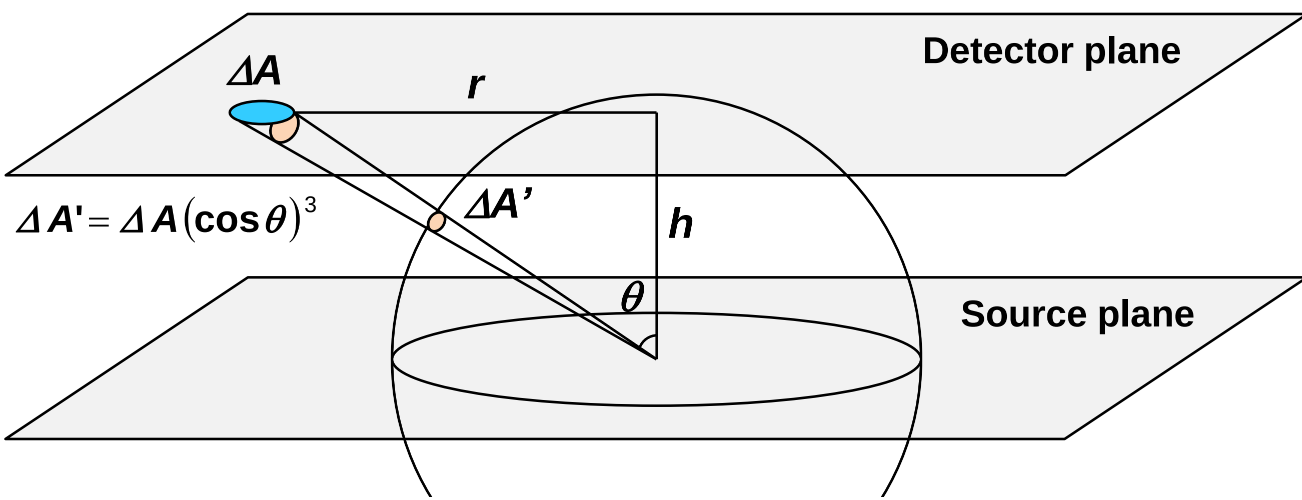
Point Spread Function (PSF)

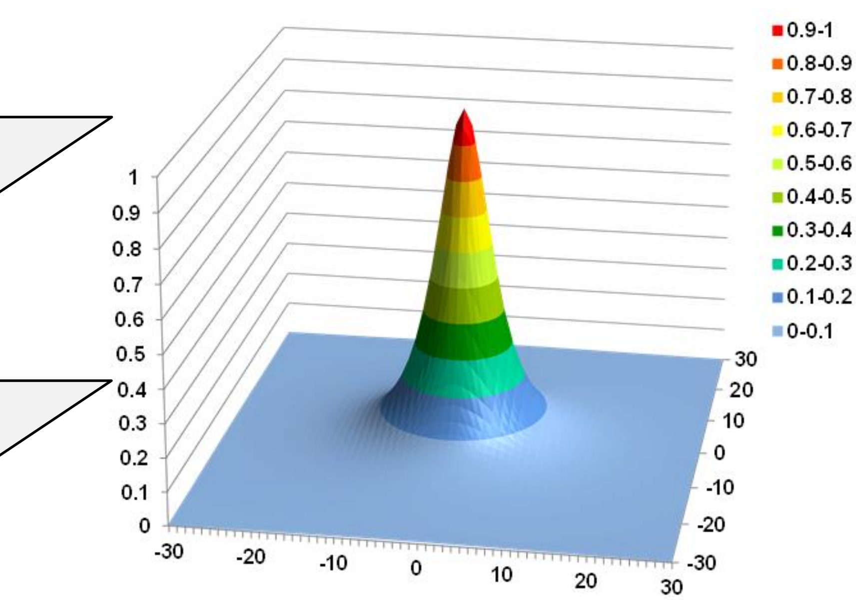
- **Assuming an isotropic point source ➡ cosine-third-power law**
  - **Combination of inverse-square law & direction cosine law**

$$E\cdot(\Delta A)=\frac{J}{4\pi h^2}(\Delta A');\quad (\Delta A)=(\Delta A')\left(\frac{r^2+h^2}{h^2}\right)\left(\frac{1}{\cos\theta}\right)$$

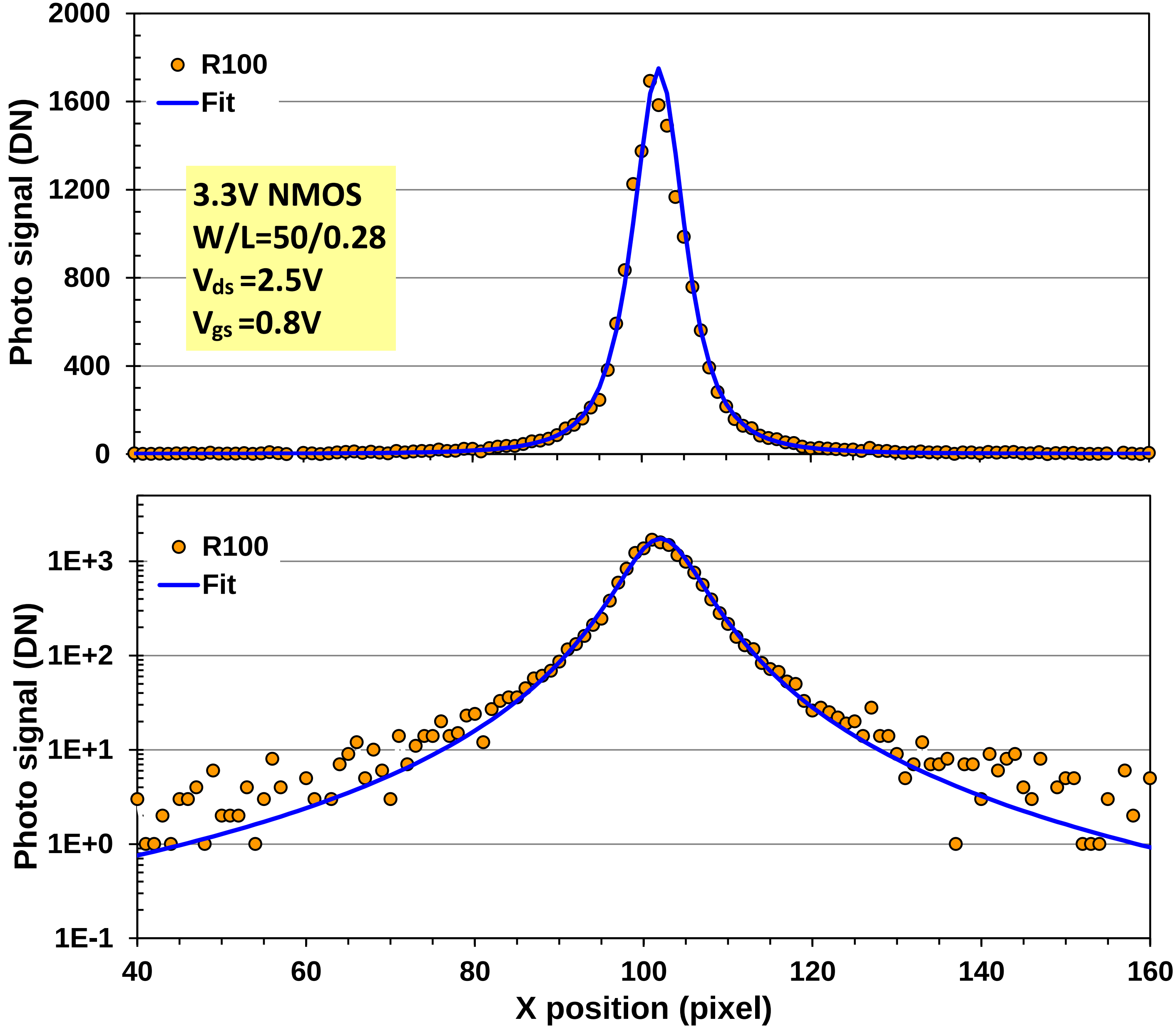
$$E(x,y)=\left(\frac{J}{4\pi h^2}\right)(\cos\theta)^3=\left(\frac{J}{4\pi h^2}\right)\frac{1}{\left(1+r^2/h^2\right)^{3/2}}$$

$$\iint E(x,y)\,dx\,dy=J/2\;;\; r^2=x^2+y^2$$





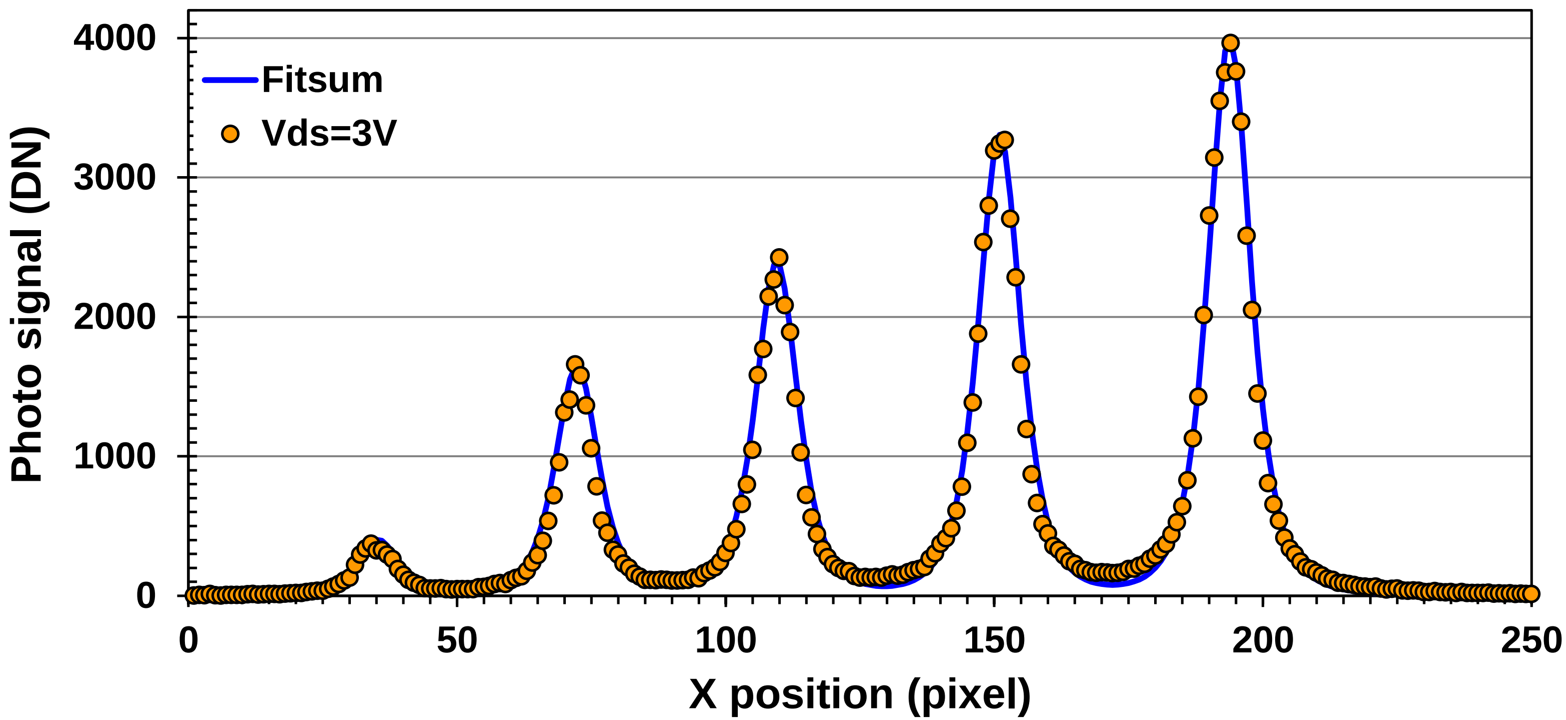
Fitting of PSF to a Single Source



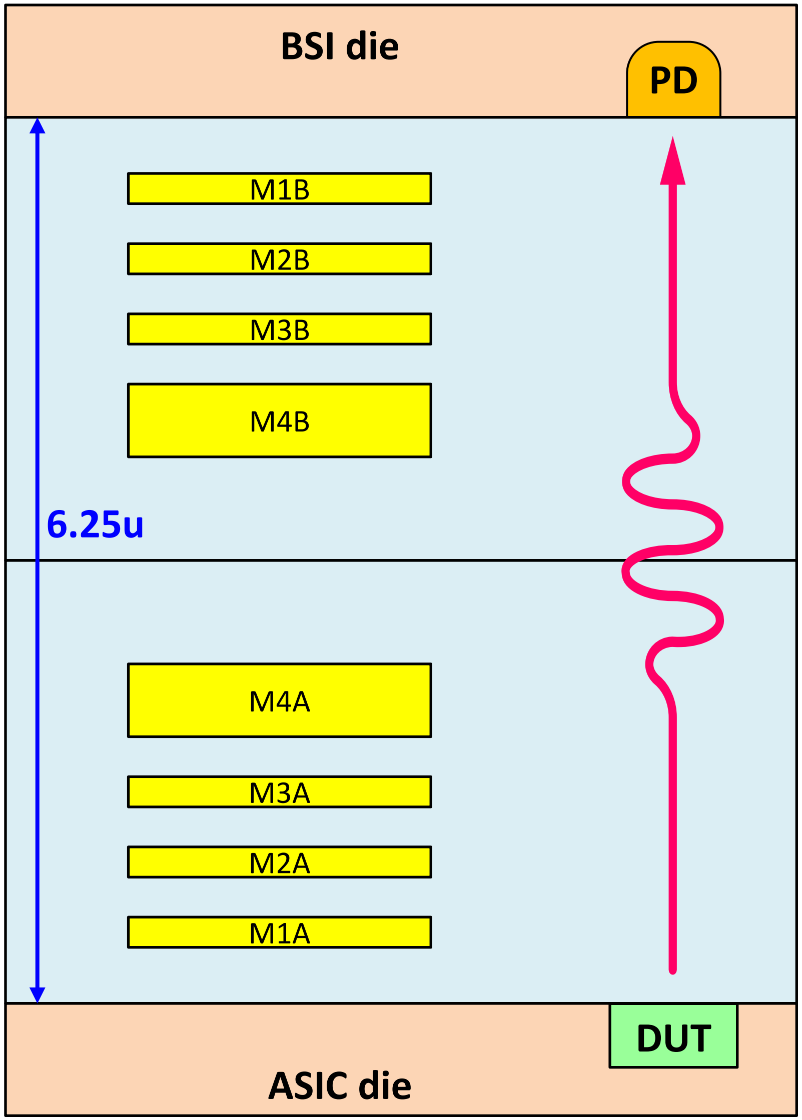
Fitting Multiple Emission Sources

- P_n, x_n, h are fitting parameters (n=1~5)
  - P_n is the strength of nth peak; x_n is the location of nth peak
  - The empirical formula fits the data reasonably well

$$E(x)=\sum_{n=1}^{5}\frac{P_n}{\left(1+\left(x-x_n\right)^2/h^2\right)^{3/2}}\ ;\ h\approx 5.5\,pixel=6.05u$$



Comparing to BEOL Structure

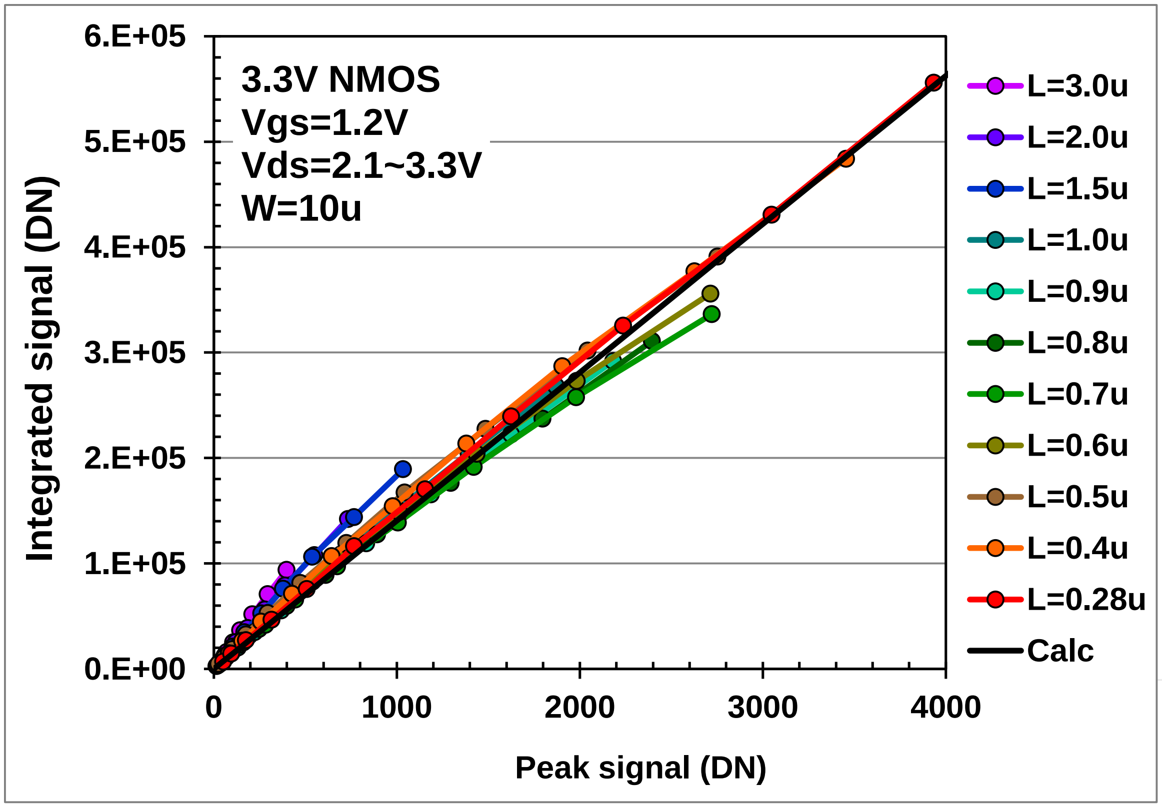


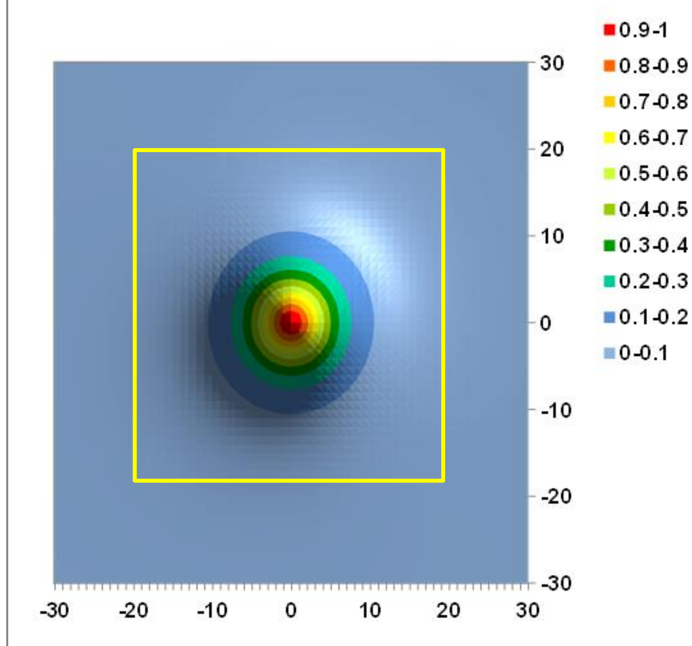
- The best-fit parameter *h* matches reasonably well with estimated distance
  - Extracted from emission data: ***h* ~ 6.05u**
  - Estimated from process: ***h* ~ 6.25u**
    - Test chip uses 1P4M ASIC & 1P4M BSI
- In real silicon the BEOL dielectric stack is a complicated multi-layer structure with various refractive indices
  - Optical simulation is needed to account for the reflection, refraction, and diffraction at various interfaces

Another Validation of the Empirical PSF

- The ratio of the integrated photo signal to the peak signal is relatively constant, independent of device size and bias conditions
  - Measured data showed the same slope as the calculation predicted

$$S = \sum_{x=-20}^{20} \sum_{y=-20}^{20} \frac{1}{\left(1+\left(x^2+y^2\right)/h^2\right)^{3/2}} \approx 145.5$$





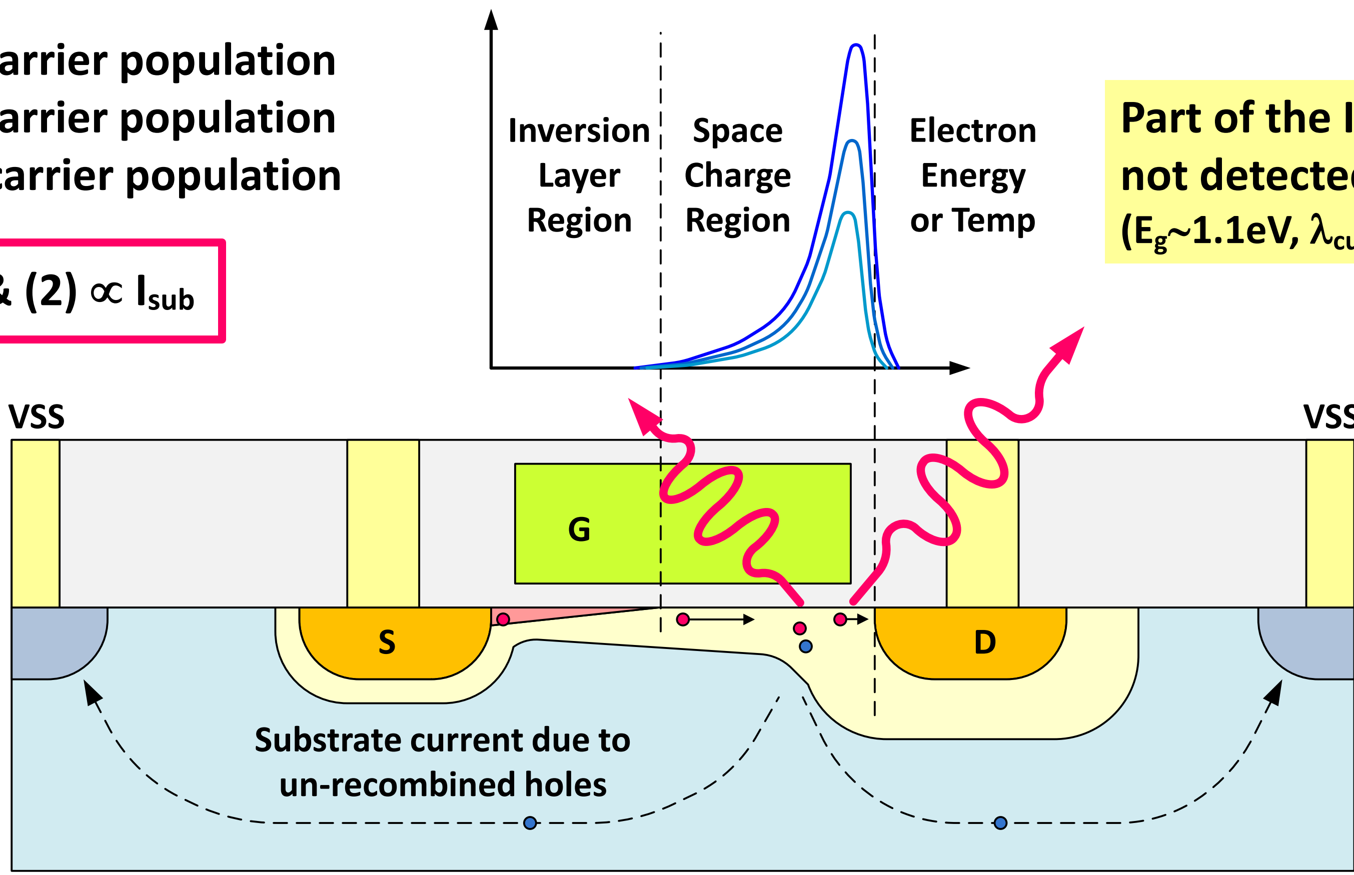
X,Y unit: pixel

Physical Mechanism

- **Hot carriers caused by high lateral electric field**
  - ➡ **(1) Brake radiation (*bremsstrahlung*) of energetic hot carriers**
  - ➡ **(2) Radiative recombination of e-h pairs generated by impact ionization**

(1) $\propto$ Hot carrier population
(2) $\propto$ Hot carrier population
I_{sub} $\propto$ Hot carrier population

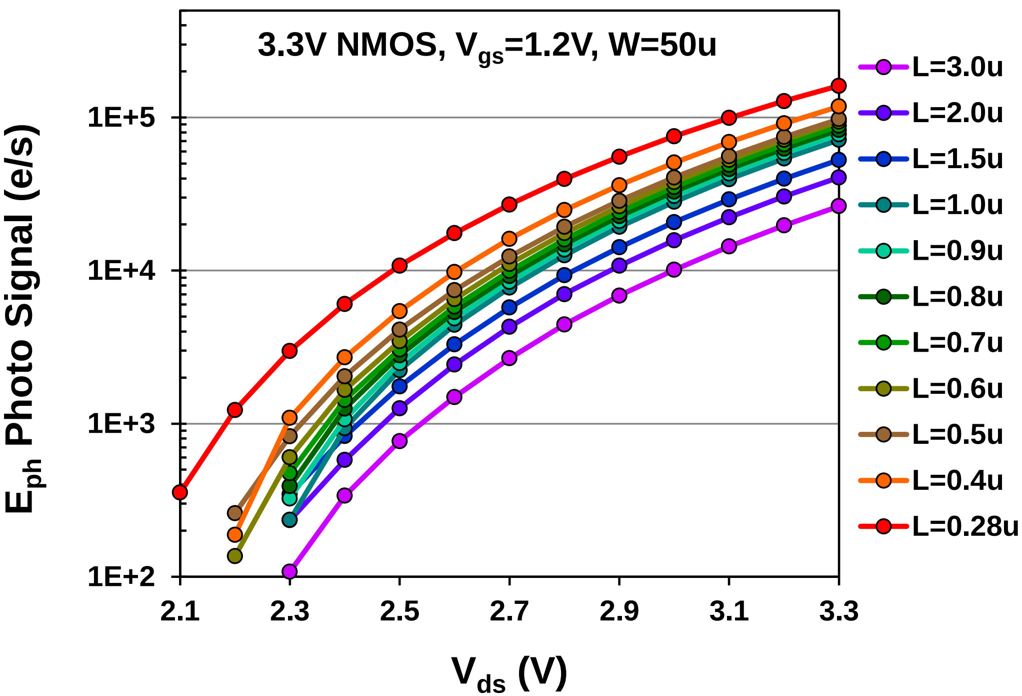
➡ **(1) & (2) $\propto$ I_{sub}**

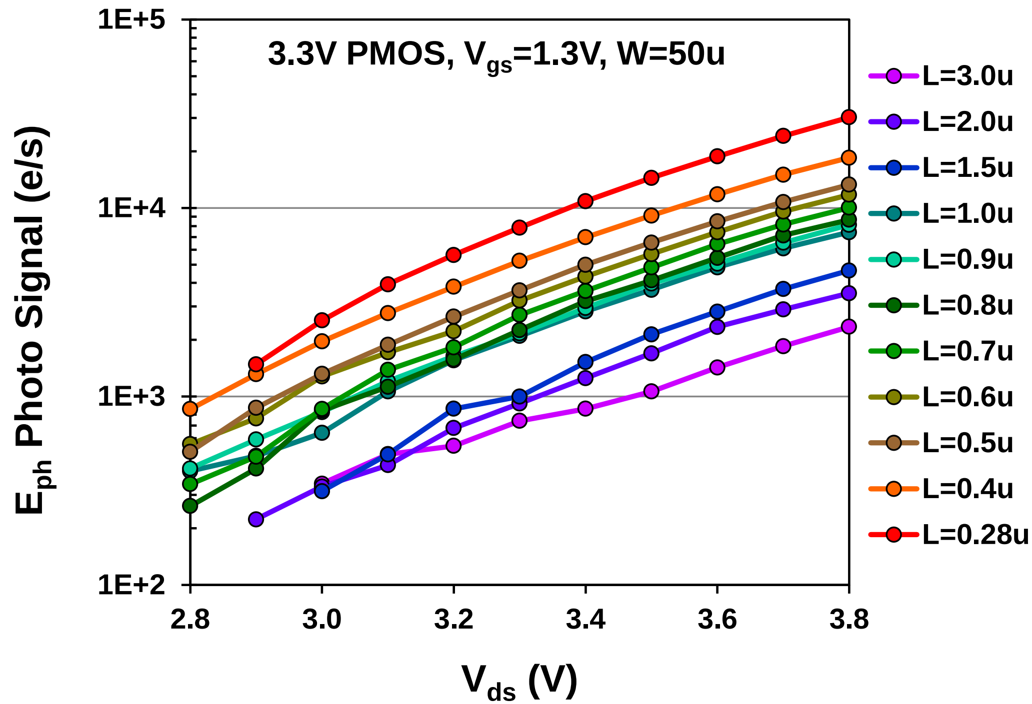


Part of the IR emission is not detected by Si PD (E_g~1.1eV, λ_{cutoff} ~1.17um)

Photon Emission vs. V_{ds}

- Photon emission is clearly not proportional to I_{ds}
- The strong dependence on V_{ds} is similar to the impact ionization I_{sub}
  - Electric field across the space-charge region ~ $(V_{ds} - V_{dsat})$
- PMOS shows much weaker photon emission than NMOS
  - Hole has larger effective mass, smaller mobility, smaller mean-free-path



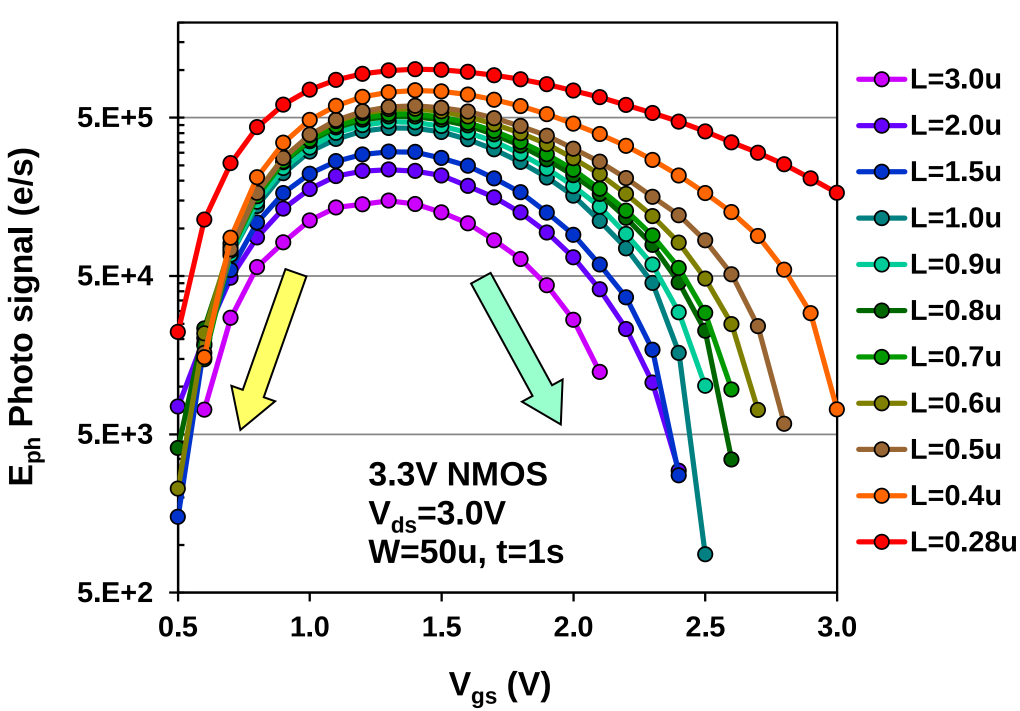


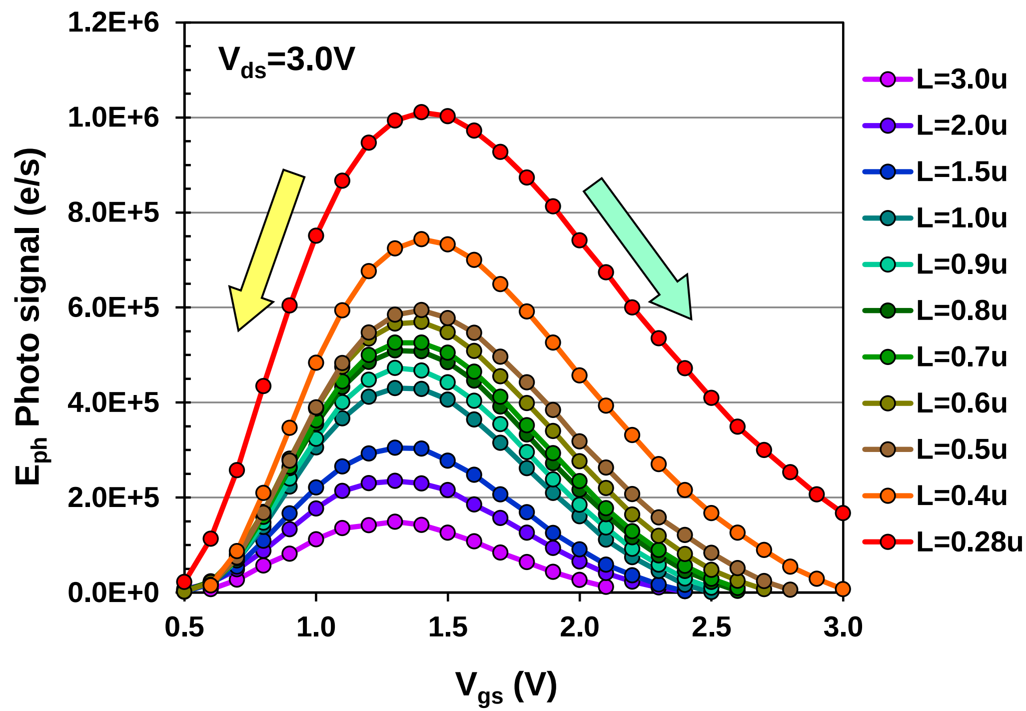
Photon Emission vs. V_{gs}

- **Low-V_{gs} region**: PE dominated by I_{ds}
- **High-V_{gs} region**: PE dominated by impact ionization
  - $V_{dsat} \sim V_{gs} - V_{th}$; $V_{ds} - V_{dsat} \sim$ voltage across the pinch-off region

$$E_{ph} \propto I_{ds} \propto \exp\left(\frac{V_{gs}}{nkT}\right)$$

$$E_{ph} \propto \exp\left\{\frac{-P_1}{V_{ds} - V_{gs} + V_{th}}\right\}$$





Photon emission dominated by I_{ds}

Emission dominated by impact ionization

V_{gs} ↓, I_{ds} ↓
Photon emission ↓

V_{gs} ↑, V_{dsat} ↑, (V_{ds}-V_{dsat}) ↓
Photon emission ↓

Empirical Formulae for Photon Emission

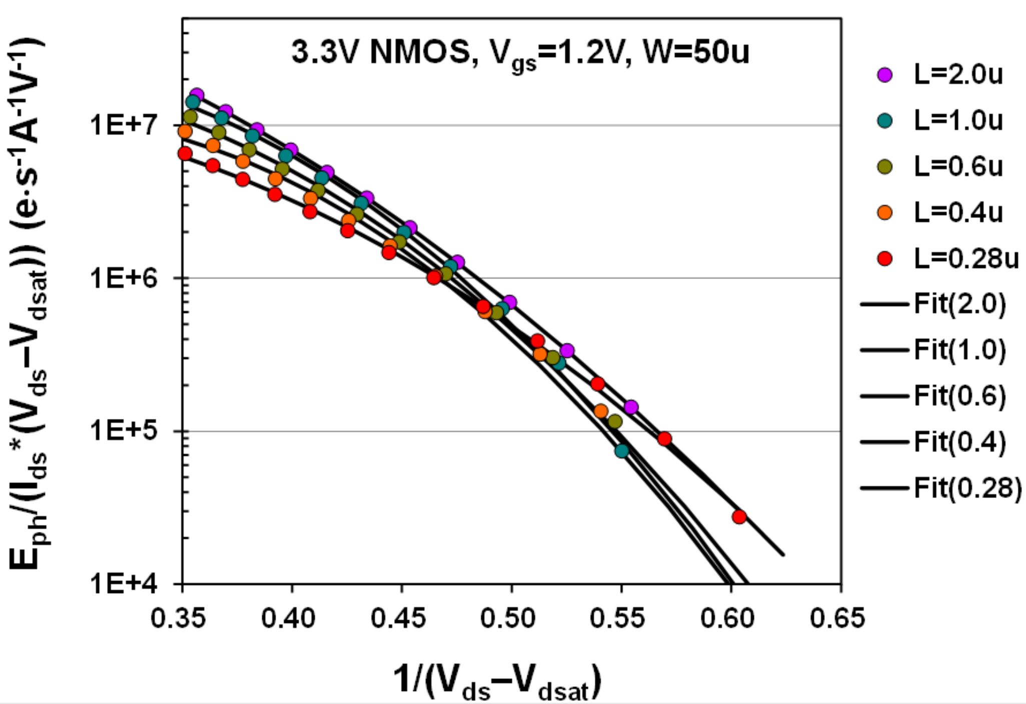
- **Use the same equation as in BSIM4 I_{sub} model**
  - For PMOS, the data can be well described by Eq. (1)
  - For NMOS, we added a 2nd order term to the exponent in Eq. (2)

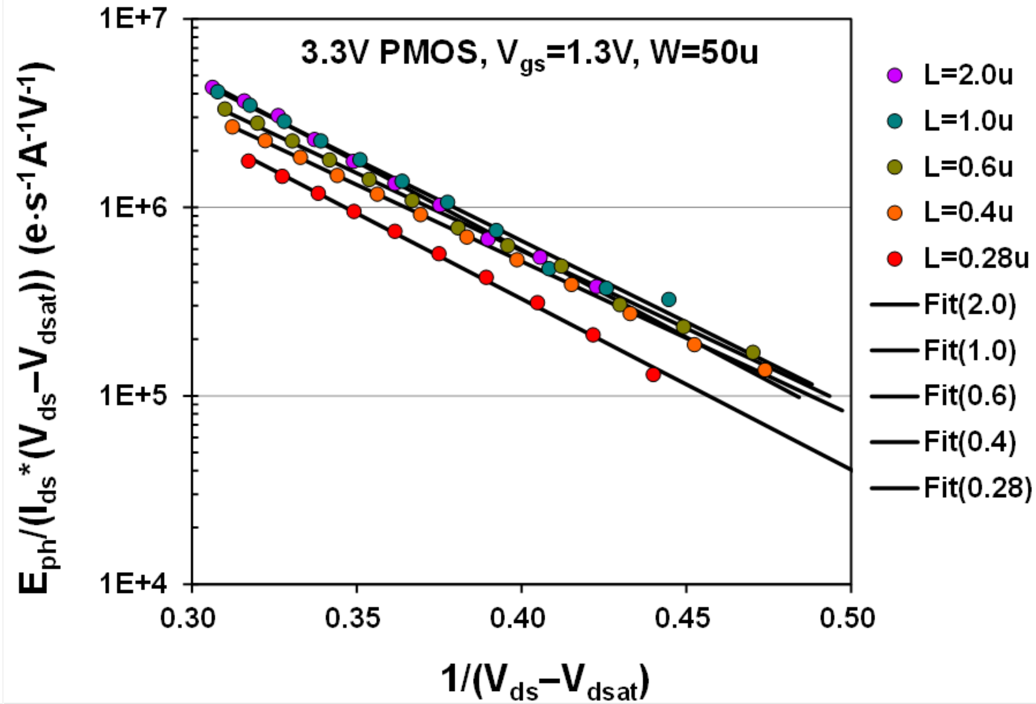
Under investigation

(1) $E_{ph} \approx P_0 \cdot I_{ds} \cdot (V_{ds} - V_{dsat}) \cdot \exp\{-P_1/(V_{ds} - V_{dsat})\}$

(2) $E_{ph} \approx P_0 \cdot I_{ds} \cdot (V_{ds} - V_{dsat}) \cdot \exp\{-P_1/(V_{ds} - V_{dsat}) - P_2/(V_{ds} - V_{dsat})^2\}$

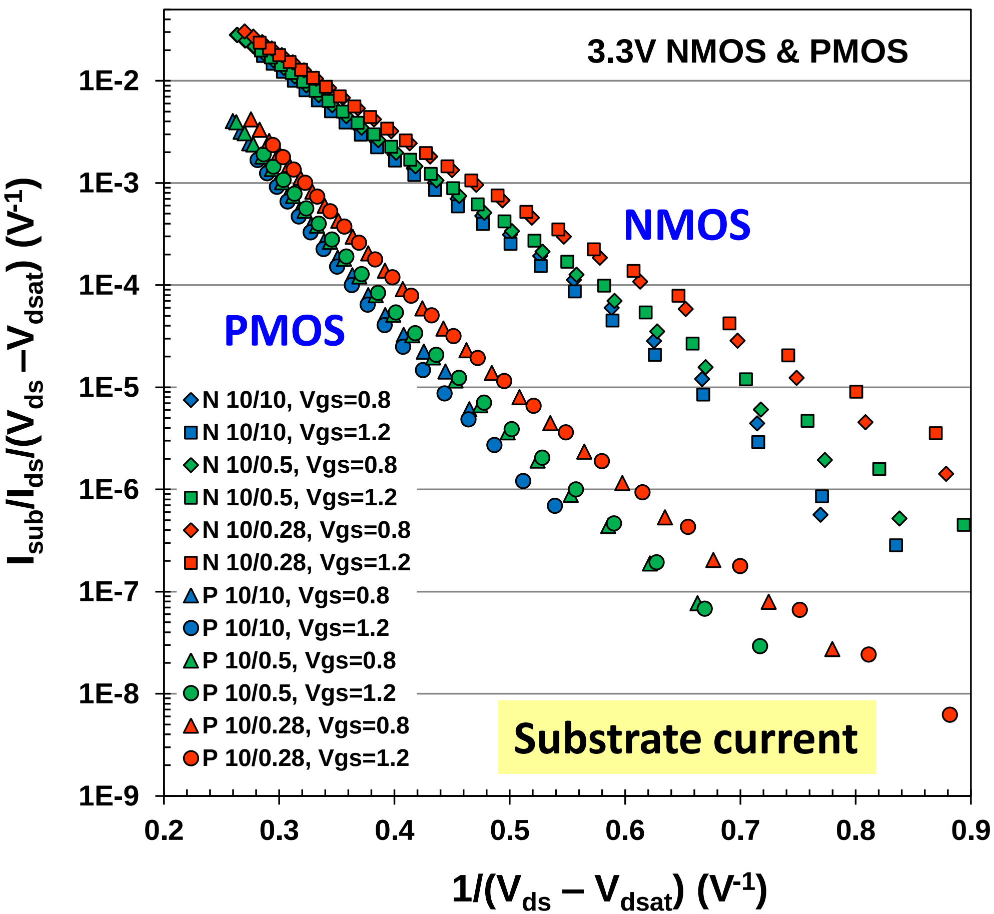
P_0, P_1, P_2 are parameters to be extracted from data

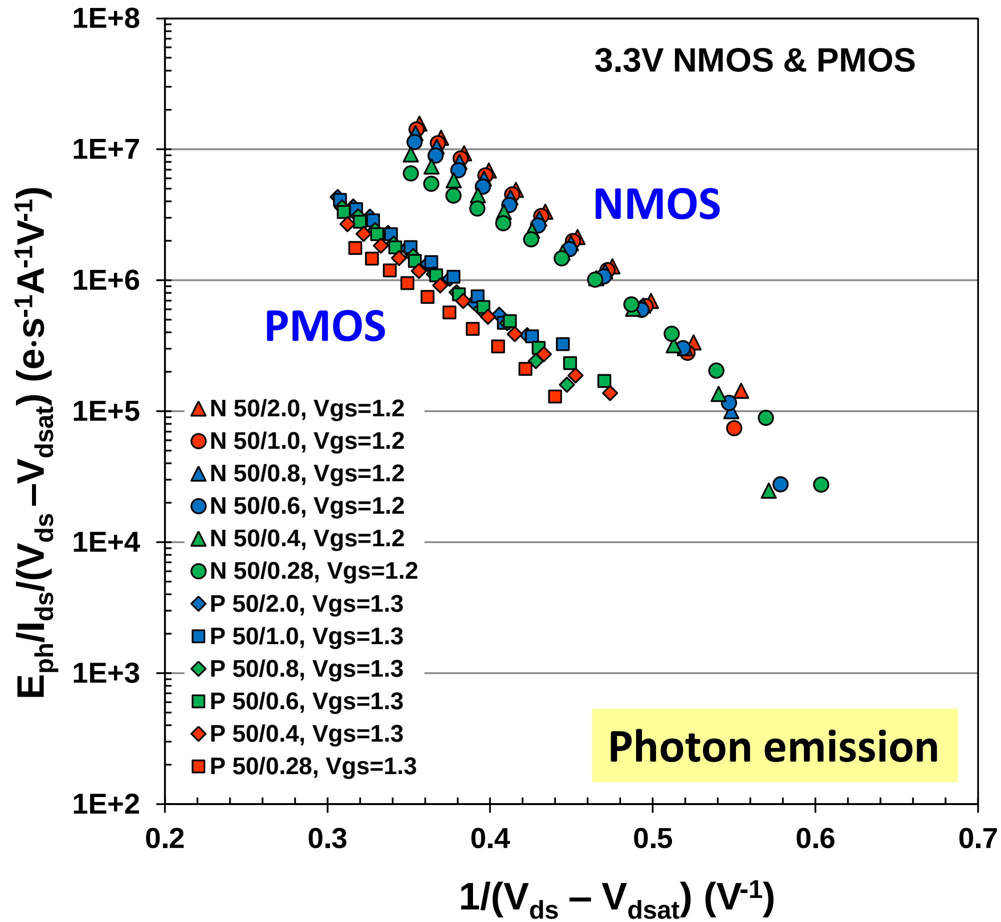




Photon Emission Correlated to I_{sub}

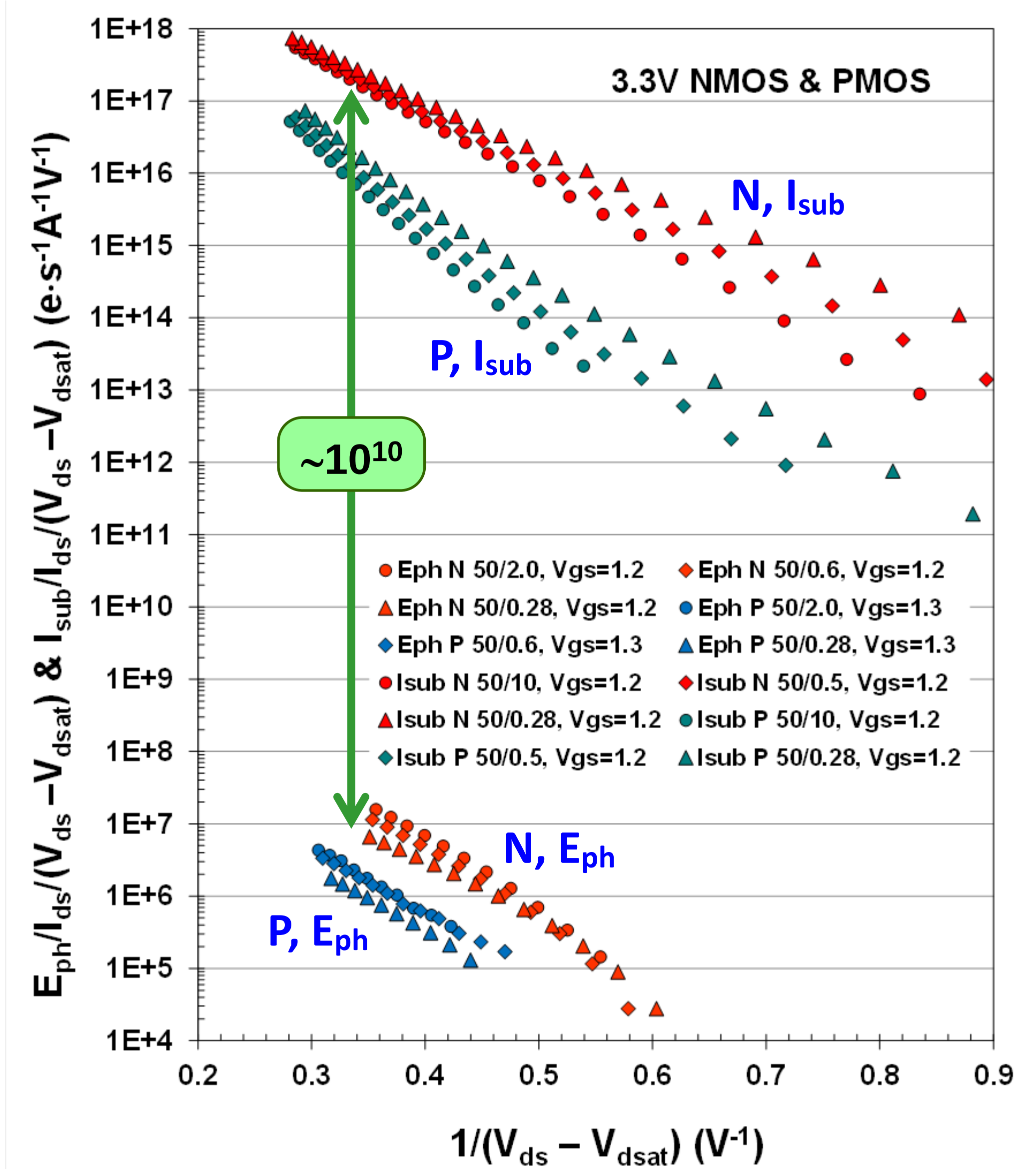
- Except the detailed features, the photon emission and substrate current show similar voltage (V_{ds}, V_{gs}) dependence and NMOS vs. PMOS ratios
  - Only part of the photon emission is detectable by Si photodiodes
  - The percentage may depend on voltage, not a constant





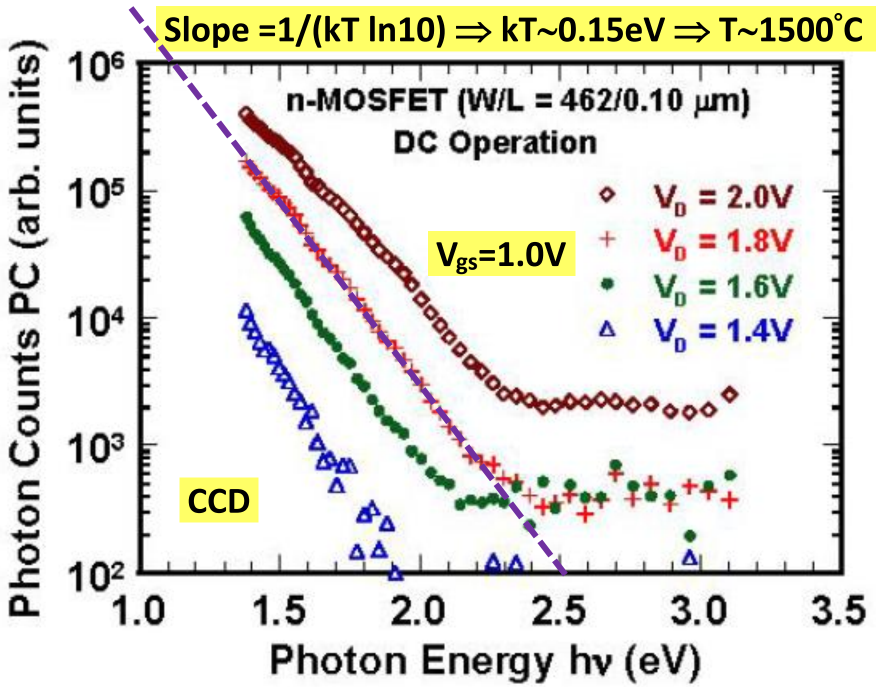
Comparing Photon Emission to I_{sub}

- **Detected photo-carriers vs. I_{sub} ratio is approximately 1 : 10^{10}**
- **Only a small portion of hot carriers generate photons**
  - Hot carriers may lose energy via impact ionization or heat dissipation
- **Only a small portion of the photons are detected by pixel array**
  - At least a hemisphere of photons are lost
  - Absorbed by poly-gate
  - Blocked by silicide & metal wires
  - Photons with E < 1.1eV are not detected
  - PD QE < 70%

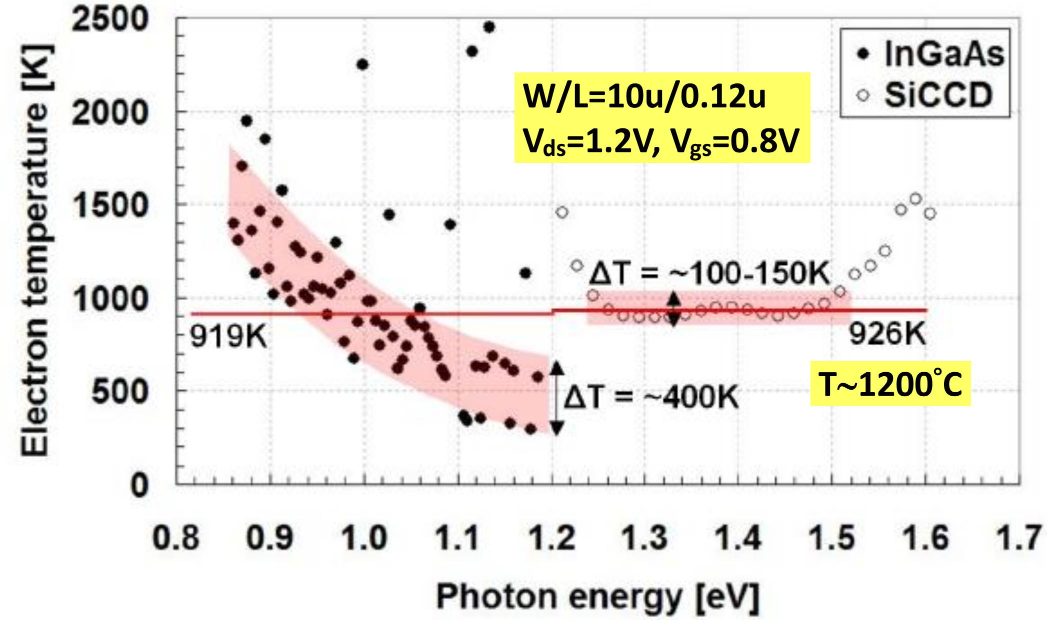


Hot Carrier Temperature

- Photon energy distribution tail follows Maxwell-Boltzmann distribution
- Inferred hot carrier temperature can be 1000˚C or higher
- Hot carrier energy can exceed eV_{ds}! (but average energy ~3kT/2 << eV_{ds})



T. Matsuda et al., "A test structure for spectrum analysis of hot-carrier-induced *photoemission* from scaled MOSFETs under DC & AC operation," pp. 71~74, ICMTS (2009)



A. Glowacki et al., "Electron temperature – the parameter to be extracted from backside spectral photon emission," IRPS, pp. 5B.6.1~5B.6.7 (2013)

Metal Shield Design Guidelines

- **Step 1: Identify the emission sources (aggressors)**
  - e.g., NMOS V_{ds} > 2V; PMOS V_{ds} > 2.7V (preliminary)
  - TBD: AC operated MOS; forward-biased p-n diodes, BJTs
- **Step 2: Estimate the total emission**
  - Process independent generic equation
  - Process dependent parameters: P_0, P_1 & P_2

$$E_{ph} \approx P_0\, I_{ds}\left(V_{ds} - V_{dsat}\right)\, \exp\left\{-\frac{P_1}{\left(V_{ds} - V_{dsat}\right)} - \frac{P_2}{\left(V_{ds} - V_{dsat}\right)^2}\right\}$$

- **Step 3: Estimate the shield size on pixel plane**
  - Define the target residual emission level (e.g., 1e/s)
  - Estimate the peak emission for each source
    - Parameter *h* is BEOL process dependent
  - Use the PSF formula to estimate the hot-spot size

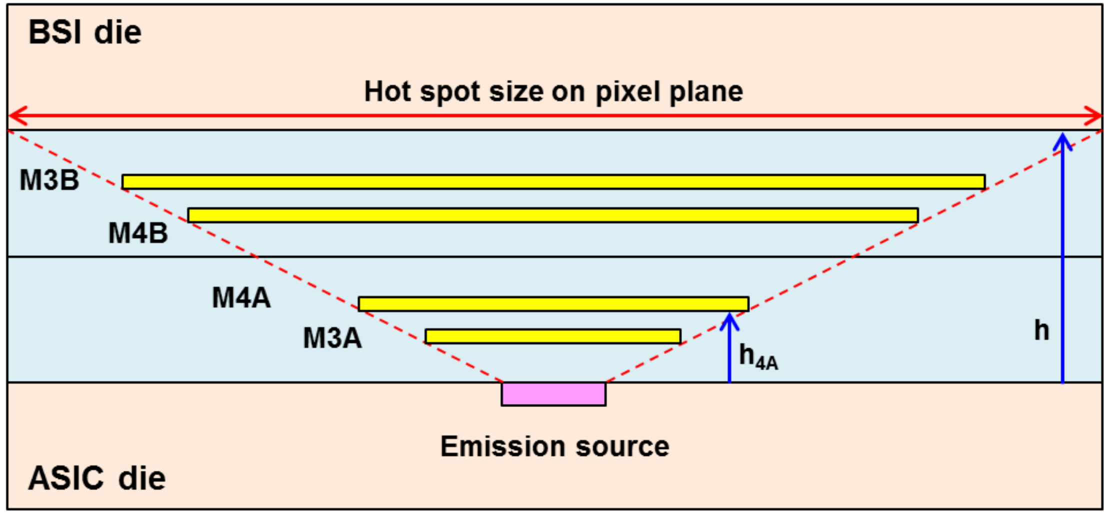
$$P_n \approx E_{ph,n} / 145.5\ ;\ n = 1, 2, \cdots N$$

$$E_{total}(x) = \sum_{n=1}^{N} \frac{P_n}{\left(1 + \left(x - x_n\right)^2 / h^2\right)^{3/2}}$$

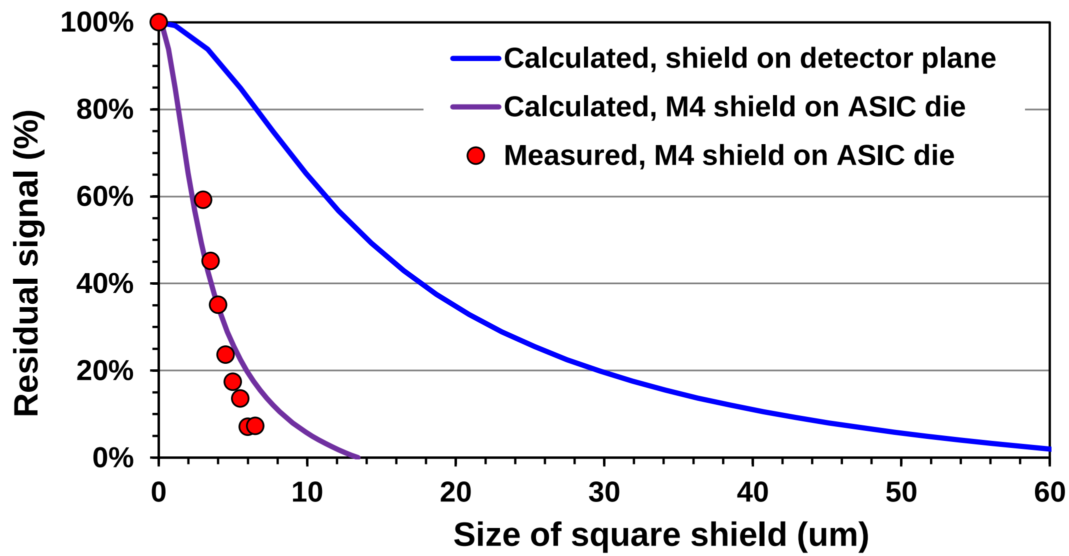
- **Step 4: Determine the metal shield size**
  - Use the BEOL structure as a scaling calculator

Example of Metal Shield Design

- Scaling the metal size according to the BEOL vertical structures
  - Line-of-sight approximation

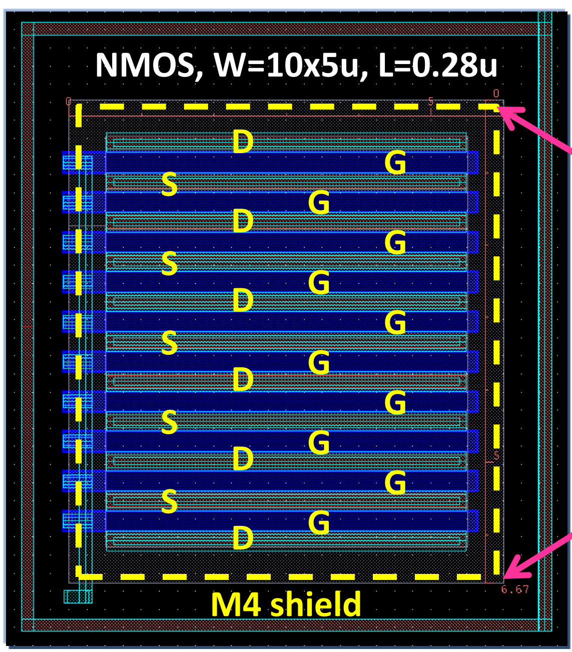


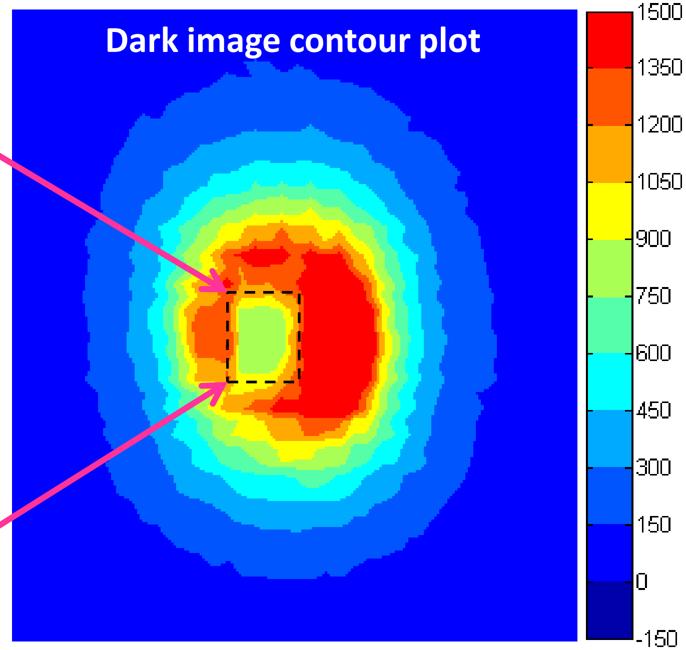
- Comparing the calculated curve with TEG measurement results
  - Reasonably matched

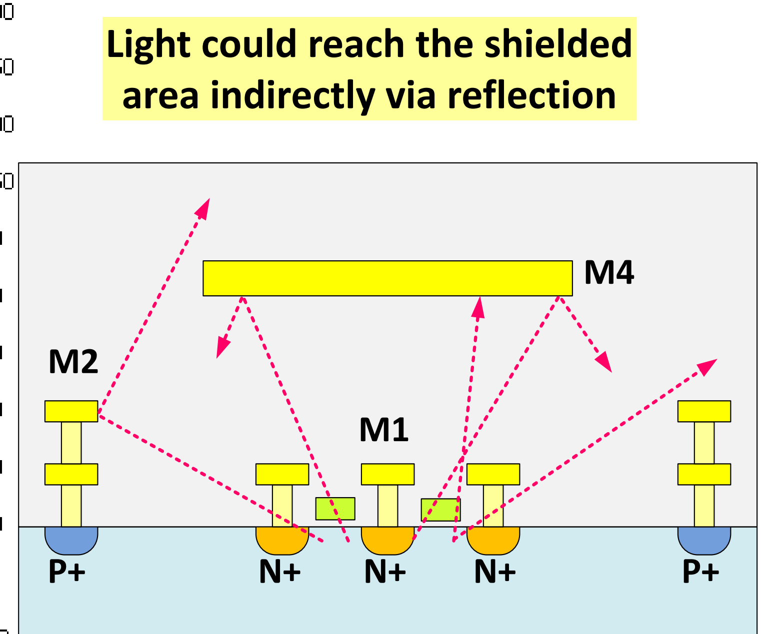


Metal Shielding & Reflection

- **The effect of combined metal shield is observed**
  - **The hot spot asymmetry reflects the metal layout asymmetry**
- **Evidence of light reflection from surrounding metal pieces**
  - **Photons are detected right on top of M4 shield**







A Note on Two Easily Confused Terms

- **"Photoemission"**
  - Emission of electrons due to light irradiation
  - Similar to "photoelectric effect"
  - Occasionally misused for "photon emission" in the literature

- **"Photon emission" or "light emission"**
  - More specifically "electroluminescence (EL)"
  - Emission of photons due to electrical stimulation
    - e.g., "hot-carrier luminescence" in MOSFETs
    - e.g., forward-biased p-n junction diodes in LEDs
  - Photon Emission Microscope (PEM, EMMI)
    - Powerful semiconductor circuit & process diagnostic tool
      - Trouble shooting junction leakage, contact spiking, floating gates, avalanche breakdown, latch-up, and oxide damage problems

Related terms
- Cathodoluminescence
- Ionoluminescence
- Chemiluminescence
- Bioluminescence
- Mechanoluminescence
- Photoluminescence
- Radioluminescence
- Thermoluminescence

Summary

- Studied the photon emission (PE) from MOSFETs in stacked CIS
- Derived & verified the point spread function
- Identified the correlation between PE and I_{sub}
- Reviewed the physical mechanism of PE
- Proposed empirical equations to model the PE
- Suggested practical metal shield design guidelines

- Potential future work
  - PE from MOSFETs under AC operations (frequency, duty cycle, etc.)
  - PE from forward-biased diodes and BJTs
  - Develop more complete design guidelines
  - Emission spectrum analysis