

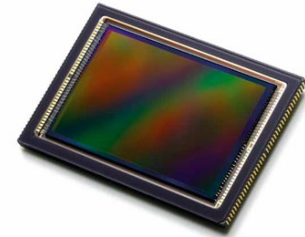
Bit-plane Processing Techniques for Low-Light, High Speed Imaging with a SPAD-based QIS

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SPAD image sensors offer:

High sensitivity

High speed



**Logarithmic
compression**

**Negligible
readout
noise**

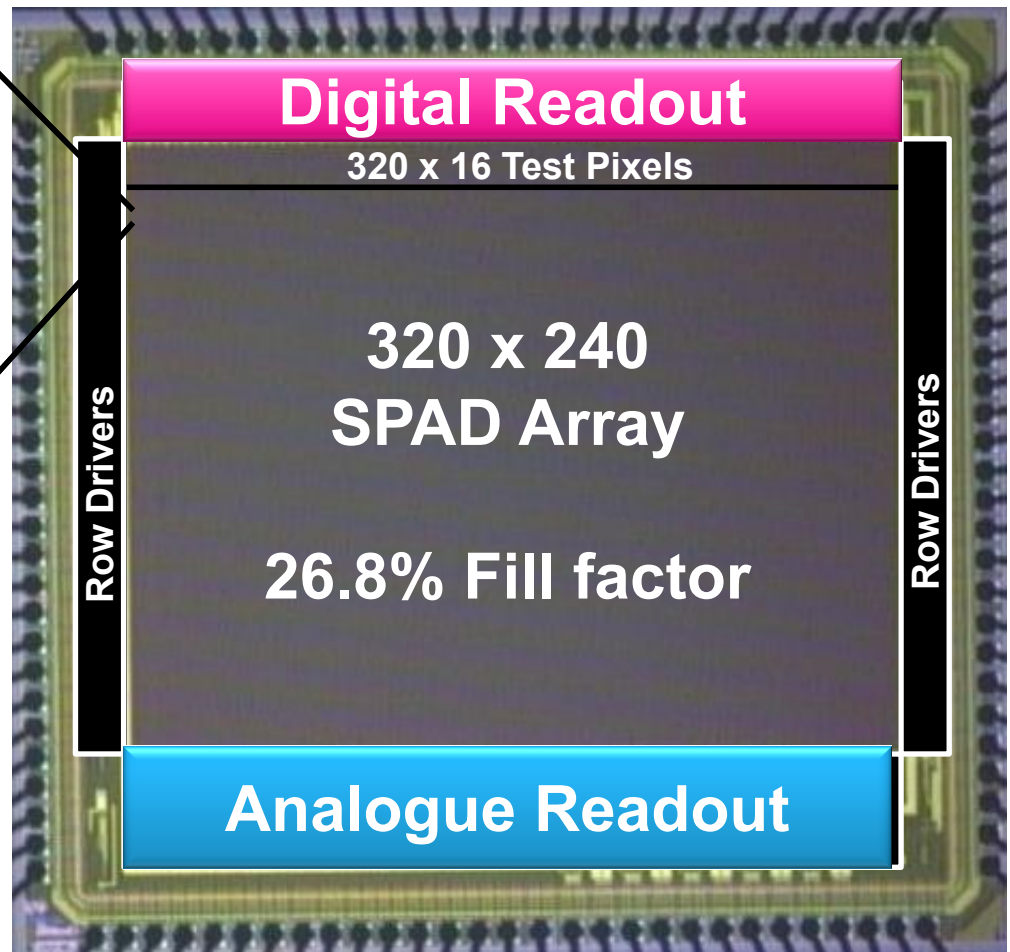
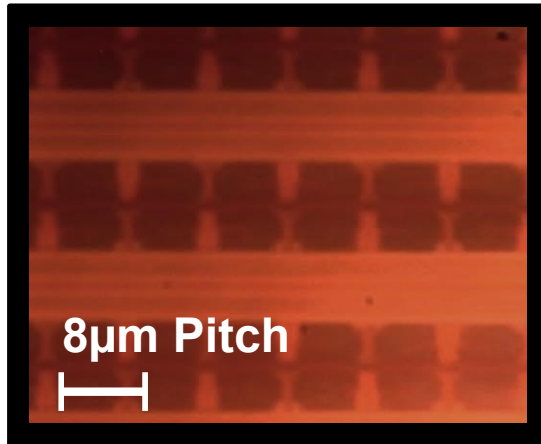
**Novel image
processing**

**QIS
mode**

We consider image processing schemes for:

- High speed imaging**
- Low light microscopy**

The SPCImager



3.1mm

3.4mm

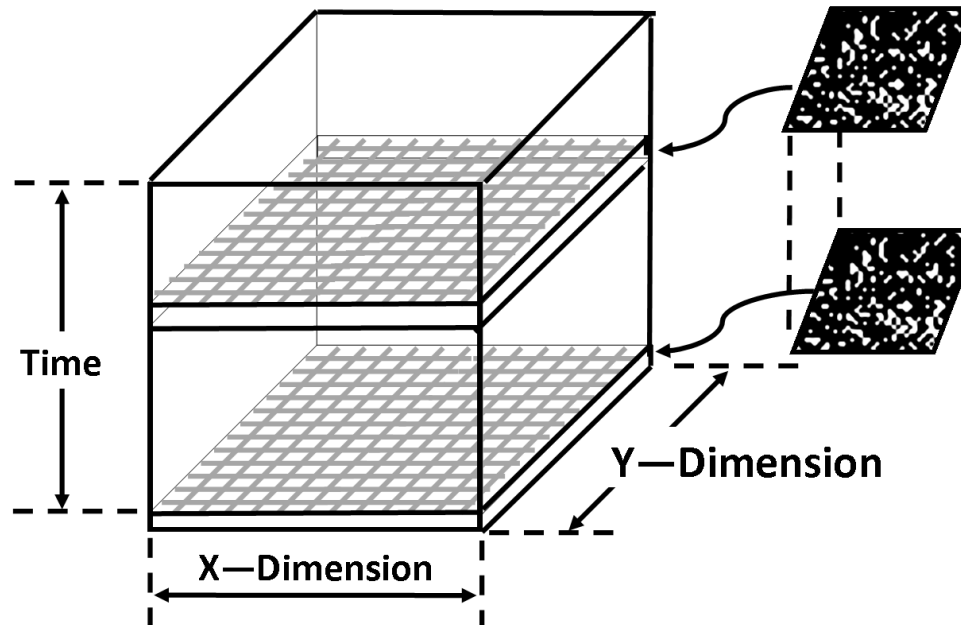
Characteristics

PDE at 450nm	35%
Median DCR	40Hz
Frame rate	10kfps

Global or rolling shutter

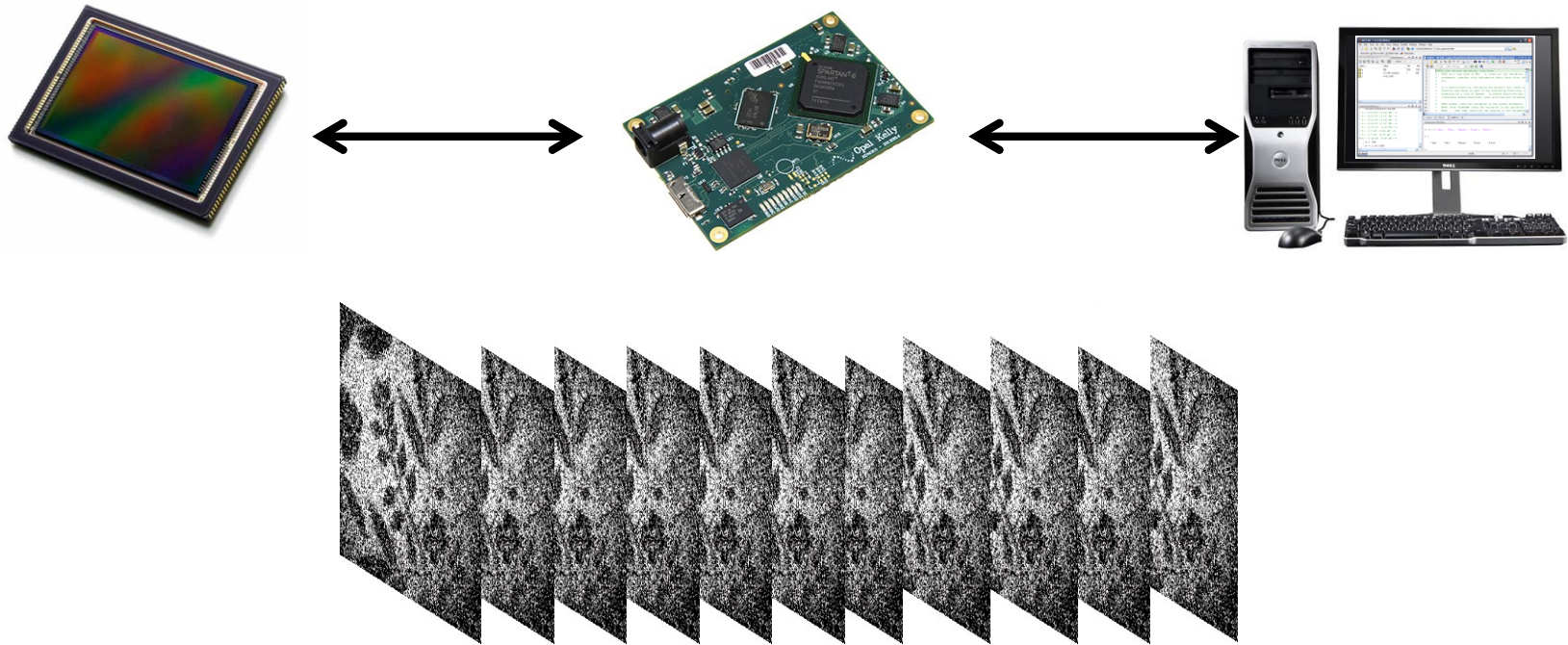
Digital mode of SPCImager

SPCImager is an implementation of the Quanta Image Sensor, i.e. a single photon oversampled binary camera



Fossum (2005) “Gigapixel Digital Film Sensor (DFS) Proposal”

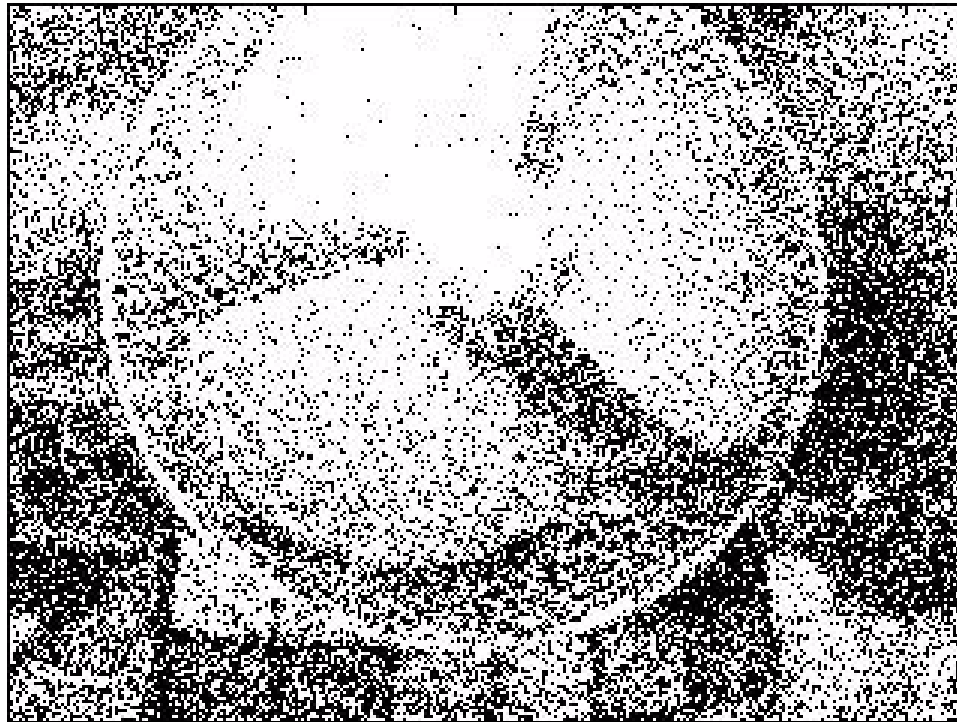
An FPGA board is used to control the capture of bit-planes and stream them to the PC over USB 3.0.



Example – Rotating fan

6

Sequence of raw bit-planes at 10kfps



(Playback at 500× slower rate)

2 μ s exposure, 100 μ s acquisition time/frame

Example – Rotating fan (II.)

7

Sum of 32 bit-planes



Fixed sum

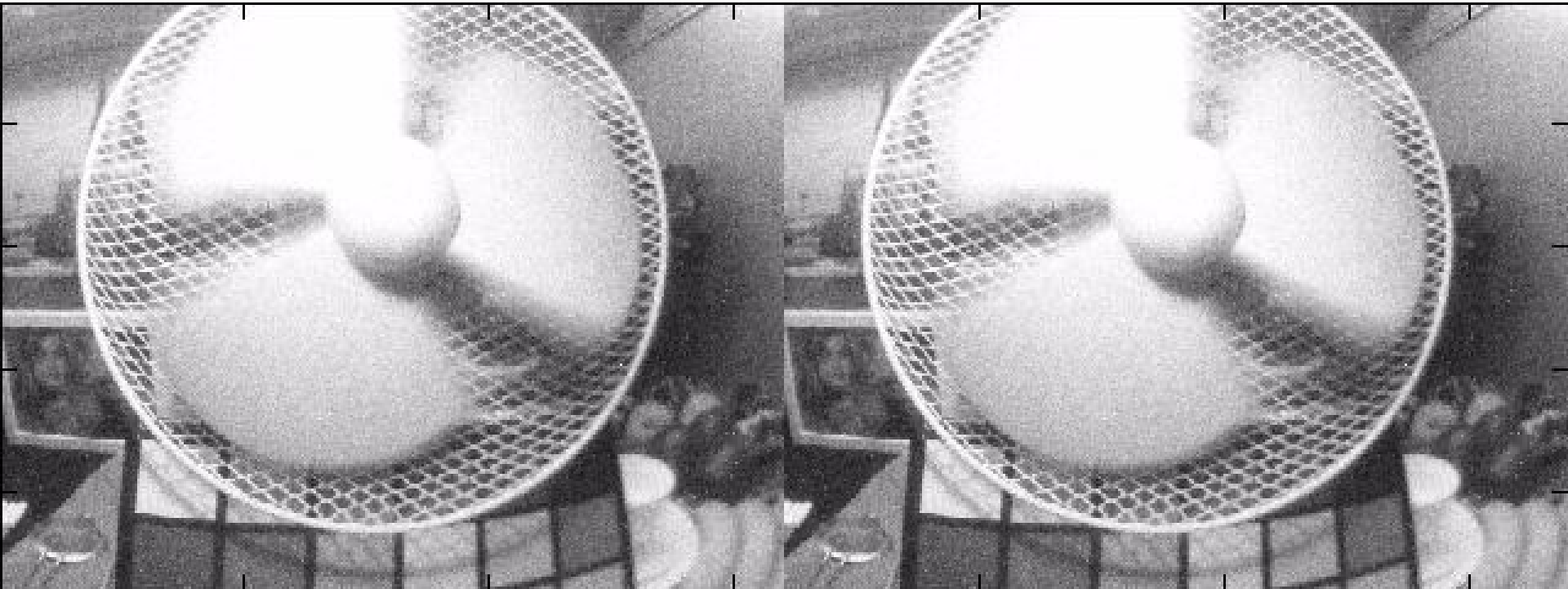
Rolling sum

64 μ s exposure, 3.2ms acquisition time/frame

Example – Rotating fan (III.)

8

Sum of 128 bit-planes



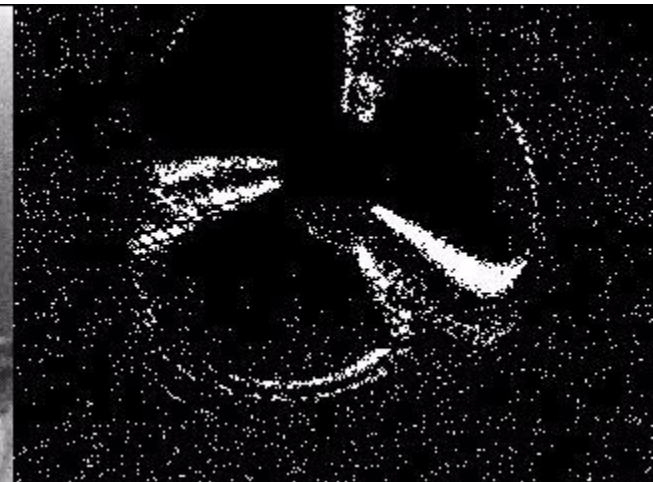
Fixed sum

Rolling sum

256 μ s exposure, 12.8ms acquisition time/frame

Example – Rotating fan (IV.)

Sum of 32/128 bit-planes



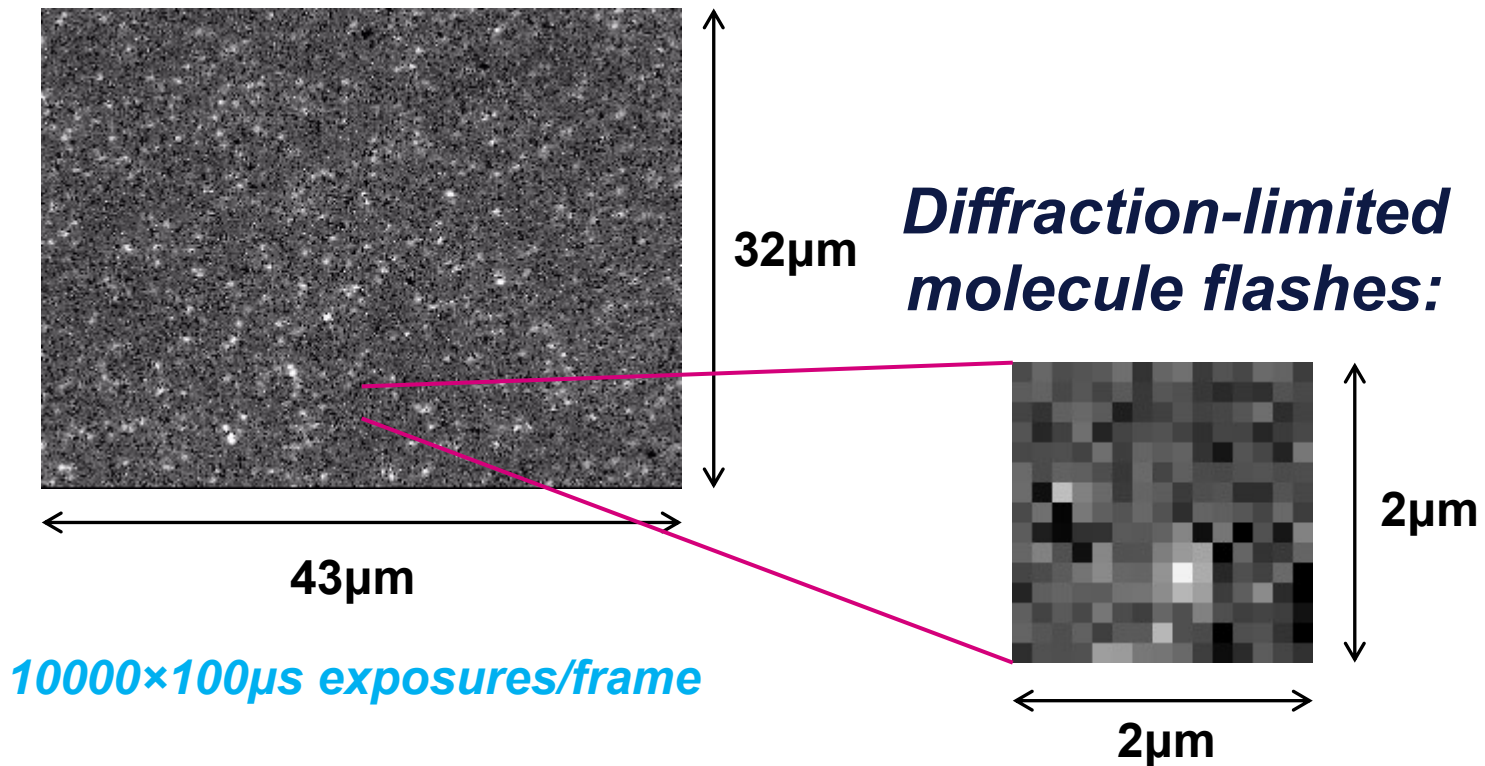
Rolling sum

Adaptive rolling sum

High var. pixels

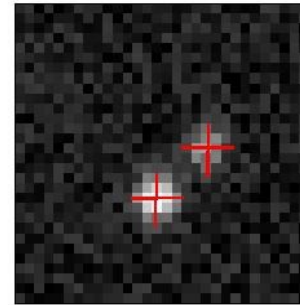
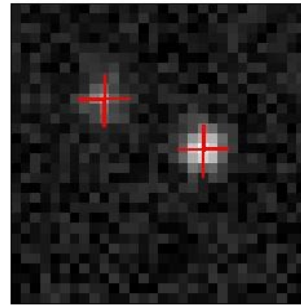
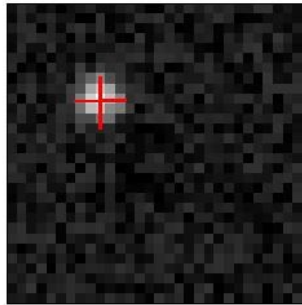
Example – Blinking molecules

Fluorescent markers (ATTO 655) used in Super-resolution Microscopy

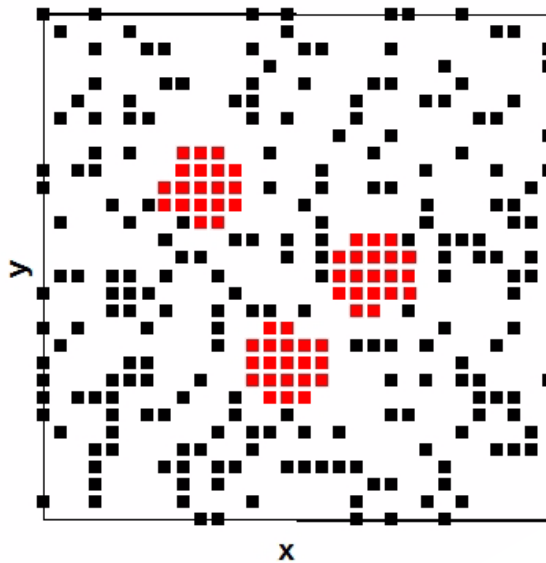


Example – Blinking molecules (II.)

Conventional IS

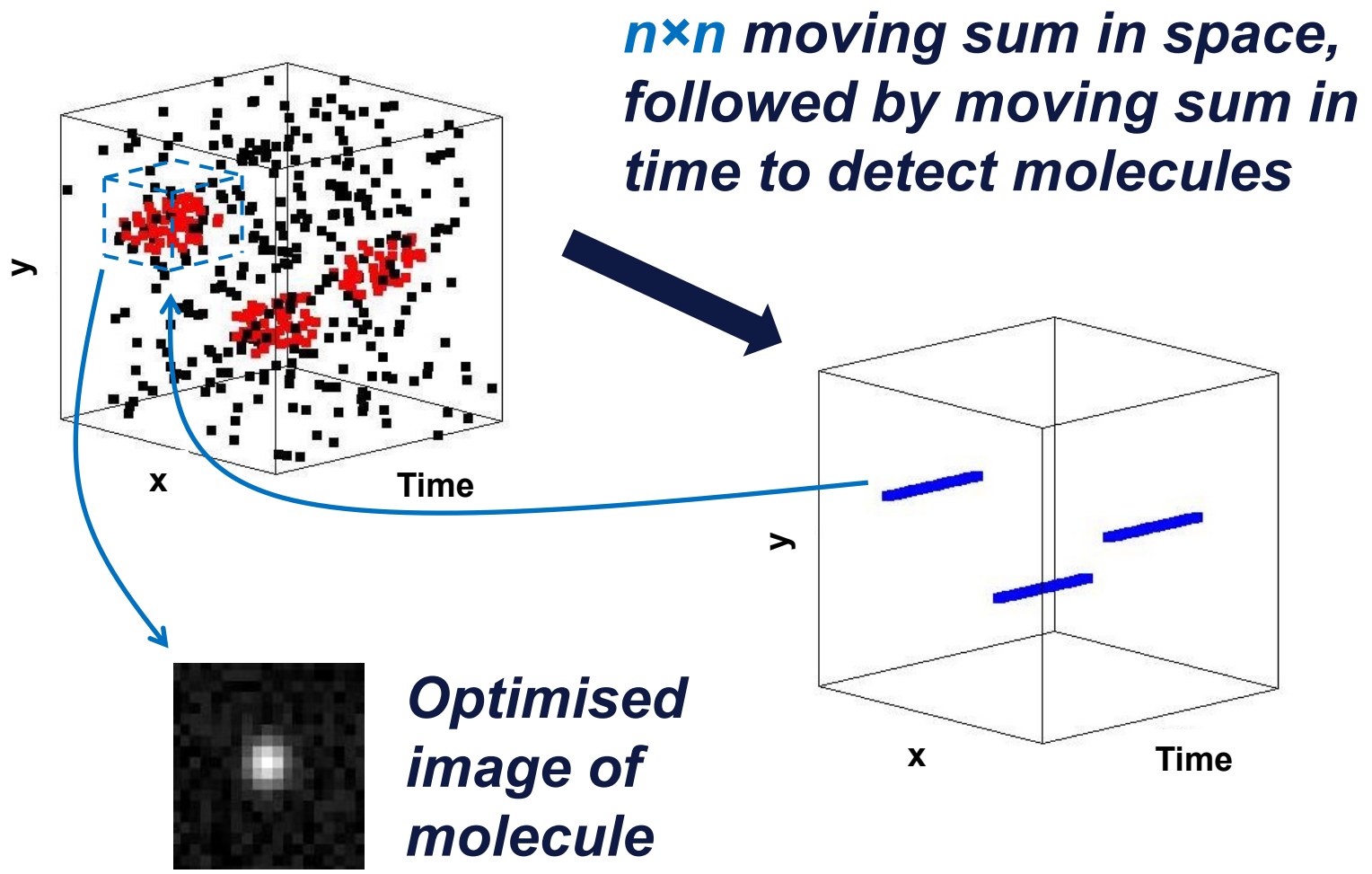


Quanta Image Sensor



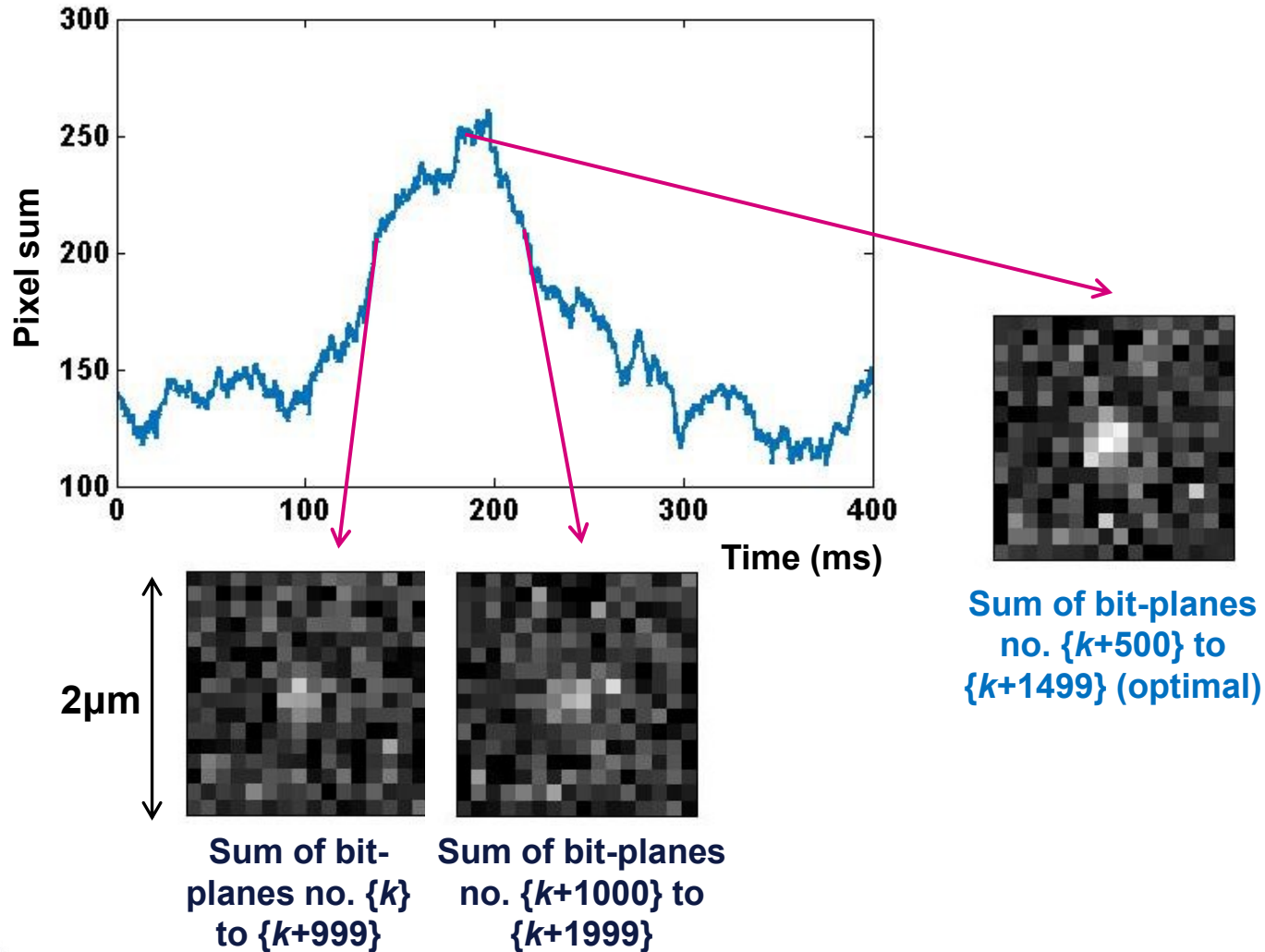
- Photon detections from molecule
- Noise/background

Example – Blinking molecules (III.)

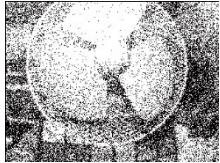


Example – Blinking molecules (IV.)

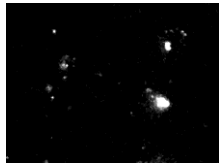
Sum of 3×3 pixel region over 1000 bit-planes



We considered two applications of a SPAD QIS:



High speed imaging



Low light microscopy

We explored the potential advantages of different bit-plane aggregation schemes.

The schemes are highly parallelisable (for an FPGA implementation) and have many possible extensions.

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