(Invited) Effect and Limitation of Pinned Photodiode

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Abstract The pinned photodiode (PPD) is the primary technology for image sensors and used in almost all CCD image sensors and CMOS image sensors. This paper discusses effect and limitation of PPD, especially dark current and electronic shuttering. Even when PPD is used and silicon surface is neutralized, proposed model explains that GR centers at the silicon surface contribute the dark current. The temperature dependence is an activation type with activation energy, E_g, not $E_g/2$. It is important to reduce GR centers for dark current reduction at PPD also. It is also noted that the vertical overflow drain (VOD) shutter combined with PPD has potential of high speed shuttering with small skew.

Keywords: image sensor, pinned photodiode, dark current, lag, noise, shutter

1. Introduction

Image sensor technologies have been advanced drastically these 4 decades, and they brought fruitful success in the market. During the image sensor developments, pinned photodiode (PPD) is one of the most valuable technologies. PPD is used in almost all charge-coupled device (CCD) image sensors and CMOS image sensors due to no image lag, low noise, low dark current, high sensitivity and realization of electric shutter [1][2]. In this paper, effects and limitations of PPD are explained. Especially, dark current reduction effect and high speed shuttering are discussed at section 3 and 4, respectively.

2. Pinned Photodiode (PPD) Structure and Effects

Figure 1 shows cross sectional view and potential profile of a PPD pixel. PPD has two important features; p^+ pinning layer and complete charge transfer.

The first distinct feature is the p^+ pinning layer over the photodiode (PD). Though there are many dark current sources, recombination-generation (GR) centers, on the silicon surface, the grounded p^+ layer protects PD from the GR centers at silicon surface. Then, low dark current is realized. Also, the pinning layer stabilizes PD electrically, which realizes large saturation and electronic shutter by the vertical overflow drain (VOD) [3]. Moreover, impurity concentration gradient in the p^+ pinning layer makes potential gradient, which moves signal electron in the p^+ pinning layer to n-type PD by fast drift motion. Then, sensitivity, especially blue sensitivity, is increased.

The second distinct feature is that signal electrons are transferred completely. In other words, the PD becomes empty after signal electrons are transferred, which achieves no image lag and no transfer noise.

3. Dark Current Reduction Mechanism and Limitation

Dark current reduction mechanism is explained using Shockley-Read-Hall Process. The recombination rate, U, is

$$U = \sigma v_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)}, \quad (1)$$

where σ is electron and hole capture cross section, v_{th} is the thermal velocity, N_t is the trap density, n_i is the intrinsic carrier density, E_t is the tarp energy level and E_i is the intrinsic Fermi level [4]. For simplicity, it is assumed E_t=E_i. If depleted, electron and hole density is much smaller than intrinsic density. The recombination rate becomes

$$U=-\sigma v_{th} N_t n_i/2. \quad (2)$$

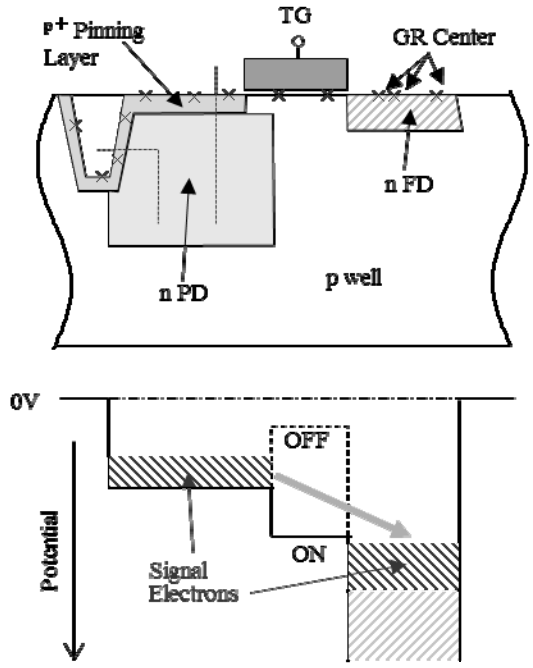

Fig. 1. Pinned photodiode structure and potential profile.

On the other hand, if not depleted due to the pinned PD, the recombination rate becomes zero.

Actually, dark current FPN is much suppressed by pinned PD, as shown in Fig. 2. The dark current FPN at her neck is much improved.

Even p^+ pinning layer neutralizes interface states, n PD is depleted nearby p^+ pinning layer. The assumption of equilibrium is not correct in a precise sense. New modified diffusion current model, having GR center, is introduced. GR centers are located at the silicon surface and STI (shallow trench isolation) surface. For simplicity, the model is one dimensional, along dot line at the pixel cross section, as shown in Fig. 1. In Fig. 3, left hand side area is p^+ pinning layer, while right hand side is n PD region. Hatched regions are neutralized while solid regions are depleted. GR centers are located at x= - x_{GR} in neutralized region. Stationary is assumed while equilibrium is not assumed. No electric field in neutralized region and low injection is assumed similarly with the derivation of the diffusion current without GR center [4].

Since GR center forces electron density n_p toward equilibrium

electron density n_{p0}, GR center effect is introduced into the equation of continuity;

$$D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} - GD_n(n_p - n_{p0})\delta(x + x_{GR}) = 0, \quad (3)$$

where D_n denotes electron diffusion constant, τ_n denotes electron life time, and G denotes intensity of GR center. The boundary conditions are the same as the derivation of the diffusion current without GR center [4];

$$n_p = n_{p0} \qquad \text{at } x = -\infty, \quad (4)$$

$$n_p = n_{p0} e^{qV/kT} \qquad \text{at } x = -x_p. \quad (5)$$

First merit of this model is that it is easy to compare this model with Sze's diffusion current model. Secondly, GR center is put at the finite distance from the depleted region.

The diffusion current with GR center, $J_n^{(GR)}$, is derived as,

$$J_n^{(GR)}(-x_p) = J_n^{(0)}(-x_p) \times EDCF, \quad (6)$$

where

$$J_n^{(0)}(-x_p) = \frac{qD_n n_{p0}}{L_n}(e^{qV/kT} - 1), \quad (7)$$

$$EDCF \equiv \frac{GL_n + 1}{GL_n + 1 - GL_n e^{-(x_{GR} - x_p)/L_n}}. \quad (8)$$

$J_n^{(0)}$ is the diffusion current without GR center, L_n is diffusion length in p^+ pinning layer [4], $\sqrt{D_n \tau_n}$. *EDCF* stands for extra dark current factor. GL_n, dimensionless parameter, indicates GR center strength. Eq. 8 clears up neutralized GR center contribution to the dark current.

The calculated *EDCF* is shown in Fig. 4. When normalized GR center position, $(x_{GR}\text{-}x_p)/L_n$, becomes larger than 2, or when GL_n is smaller than 0.2, *EDCF* tends to 1, which means GR center does not increase dark current. When $(x_{GR}\text{-}x_p)/L_n$ is zero, the GR center is not neutralized and *EDCF* increases linearly with GL_n;

$$EDCF = GL_n + 1. \quad (9)$$

When $GL_n \to \infty$, *EDCF* increases and saturates instead of diverging;

$$EDCF \to 1 \Big/ \left(1 - e^{-(x_{GR} - x_p)/L_n}\right). \quad (10)$$

Temperature dependence of Eq. 9 is an activation type with activation energy, $E_g/2$, through G, where E_g is the band gap energy. On the other hand, Eq. 10 depends a little on temperature only through L_n. Therefore, $J_n^{(GR)}$ has the same temperature dependence as $J_n^{(0)}$, which has an activation type. The activation energy is E_g, not $E_g/2$.

To decrease dark current, GR centers should be reduced even they are neutralized, and thickness and density of p^+ pinning layer should be well designed.

One approach to reduce GR centers is SITless isolation [5]. No isolation grooves or ridges and no substrate etching like STI are used. Just p^+ region is used for the isolation in a pixel. The other approach is an atomically flattening method [6]. Atomically flat surface is prepared just before oxide formation. Dark current reduction is realized by both approaches.

4. VOD (Vertical Overflow Drain) Shutter

High speed shutter possibility of VOD shutter is explained in this section. Here, definition of high speed shutter is that exposure time is very short, while definition of high speed camera is that frame rate is very large. Therefore, high speed camera needs high speed shutter, but the definitions are different. High speed cameras have been developed eagerly in Japan and 20 Mfps is realized [7, 8].

Shutter time is limited by following factors;

(1) The time while photo generated carriers are moved to the storage region in the photodiode.

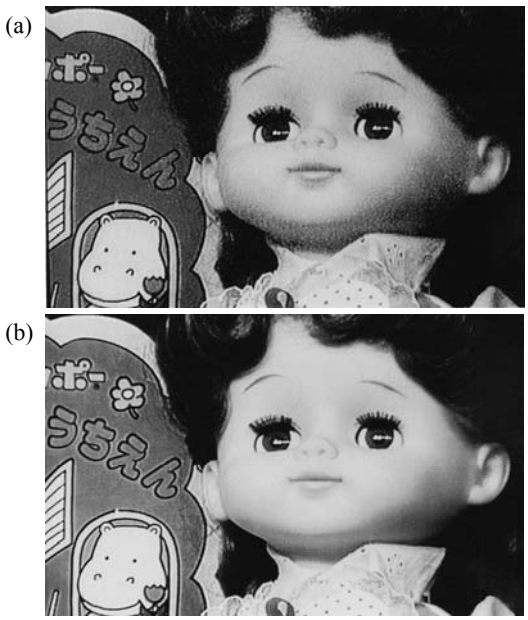

Fig. 2. Dark current FPN improvement by pinned PD. (a) is by conventional PD while (b) is by pinned PD.

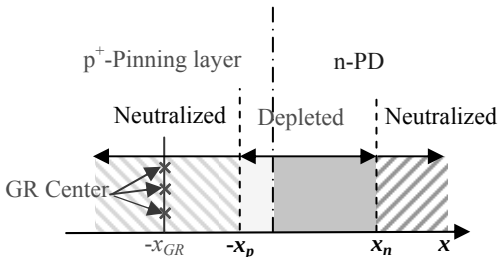

Fig. 3. New diffusion dark current model. GR centers are located in p^+ pinning layer.

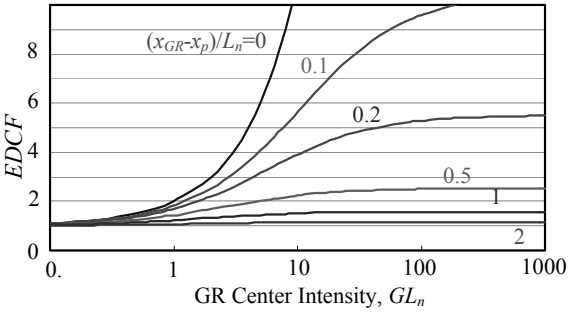

Fig. 4. Result of new diffusion dark current model.

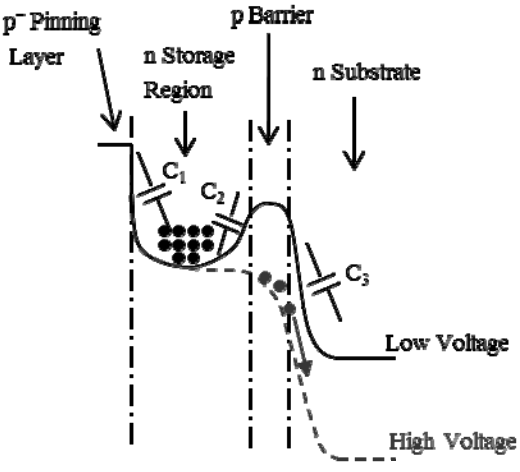

Fig.5. PPD potential profile in depth direction to explain VOD shutter motion.

(2) The delivering time of driving pulses, which is determined by (load capacitance) x (driver output impedance + parasitic resistance). VOD shutter can reduce parasitic resistance and realize small skew among pixels.

Figure 5 shows the PD potential profile in the depth direction to explain VOD shutter motion. There are p^+ pinning layer, n storage region, p barrier, and n substrate from the silicon surface. At the storing mode, low voltage is applied at n substrate. Then, potential barrier is formed between n storage region and n substrate, and signal electrons are stored at n storage region. At the shuttering mode, such high voltage is applied at n substrate that the potential barrier is disappeared and all photo generated electrons are drained into the n substrate. The n substrate voltage controls shuttering motion.

According to simple model by series of 3 capacitors, as shown in Fig. 5, dependence of barrier height, V_B, on n substrate voltage, V_{Sub}, becomes,

$$\Delta V_B = -\frac{C_1 C_3}{C_2 C_3 + C_3 C_1 + C_1 C_2} \Delta V_{Sub} \qquad (11)$$

To reduce *Vsub* swing for shuttering, larger C_1 and C_3 and smaller C_2 are needed. The p^+ pinning layer much increases C_1, and large C_1 stabilizes n storage region potential. Thanks for PPD, VOD shutter with practical voltage is realized, and almost all CCD image sensors adopt it.

Pulse skew, a big issue for high speed shuttering, can be resolved by VOD shuttering, because the shutter pulse can be applied not through wiring but through backside. Parasitic resistance itself is small and parasitic resistance variation in entire image area is also small. Less than 200 ps skew in entire image area was reported [9].

5. Conclusion

PPD is the primary technology for image sensors and used in almost all CCD image sensors and CMOS image sensors. PPD realizes no image lag, low noise, low dark current, high sensitivity and electric shuttering.

Though PPD reduces dark current drastically, there still remains dark current. The new modified diffusion dark current model for GR center in p^+ pinning layer is proposed. Even when GR centers are neutralized, they contribute to diffusion dark current. The temperature dependence is $J_n^{(GR)} \propto e^{E_g/kT}$. GR centers should be reduced even they are neutralized, and p^+ pinning layer should be well designed. Both macroscopically and atomically flatness of silicon surface reduces dark current.

VOD shutter with PPD has possibility of high speed and small skew, because the shutter pulse is applied from the backside, which has low parasitic resistance and low parasitic resistance variation. Actually, less than 200 ps skew was reported.

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* Part of this paper was presented by N. Teranishi, “Dark Current and White Blemish”, Image Sensors 2012, London,, March, 2012, and N. Teranishi, “Dark Current and White Blemish in Image Sensors”, 2013 VLSI-TSA Symposium, April 24, 2013.

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