Column-Parallel Oversampled ADCs for High Performance CMOS Image Sensors

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Abstract In this paper, the operation of column-parallel oversampled ADCs for CMOS imager is reviewed and several implementations are described. Both architectural and circuit level innovations are explained for practical column-parallel implementations and prototype implementations are described. Because of their multiple sampling nature, such column-parallel oversampled ADCs have also been investigated for high performance imagers, e.g. low-light level imaging and compressed sensing. Finally, several extensions of column-parallel oversampled ADCs are briefly discussed.

Keywords: Column-parallel oversampled ADC, CMOS image sensor, high-speed imaging, low-light level imaging, compressed sensing

1. Introduction

A column-parallel ADC architecture provides a good trade-off among frame rate, the number of columns, noise performance and power consumption, and thus it has been widely used in CMOS image sensors. Several column-parallel ADCs have been extensively investigated, such as single-slope ADC, cyclic ADC, SAR ADC, and ΔΣ ADC. Each ADC architecture imposes unique features, and thus architectural level understanding is essential for target imaging applications. Although the ΔΣ ADC could provide high resolution with less accurate analog components, column-parallel integrations were not widely used because of the complexity of ΔΣ modulator and following decimation filter. However, the recent advance of architectural and circuit level innovations make the architecture feasible and open up many different possibilities [1].

The paper is organized as follows. Section 2 reviews column-parallel oversampled ADCs. Section 3 describes key innovative aspects for the ADC implementations. Finally, extension and outlook are briefly discussed in Section 4.

2. Column-Parallel Oversampled ADCs

A. Oversampled ADC

Sensor applications typically require ADCs with both high absolute accuracy and high resolution [2]. Since the input signals are near DC, such ADCs must be robust to offset and flicker noise, also required for imaging applications. Unlike Nyquist ADCs, oversampled ΔΣ ADCs, by utilizing over-sampling and noise-shaping, can achieve high resolution without relying on component matching property and so can achieve better energy efficiency without the help of calibration, especially, when 12b+ resolution required. For sensor applications, such ADCs usually operate in incremental mode, in which they are first reset and then operate for a fixed number of cycles.

B. First-Order ΔΣ ADC

Earlier work described the operation of the first-order ΔΣ ADC in incremental mode, which includes the first-order switched-capacitor (SC) loop filter, and a counter for digital decimation filter, resulting in 16 bit resolution, 12 μV offset, and 1 second conversion time [3]. Because of this low complexity, the first-order incremental ΔΣ ADC had been applied for column-parallel ADCs of CMOS imagers [4]. However, it has several drawbacks. The first-order converter requires 2^N cycles for N-bit resolution leading to a long conversion time and thus resulting in poor energy-efficiency. Moreover, it suffers severe limited cycles for DC input and the finite DC-gain of an integrator also causes limited cycles. To avoid such problems, high DC-gain is required for its loop filter implementation, which is not desirable for column-parallel integration.

C. High-Order ΔΣ ADC

To achieve a reduced conversion time, higher-order incremental ΔΣ ADC was proposed by using MASH architecture. A MASH 1-1 implementation was used in [5] and had been adopted in column-parallel ADCs [6]. However, it imposes stringent requirements of loop filter implementation to avoid limited cycle issue as the first-order ADC. The use of single-loop topology circumvents the issue, and several implementations result in 20 bit resolution with reduced conversion time [7]. A single-loop second-order ΔΣ ADC was introduced for fully-integrated column-parallel ADCs, which result in 2.1M pixel, 120 fps CMOS imager [1]. Within a 4.5μm column-pitch, a compact ΔΣ ADC employing a compact low-power modulator and a matched decimation filter with digital CDS functionality. The prototype imager presented the temporal noise level of 2.4e- and a dynamic range of 73dB, achieving the state-of-the-art energy-efficiency of 1.7e-·nJ. This approach has been extended to third–order implementation for the further reduction of conversion time and verified with 1000 column-parallel ADCs [8].

D. Extended Counting ADC

Alternative approach to achieve a reduced conversion time is the extended-counting ADC, in which the residue of a coarse ΔΣ ADC is digitized by a fine Nyquist ADC [9]. This two-step approach can be energy-efficient, because the resolution requirement of ΔΣ ADC is relaxed by the fast Nyquist ADC. The first or second-order extended-counting ADCs were implemented and achieved good energy-efficiencies. Such an advantage is still valid for CMOS imagers, since the coarse ΔΣ ADC samples input signal for multiple times, which reduces input noise without suffering dynamic range reduction, and the fine Nyquist ADC manages the level of quantization noise. Column-parallel extended-counting ADCs with a coarse first-order ΔΣ ADC and a fine cyclic ADC were implemented for low-light level imaging [10]. The prototype 1Mpixel imager demonstrated the very low temporal noise of 1.2e- and a wide dynamic range of 82dB. An

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alternative prototype achieved 24 Mpixel 10.2 fps with 14 bit resolution [11].

3. ADC Implementation

A. Inverter-based ΔΣ Modulator

Since the operational amplifier consumes considerable area and power, a logic inverter can be used for the column-parallel implementation of ΔΣ modulator [1]. Since the offset voltage of an inverter is sensitive to PVT variations, a dynamic offset cancellation technique is also applied [12]. Both PMOS and NMOS of an inverter contribute to g_m while sharing the same supply current. As a result, the intrinsic current efficiency becomes double. In addition, the inverter behaves as a class-AB amplifier and thus large driving current can be obtained with less quiescent current. Inverter-based ΔΣ modulators achieved state-of-the-art ADC FoMs of 50-300 fJ/steps with 12-20 bit resolutions [1], [2], [8], [13]-[14]. For CMOS imager, a 13-bit ΔΣ modulator was implemented within the area of 4.5μm × 300μm, which was comparable to the area of single-slope ADC. The inherent PVT variations of an inverter often limits its performance, but recently several techniques have been successfully demonstrated to address this issue by adjusting supply voltage [8] or body voltage [13] or by using capacitive biasing from current source [14]. This progress makes the inverter-based ΔΣ modulators more visible for its column-parallel integration. Because of multiple sampling effect, the required first sampling capacitor of a ΔΣ ADC is much smaller than that of a Nyquist ADC, which is also important advantage especially targeted for high resolutions (>12bit).

B. Decimation Filter

The decimation filter decodes the modulator's bit-stream and produces a digital value. A sinc-type filter is commonly used for the decimation filter, but this is not essential for an incremental operation because of the static input (no needs to be linear phase). Therefore, a decimation filter composed of integrators with the same orders of the modulator, so called matched filter, is sufficient. A second-order matched filter was implemented with a ripple counter for the first integrator and an accumulator for the second integrator [1], whose weight coefficient of the filter corresponds to a triangular shape. The overall TR counts of the second-order matched filter were 320 for 14-bit decimation, which only occupied the area of 4.5μm × 300μm including 14-bit SRAM bank in a 0.13μm CMOS technology. Therefore, the area burden of digital decimation filter would become negligible w.r.t. process scaling.

4. Extension and Outlook

The column-parallel implementation of ΔΣ ADC has been further investigated for compressed sensing (CS). To reduce the ADC sampling rate, the conventional CS requires an additional analog-processing. However, this CS can be performed within the column-parallel ΔΣ ADCs due to the decimation filter's post-processing ability [15]. A prototype with the first-order column-parallel ΔΣ ADC demonstrated that the compression ratio of 1/4, 1/8, or 1/16 was achieved without any additional hardware penalty and in turn the frame rate of the imager was boosted without extra power increase. The column-parallel ΔΣ ADCs have also been applied for the readout-IC of a capacitive touch-screen panel [16]. The ADC architecture was adopted from [1], and the prototype readout-IC achieved a 60dB SNR with 200 Hz frame rate and improved noise immunity.

Due to multiple sampling, noise shaping and digital post filtering, the column-parallel oversampled ADC can provide superior noise performance over other approaches and thus can be applicable to high performance CMOS imagers as well as various array-type sensors.

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