Column parallel SS-ADC with TDC using multi-phase clock signals for CMOS imagers

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Abstract We propose a single-slop ADC with a time to digital converter (TDC) that uses a multi-phase clock. When the TDC with resolution of n bits is adapted to the ADC, the conversion time is reduced by a factor of 2^n. Applying the TDC that uses multi-phase-clock signal reduced the number of circuit elements, achieved consistency between the single-slope ADC and the TDC, and realized robust meta-stability.

Keywords: single-slop ADC, TDC, multi-phase-clock signal, meta-stability

1. Introduction

A single-slope ADC is the simplest and the smallest ADC and is widely used for column parallel ADC of the CMOS imager. When a ramp signal and an analog one are given to the comparator, the comparator generates a PWM signal. Counting the high-time of the PWM signal by a clock signal, the analog signal is digitized. The problem for the single-slope ADC is operation speed. In the single-slope ADC, whenever the accuracy of the ADC doubles, so does the operation time. Therefore, realizing multi-stage ADC by using multi-ramp signal and generating a high-speed-clock signal in the sensor chip has been proposed to solve this issue[1], [2], [3], [4]. However, the multi-ramp signal generator required complicated control and digital calibration for consistency between ADC stages. In this study, focusing on a quantization error of the single-slope ADC, we developed an effective multi-stage-single-slope one.

2. Structure of proposed ADC

Figure 1 shows a block diagram of the proposed ADC configuration. The ADC has two stages. The first is the 4-bit TDC with multi-phase clock signals, and the second is a single-slope ADC with a 8-bit ripple counter. The comparator of the single-slope ADC generates the quantization error between the outputted PWM signal and the clock signal. The quantization error is given to the TDC, and the error period between the risings of signals is digitized. Therefore, the TDC measures the quantization error of the single-slope ADC (Fig.2).

The TDC consists of 8 D-FFs, a 4-bit ripple counter and some logic gates. Using the 4-bit ripple counter, the counter can handle a 4-bit encoded word. The encoded word is required for a correlated double sampling (CDS) operation. The proposed TDC uses the special thermo-code. When the master clock period is denoted as T_c, our 4-bit-TDC codes are those given in Fig. 3.

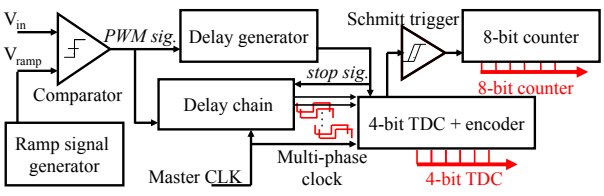

Fig. 1. Block diagram of proposed ADC.

The code denotes the time shift of the multi-phase clock. The conventional thermo-code, which is used for the delay-line TDC, is not applied to the proposed circuit. Therefore, considering the 4-bit-resolution, the compact TDC with 8 D-FFs can be achieved. The proposed circuit has fewer than half the D-FFs the delay-line TDC has.

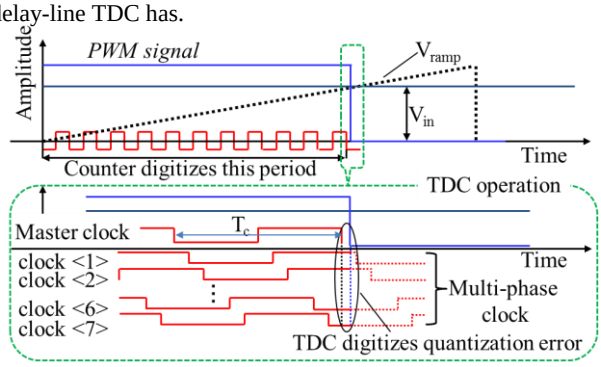

Fig. 2. Operation of proposed ADC.

code	Tdelay	Digital
1000 0000	0/16 Tclk	0000
1100 0000	1/16 Tclk	0001
1110 0000	2/16 Tclk	0010
1111 0000	3/16 Tclk	0011
1111 1000	4/16 Tclk	0100
⋮		
0000 0011	13/16 Tclk	1101
0000 0001	14/16 Tclk	1110
0000 0000	15/16 Tclk	1111

Encoder

Fig. 3. TDC code of proposed TDC.

3. Consistency of proposed ADC

To achieve the consistency between lower and upper bits in the multi-stage ADC, the master clock which is inputted to the first D-FF of the TDC is distributed from the D-latch in the D-FF and lead to the LSB D-FF of the ripple counter (in Fig. 1). Moreover, to prevent miscounting due to the D-latch meta-stability, the distributed signal master clk transmits thorough the Schmitt trigger. When the master clk value is hold as D-

latch_clk in the D-latch of the first D-FF, the Schmitt-trigger-output signal D-latch_clk simultaneously stops At that time, steady-state of the D-latch_clk and the master clk have same value. Also predefined multi-phase clocks clock<1:7> are provided from the common DLL to the remaining seven D-FFs of the TDC. Therefore, the consistency between the first D-FF of the TDC and the LSB D-FF of the ripple counter can be achieved. When the meta-stability occurs in the first D-FF of the TDC, two conditions are considered. First, in the D-latch_clk falling slowly, since the ripple counter is the following stage, the counter does only slow stopping, and the miscount doesn't occur. Second, when the D-latch_clk falls to the intermediate state and rises, the signal form is distorted and the miscount may occur. However, using Schmitt trigger, the signal distortion is stabilized and the miscount can be prevented. A stand-alone single-slope ADC with a delay-line TDC has been proposed for low voltage use [5]. An additional circuit was required for delay adjustment of the meta-stability. Moreover, since there is no consistency between the ADC and the TDC, digital calibration was also needed.

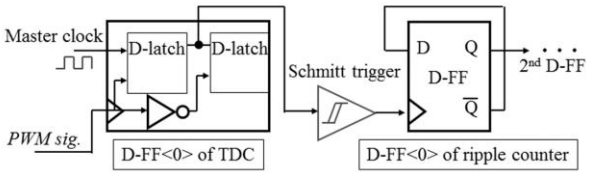

Fig. 4. Shared clock signal.

4. Simulation and measurement results

Figure 5 shows a transient characteristic of the metastability. When the input signal and the stop signal approach, large delay generation and signal distortion were confirmed. However, through the Schmitt-trigger, the D-latch output was stabilized. Figure 6 shows circuit delay with the metastability.

The delay time of our circuit was less than 1.6 ns. Before passing through the Schmitt-trigger, both rising and falling delays occurred. However, after passing, the delay with half falling and the rising (region of > 4.52 ns) was suppressed because the Schmitt-trigger stabilizes the D-latch output. In our ADC, the simple falling delay (region of · 4.52 ns) has no effect for the miscounting. Figure 7 shows measured correct operation percentage. We configured the proposed TDC by discrete ICs, and measured 50 times a point. The proposed TDC with the Schmitt-trigger performed 100% correct operation.

5. Conclusion

We propose a single-slope ADC with time to digital converter (TDC) that uses multi-phase clock. Applying the TDC that uses a multi-phase-clock signal reduced the number of circuit elements, achieved consistency between the single slope ADC and the TDC, and realized robust meta-stability.

References

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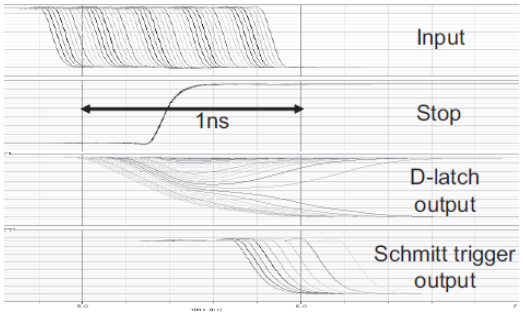

Fig. 5. Transient characteristic of meta-stability.

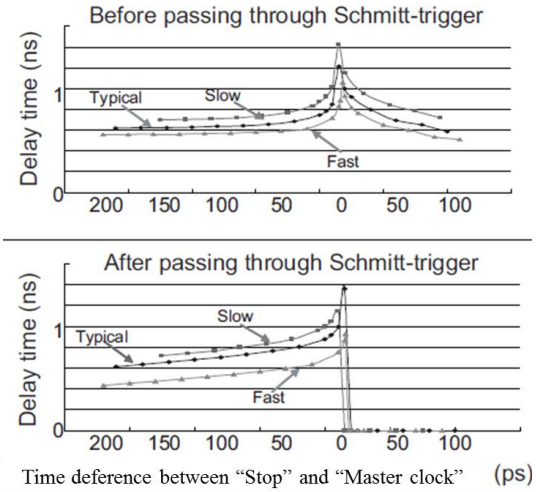

Fig. 6. Circuit delay with meta-stability.

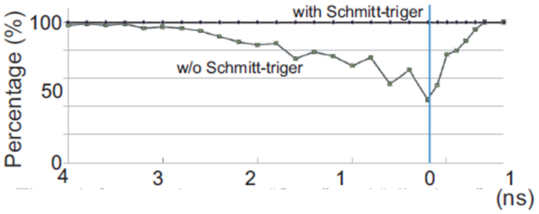

Fig. 7. Measured correct operation percentage.

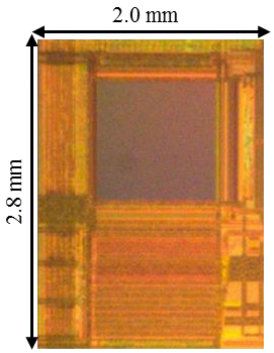

Fig. 8. Chip micrograph.

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