# [Invited]　Ultra low voltage and low power mixed-signal circuits

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**Abstract**　This paper presents ultra-low voltage (lower than 0.5V) and low power (sub-microwatt operation) data converter techniques. For applications such as sensor nodes and medical implantable devices, power scalability at wide frequency range is very important. Systematic approaches to reduce the power consumption at middle frequency range, to improve the maximum operating frequency, and to reduce the leakage power at low frequency ranges are introduced.

**Keywords:** Ultra low voltage, Ultra low power, Successive approximation, Power scalable, ADC

## 1. Introduction

Ultra low voltage and low power circuits becomes more and more important for such application of wireless sensor networks or medical implantable devices. Small size energy harvesting devices usually require the sensor nodes or medical implantable devices to operate at lower than 0.5V and in microwatt range. Power scalability is another important characteristic, because the required signal bandwidth strongly depends on the target applications.

ADC is one of the most important building blocks which digitize the sensed signal such as the temperature, light intensity, humidity, or sound. The charge redistribution type SAR-ADC uses relatively simple architecture and suited for energy efficient operation [1-3]. However, various kind of issues should be solved if the SAR-ADCs are used at ultra-low voltage.

In this paper, systematic approaches to improve the energy efficiency of ultra-low voltage SAR-ADCs in wide frequency range are introduced.

## 2. Issues in ultra-low voltage, power scalable ADC

As shown in Fig.1, energy efficiency of the ultra-low voltage SAR-ADC is limited by several factors. In the charge redistribution SAR-ADC, the power consumption is mainly determined by the capacitance value. If the capacitance value can be reduced, the power consumption can be decreased toward the direction “1” in Fig.1. The maximum sampling frequency is severely restricted because the gate overdrive of MOSFET becomes very small at ultra-low voltage operation. Therefore, speed enhancement techniques are desired to improve the power scalable range toward the direction “2” in Fig.1. At low frequency range, leakage power dominates the total power consumption, which limits the minimum level of power consumption. Leakage reduction techniques are required to improve the energy efficiency toward the direction “3” in Fig.1.

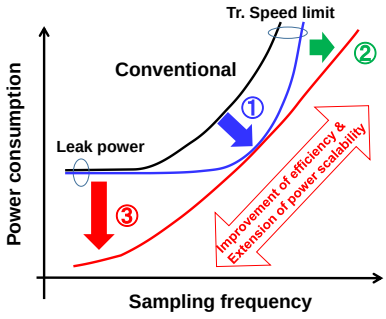


Fig. 1. Approaches to improve the enegy efficieny in wide frequency range.

## 3. Energy efficiency improvement techniques in SAR-ADC

SAR-ADC with tri-level comparator can halves the size of the internal charge redistribution capacitor DAC (Fig.2). In our previous reported work [4], meta-stability in a comparator is used to realize a tri-level detection. If the input differential voltage of the comparator becomes small, it takes a long time until the comparator output is decided. By detecting the duration time of the meta-stable state, one can judge whether the input signal is smaller than a certain level ($-\varepsilon < V_{in} < +\varepsilon$) or not. If the $\varepsilon$ is chosen as half of the LSB, the effective number of bits (ENOB) can be improved by one bit. This reduces the number of capacitors in DAC and therefore reduces the power consumption.

Combined with a digital self-calibration technique of internal DAC, test chip fabricated by 40nm-CMOS process has achieved energy efficiency of 6.3fJ/conv.-step and 0.5bit resolution improvement by tri-revel comparator.

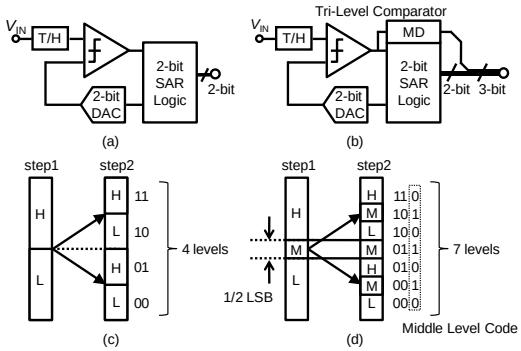


Fig. 2. Resolution improvement by tri-level compartor.

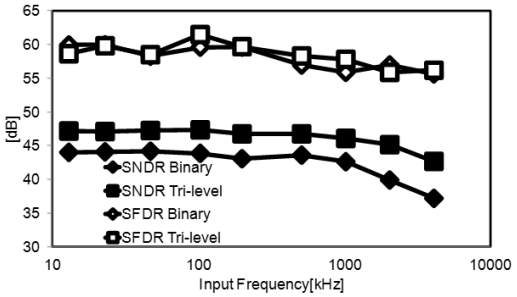


Fig. 3. Experimental results of SNDR and SFDR of fabricated test chip in 40-nm CMOS.

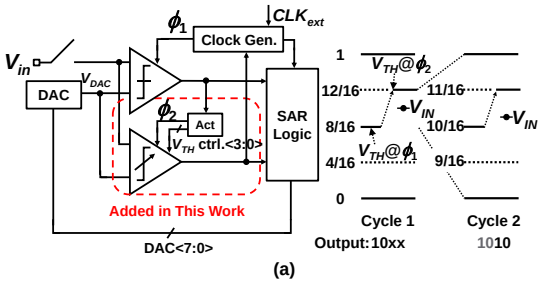


Fig. 4. 2bit/step SAR-ADC with dainamic threshold configureing comparator.

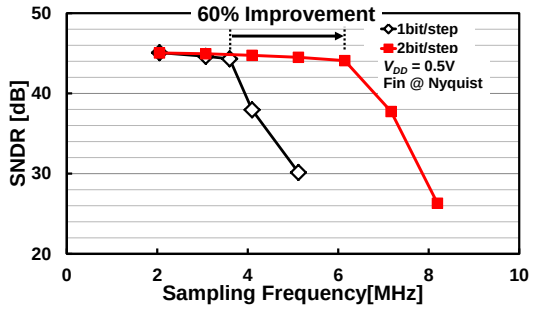


Fig. 5. Experimental results of speed improvement by 2bit/step.

To increase the maximum sampling frequency of SAR-ADC, multi-bit/step technique is often used [5]. To reduce the circuit area and power consumption in 2bit/step, we have reported a technique to use a dynamic threshold configuring comparator [6]. In the proposed technique (Fig.4), after the external clock (CLKext) sets down, successive approximation (SA) cycle 1 starts by rising $\phi_1$ and the first comparator with fixed threshold decides the first bit (MSB). After the first bit decision, the threshold voltage of the threshold configuring comparator ($V_{TH}$) is set depending on the result of the first bit. In this case, $V_{TH}$ is set to 3/4, and then $\phi_2$ is asserted and second bit is decided. Therefore, 2bit result is acquired in a single cycle. By repeating the same procedure, the ADC achieves 8bit conversion with 4 SA-cycles. Test chip fabricated in 40-nm CMOS has achieved 60% speed improvement by dynamic threshold configuring 2step/bit technique (Fig.5).

Leakage power is severe problem of advanced CMOS technology. In digital circuits, power gating is often used to reduce the leakage power. Same kind of technique can also be used for ADC [7]. However, the on resistance of power switch becomes very large and degrade the performance of the ADC if the power supply voltage is around 0.5V, because the high Vth MOSFET should be used for power switch. In our previous reported power gating technique [8], the control voltage of power switch is self-boosted to reduce the on-resistance. As shown in Fig. 6, the ADC consists of Wakeup and Sample ("WaS") logic, bootstrapped S/H circuit, asynchronous clock generator, comparator, DAC, SAR logic, clock boosting (CB) circuit, power gating switches, and output registers (D-FFs). Internal clock and control signal for power gating are automatically generated and conversion-cycle level self-power gating is realized. As shown in Fig.7, 98% leakage power reduction has been achieved at low frequency. The test chip demonstrated 650pW operation at 0.5V power supply.

## 4. Conclusion

The energy improvement techniques have been introduced. Each techniques can be combined to realize a power scalability in wide frequency range.

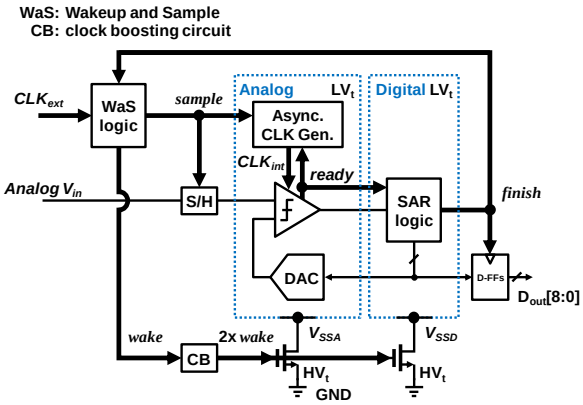


Fig. 6. Self-power gating technique to reduce leakage power.

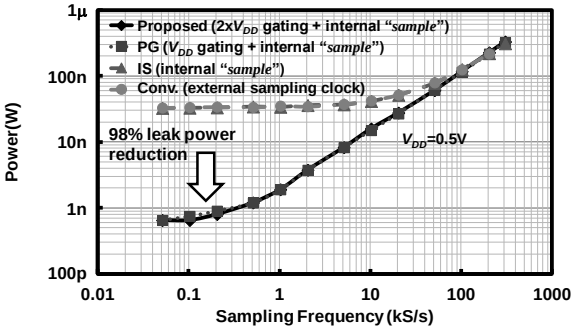


Fig. 7. Experimental results of leakage power reduction by self power gating.

## References


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