Design of Low-voltage Low-power CMOS Imager

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Abstract The demand of low-power imaging solution is urgent for emerging internet-of-things (IoT) applications. In this paper, the design challenges of low-voltage and low-power CMOS imager are investigated. Several design solutions of low-voltage operation including high dynamic range and smart function are also introduced.

Keywords: low-voltage CMOS image sensor, high dynamic range, smart image sensor

1. Introduction

Lately, developing a low-voltage and power-efficient image sensor for emerging applications in the wearable devices and internet of things (IoT) has become an important topic. The rising demand of CMOS image sensors (CIS) technology is expected to continue due to its low-power operation and high system integration property. To minimize the power consumption of CIS, low-voltage, low-leakage, and power-efficient techniques are the main design challenges.

2. Low-voltage CMOS Image Sensor

In the conventional CMOS active pixel sensor (APS) pixel, the accumulated photo-generated charge is converted to voltage and readout through a voltage buffer, which is commonly implemented by a source follower. The input-output voltage drop of source-follower reduces the available signal swing on conversion node and the full-well capacity also at a certain low supply voltage. To overcome the limited full well at ultra-low-voltage operation and extend the dynamic range, pulse-width modulation (PWM) image sensors [1-2] are reported as a proper solution. Instead of using a conventional APS pixel, the PWM sensor converts the photo-generated voltage signal into a pulse width in pixel and readout in digital form to avoid the necessary voltage headroom of an analog buffer. Consequently, the voltage-to-time domain conversion of PWM sensor efficiently avoids full-well degradation of limited signal swing at scaling down voltage operation.

The design of an in-pixel comparator is critical in PWM CIS which needs to be simple and identical. For simplicity and fill-factor concern, inverter-based comparator has been widely adopted. However, the threshold of the comparator is sensitive to process variation and results in non-uniformity of response in a pixel array. For high dynamic range CIS design, logarithmic response is one of the common implementations to approach a result of several hundred decibels. However, the SNR performance of the mentioned solutions degrades severely at low-supply operation with the limited signal swing and the weak low- light response. Dual slope response is another popular solution to extend the dynamic range by dual-exposure frames at the expense of lower frame rate, additional power, and complex following image reconstruction operation.

The previous work [1] successfully provides solutions to the mentioned design issues: 1) threshold-variation effects in PWM-based sensors, and 2) low dynamic range of circuits with low supply voltage. A 0.5V CMOS imager with threshold-variation-canceling (TVC) and programmable current-controlled threshold (PCCT) schemes are reported to achieve 0.055% fixed-pattern-noise (FPN) and 82dB dynamic range, respectively.

3. Low-voltage Smart Image Sensor with Array-Level Analog Signal Processing

Low power smart CMOS imagers are reported [3-5] to provide solutions for feature extraction and processing applications. By adopting the proposed low-voltage PWM image sensing platform, a 0.5V smart image sensor is proposed [3] with multi-operation modes of edge extraction, centroid tracking, and high-dynamic-range imaging output. The array-level analog signal processing (ASP) is implemented by local inter-pixel feedback and the event-driven (ED) hand-shaking readout. The prototype has been verified to demonstrate the features of real-time edge extraction, object tracking, and high-dynamic range imaging successfully. The measurement results show a power dissipation of 34.4uW in edge extraction mode, a frame rate of 14.28kfps and a tracking error of 0.36 pixels in centroid tracking mode, and a high dynamic range (DR) of 105dB in imaging mode.

Figure 1 shows the architecture of the proposed smart sensor, which consists of a 64x64 smart pixels array, the peripheral bias, pre-charge circuit and ED readout. The column-wise ED part includes a 64-bit handshaking arbiter tree and a 64x4-bit SRAM array for asynchronous event data storage. For power reduction and gate delay concern in 0.5V operation, a column-wise 10-bit TSPC counter is adopted for PWM HDR image output. The array-level ASP implemented by inter-pixel feedback topology is illustrated in Fig. 1. Each pixel is inter-connected with every other two of the adjacent pixels in up(U1-U2), down(D1-D2), left(L1-L2), and right(R1-R2) directions. Two smart functions have been achieved in the sensor array with ASP, i.e. (1) Edge extraction: to extract the bright object's high-contrast contour in dark background; and (2) Centroid tracking: to shrink the arbitrary shaped target in the focal plan into its centroid and track the addresses.

Fig. 2 shows the captured image comparison with and without HDR control. As shown in Fig. 2(b), the HDR operation conserves more detail than a standard PWM imager. Fig. 3 shows the re-constructed image of edge extraction mode. Fig. 3(a) is the original image pattern and Fig. 3(b) shows the

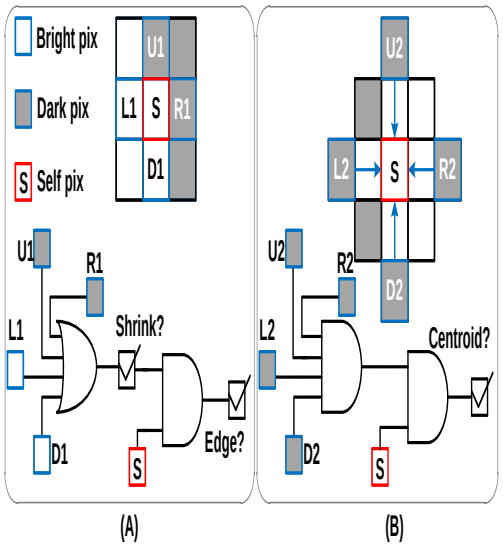

Fig. 1. Architecture of the 0.5V smart imager.

extracted edge element indexes of three targets. Fig. 4(a) shows the real-time tracking of a circling object in 3-D demonstration with x-y axis as the spatial addresses and the z-axis as the time steps. The 2-D circular orbit is then turned into a spiral-shape. Fig. 4(b) illustrates the analysis of the tracking error.

Because of the slight angle difference between the target tracking plane and the focal plane, the circling object orbit is modeled as an elliptic track. 500 tracking address data are collected to do the asymptote ellipse curve fitting and calculate the tracking error. The tracking error is defined as follows:

$$D_i = \tfrac{1}{2} \times (\sqrt{\overrightarrow{A_i f_1}^2} + \sqrt{\overrightarrow{A_i f_2}^2}), i = 1 \sim 500 \qquad (1)$$

$$e_{track} = \tfrac{1}{500} \times \sqrt{\sum_{i=1}^{500} (D_i - \overline{D})} \qquad (2)$$

D_i is the distance between each tracking address and the two focus points of the asymptote ellipse; A_i is the tracking address and f_1, f_2 are the focus points. The tracking error e_{track} defined by the standard deviation of D_i shows a measured result of 0.36 pixel pitches.

4. Conclusion

For low-power imaging applications, low-voltage operating imager with embedded smart function is highly demanded. This paper introduces a 0.5V smart image sensor with multi-operation modes of edge extraction, centroid tracking, and high-dynamic-range imaging output. A 0.5V operated pulse-width-modulation (PWM) sensing platform is applied to achieve a high dynamic range (HDR) response with reduced fixed pattern noise (FPN). Array-level analog signal processing (ASP) is implemented by local inter-pixel feedback and the event-driven (ED) hand-shaking readout.

Compared to approaches with post-processing by off-chip DSP, the proposed smart imager effectively reduces the required data bandwidth and power consumption for high frame rate operation. The prototype achieves an asynchronous signal processing and recording operation in sub-micro seconds, which is suitable for low-power applications such as wearable devices and IoT.

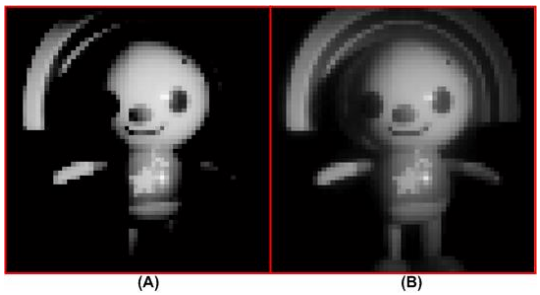

Fig. 2. Captured images (a) PWM (b) HDR PWM

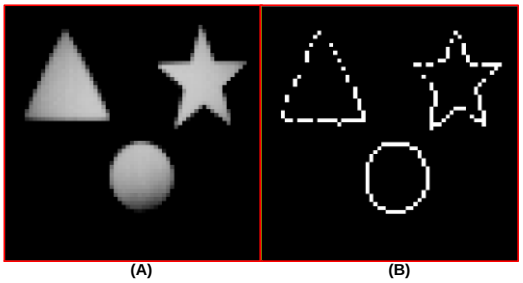

Fig. 3. Edge extraction (a) Original patterns (b) Extracted edge elements

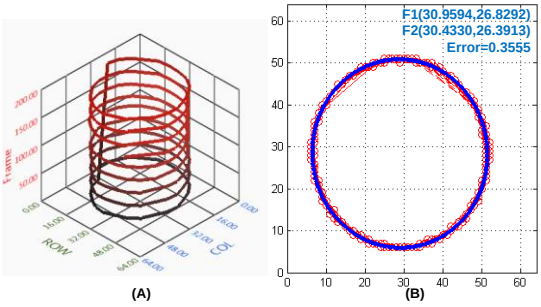

Fig. 4. Centroid tracking (a) Real-time track (b) Tracking error

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