A lin-log CMOS image sensor with controllable dynamic range

Myunghan Bae[1], Jeongyeob Kim[2], Byung-Soo Choi[1], Sannggwon Lee[1], Eunsu Shin[2], Heedong Kim[1], Jang-Kyoo Shin[1,†], and Jongho Park[3]

[1]School of Electronics Engineering, Kyungpook National University
80 Daehakro, Bukgu, Daegu 702-701, Korea

[2]Department of Sensor and Display Engineering, Kyungpook National University
80 Daehakro, Bukgu, Daegu 702-701, Korea

[3]Center for Integrated Smart Sensors (CISS), KAIST
291 Daehak-ro, Yuseong-gu, Daejeon, 305-701, Korea

E-mail: †jkshin@ee.knu.ac.kr

Abstract This paper presents the performance characteristics of a new active pixel sensor (APS) structure based on a linear-logarithmic response, which is implemented using a 0.35-μm standard CMOS process. The new pixel structure allows tuning of the dynamic range and the sensitivity. At the low-intensity light, both the dynamic range and the linear sensitivity were improved due to the increased capacitance of the photodetector. At the high-intensity light, the pixel is operated in a logarithmic mode by an additional MOSFET. Furthermore, the reference voltages can adjust the sensitivity and the starting point of logarithmic response.

Keywords: CMOS image sensor, linear-logarithmic response, wide dynamic range

1. Introduction

Recently, the CMOS active pixel sensor (APS) has been used in a wide variety of applications, including digital camera and mobile phones. The APS usually consists of a 3-transistor (3-Tr) APS or a 4-transistor (4-Tr) APS. The pinned photodiode based 4-Tr APS structure has been favorably used in the APS due to the performance advantages of low dark current and high sensitivity compared to the 3-T pixel structure [1]. However, the pinned photodiode based 4-Tr APS has some disadvantages, such as a small fill factor emerging from the use of additional transistors, a low dynamic range (DR) associated with the small well capacity, and high cost due to the required modification in the typical CMOS process [2][3].

Various approaches have been proposed to attain high-sensitivity and wide dynamic range [4][5][6]. Some equipment for high-sensitivity applications use photomultiplier tubes or charge-coupled devices (CCD). However, these photodetectors consume a large amount of power and cannot be integrated with CMOS logic circuits. Logarithmic sensors may extremely widen its dynamic range in high illumination range by compressing image signal. However, conventional logarithmic sensors operating in the sub-threshold region suffer from low sensitivity at low light intensity. The quality of the resulting output image of the logarithmic sensor is degraded by mismatches between the individual pixels in each sensor. Multiple sampling technique provides wide dynamic range without pixel modification. However, conventional multiple sampling method requires additional frame memory circuits and image synthesis process.

In this work, we proposed a novel CMOS image sensor to extend the dynamic range. The proposed APS has linear-logarithmic response and varied dynamic range by adjusting the reference voltage. It has been designed by using the 0.35μm 2-poly 4-metal CMOS process.

2. Pixel Structure and Operation

The pixel schematic diagram is illustrated in Fig. 1. This is equivalent-circuit diagram of the new pixel structure for the desired second linear operation and controllability of the proposed structure, a positive bias voltage (V_{lin}) is applied at the photogate. The new pixel structure is designed to be similar to a conventional 3-Tr APS structure. The overall photosensing part of the new structure is composed of both a photogate region and a photodiode region, as shown in Fig. 1. And logarithmic response is guaranteed by a series of transistors (M4 and M5), with the gate connected to the drain. The pixel response can simply be adjusted by tuning the point of transition between the linear and the logarithmic domains through the setting of a reference voltage (V_{log}).

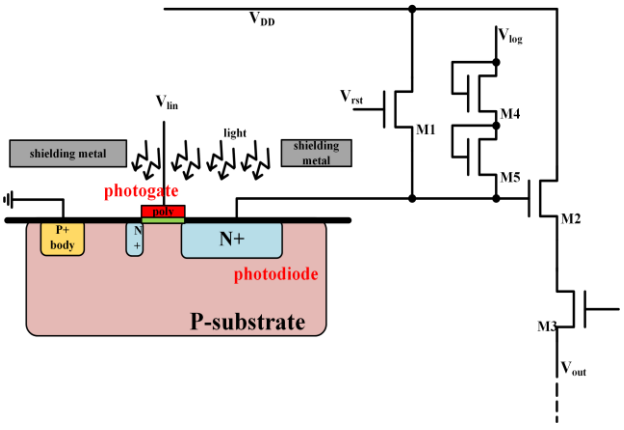

Fig. 1. Schematic diagram of the proposed pixel.

The detailed operating principle of the proposed pixel is as follows

equation:

$$V_{rst} \geq V_{PD} > V_{lin} - V_T : V_{PD} = \frac{\Delta Q}{C_{PD}} \quad \text{(1st linear response)} \qquad (1)$$

$$V_{lin} - V_T \geq V_{PD} > V_{log} - 2V_T : V_{PD} = \frac{\Delta Q}{C_{PG} + C_{PD}} \quad \text{(2nd linear response)} \qquad (2)$$

$$V_{log} - 2V_T \geq V_{PD} : V_{PD} = V_{log} - 2\frac{kT}{q}\ln\left(\frac{i_{ps}}{i_0}\right) \quad \text{(Logarithmic)} \qquad (3)$$

3. Simulation Results

Fig. 2 shows the simulation results of the variation of the output voltage in the proposed APS as function of V_{lin}. The Capacitance of sensing node can lead to second linear response. It has been found that the sensitivity of the new pixel structure at different photocurrent levels is tunable and controllable by varying V_{lin}.

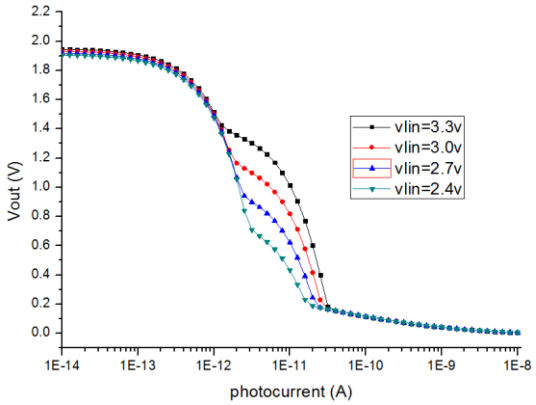

Fig. 2. Simulation results of the variation of the output voltage in the proposed APS as function of V_{lin} (V_{log} = 1.8V).

Fig. 3 shows the simulation results of the variation of the output voltage in the proposed APS as function of V_{log}. The results indicate that both the high-intensity sensitivity and the dynamic range of the new pixel structure can be significantly improved due to logarithmic response. The V_{log} can adjust the starting point of the logarithmic response.

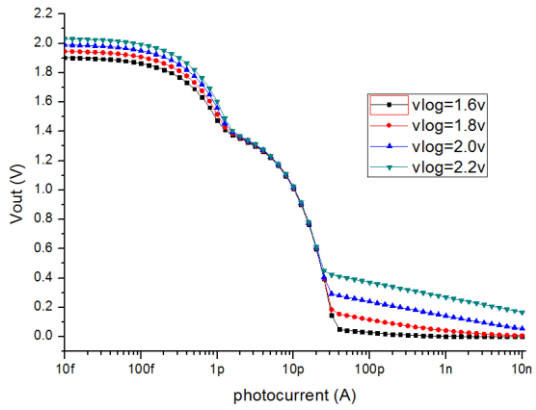

Fig. 3. Simulation results of the variation of the output voltage in the proposed APS as function of V_{log} (V_{lin} = 3.3V).

4. Conclusions

A new wide dynamic range pixel structure was proposed based on linear-logarithmic response. At the low-intensity light, both the dynamic range and the linear sensitivity were improved due to capacitance condition of the photodetector. The V_{lin} can adjust starting the point the second linear response. Furthermore, the pixel response can simply be adjusted by tuning the point of transition between the linear and the logarithmic domains through the setting of the V_{log}. The proposed pixel will be fabricated in a prototype with 120 x 160 resolution. Its characteristics will be evaluated and will be compared with the simulation results.

Acknowledgments

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References

[1] H. Abe, “Device technologies for high quality and smaller pixel in CCD and CMOS image sensors” IEDM Tech. Dig., pp. 989–992, (2004).

[2] K. Mabuchi, N. Nakamura, E. Funatsu, T. Abe, T. Umeda, T. Hoshino, R. Suzuki, and H. Sumi, “CMOS image sensors comprised of floating diffusion driving pixels with buried photodiode,” IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2408–2416, (Dec. 2004).

[3] H. Takahashi, M. Kinoshita, K. Morita, T. Shirai, T. Sato, T. Kimura, H. Yuzurihara, S. Inoue, and S. Matsumoto, “A 3.9-µm pixel pitch VGA format 10-b digital output CMOS image sensor with 1.5 transistor/pixel,” IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2417–2425, (Dec. 2004).

[4] T. H. Hsu, Y. K. Fang, D. N. Yaung, J. S. Lin, S. G. Wuu, H. C. Chien, C. H. Tseng, C. S. Wang, S. F. Chen, C. Y. Lin, C. S. Lin, and T. H. Chou, "An effective method to improve the sensitivity of deep submicrometer CMOS image sensors", IEEE Electron Device Letters, vol. 26, pp. 547-549, (2005).

[5] Y. Chae, K. Choe, B. Kim, and G. Han, "Sensitivity controllable CMOS image sensor pixel using control gate overlaid on photodiode", IEEE Electron Device Letters, vol. 28, pp. 495-498, (2007).

[6] M. Bae, S.-H. Jo, M. Lee, J.-Y. Kim, J. Choi, P. Choi, J.-K. Shin, "A wide dynamic range CMOS image sensor based on a pseudo 3-transistor active pixel sensor using feedback structure", Journal of Sensor Science and Technology, vol. 21, pp. 413-419 (2012).