

Block-based CMOS imaging system with reduced power consumption

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Abstract We have designed the block-based complementary metal oxide semiconductor (CMOS) image sensor. This image system has a unit block of the 4-by-4 pixels using the conventional 3-transistor active pixel sensor (APS). In addition, this system used additional computation circuit. The proposed imaging system can control the switch between the bias circuit and the transistor of pixel bias. The block-based CMOS imaging system has been fabricated using 0.35 μ m standard CMOS process. It was confirmed that the proposed block-based system can reduce the power consumption of the unit pixel arrays compared to the conventional active pixel arrays.

Keywords: CMOS image sensor, block-based system, active pixel sensor, power consumption

1. Introduction

The image sensor has distributed charge coupled device (CCD) and CMOS image sensor (CIS) [1]. Recently, the sensor is used in many applications that is available the security camera, digital camera and medical equipment. Because the CIS is superior in power efficiency than the CCD [1-2]. The operation of CIS depends on battery. By using the battery, power consumption is very important for low power CIS. In recent years, the CIS have been conducted the many research to improve the operated in low power consumption [3].

We propose the block-based CMOS imaging system that it clearly improves the power efficiency of the pixel arrays. Using the additional computation circuit, the proposed CIS can control the pixel arrays [4]. And this image system is used conventional 3-transistor active pixel sensor. In addition, this system can control using the switch between the bias circuit and pixel bias.

In this paper, the block-based CMOS imaging system was fabricated using 0.35 μ m standard CMOS process on a Cadence Virtuoso platform.

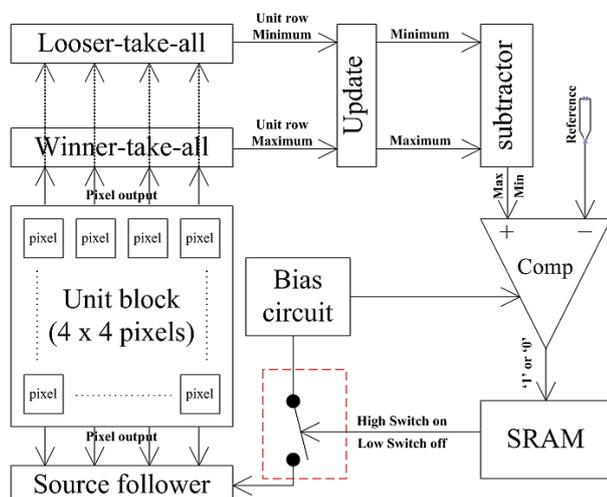


Fig. 1. Structure of proposed block-based CMOS image system.

2. Experimental

The proposed block-based CMOS imaging system structure is shown in Fig. 1. This CIS consist of a unit block, the winner-take-all(WTA), the loser-take-all(LTA), the update circuit, the subtractor, the comparator, the static random access memory (SRAM) cell, the bias circuit and the control switch. A unit block is consist of the 4-by-4 pixel arrays. The structure of unit block is

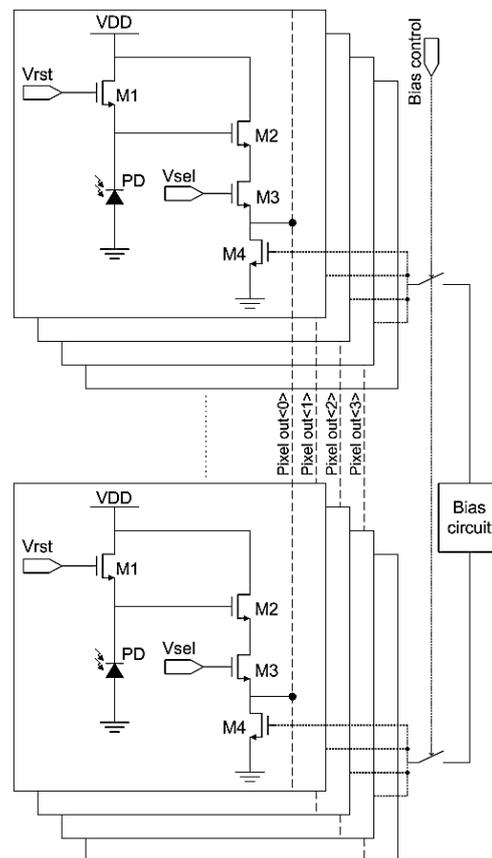


Fig. 2. A unit block structure composed of 3-transistor active pixel sensor.

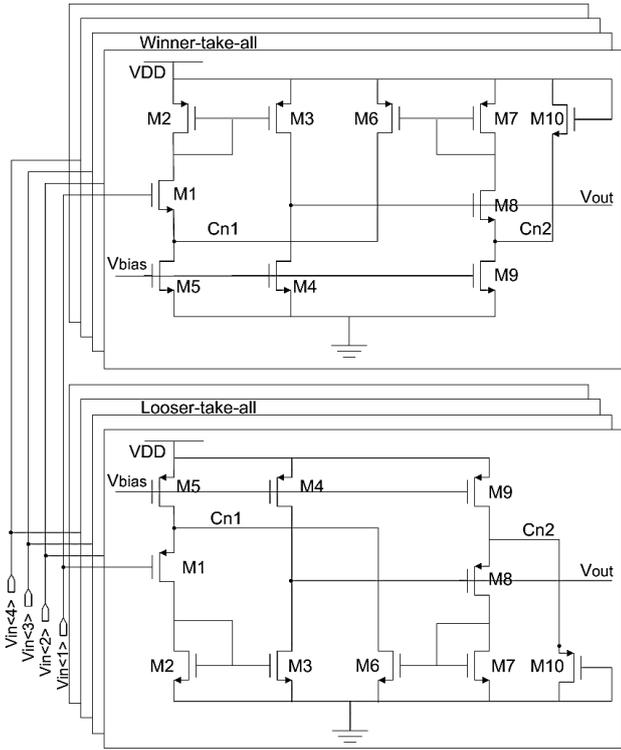


Fig. 3. The winner-take-all and looser-take-all circuit.

shown in Fig. 2. The output signal of pixel for first row is transmitted to the input signal of the WTA and LTA. The WTA and LTA circuit is shown in Fig. 3. After the output signal of the WTA and LTA calculated from the update circuit and the subtractor in a unit block. Using the comparator, the output signal of the subtractor circuit is compared to the reference signal. And this output signal stored in the SRAM cell. Therefore, the stored signal in the SRAM can control the switch between the bias circuit and the pixel bias.

3. Simulation and results

In simulation, the operation of WTA and LTA are shown in Fig. 4. The input voltage range of the WTA/LTA is set up the output swing of the pixel in Fig.4 (a). The WTA/LTA selects the maximum and minimum signals in the first row of a unit pixel in Fig. 4 (b).

Fig. 5 shows measurement result of (a) conventional image and (b) block-based image. The conventional image mode shows the blooming phenomenon around the light source. But the block-based image mode can decrease blooming phenomenon controlling the pixel. The block-based CMOS imaging system can reduce the power consumption of the pixel compared to the conventional active pixel arrays.

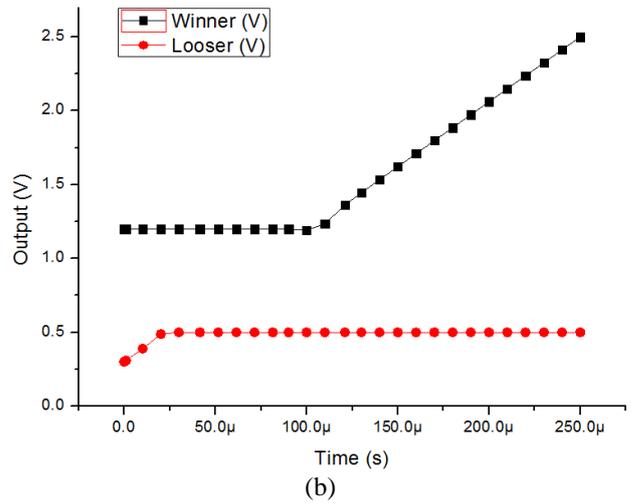
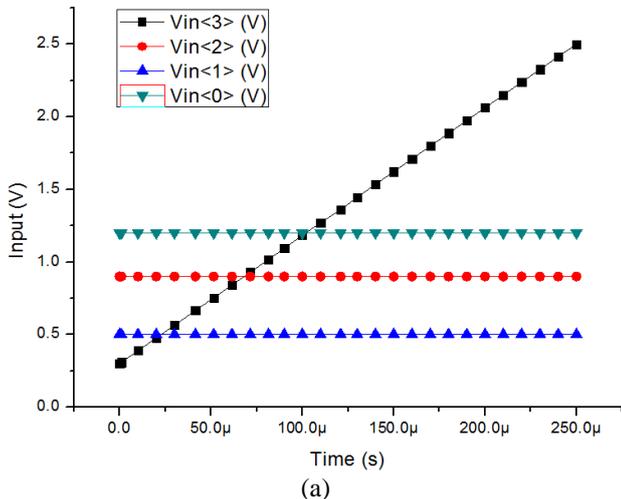


Fig. 4. Simulation of the winner-take-all and the looser-take-all circuit

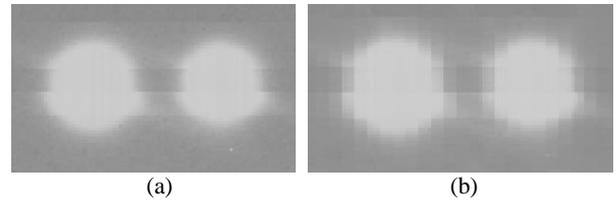


Fig. 5. Measurement result of (a) conventional mode and (b) block mode

4. Conclusion

In this paper, the block-based CMOS imaging system has been fabricated using 0.35µm standard CMOS process. By using the additional computation circuit, the block-based CMOS imaging system can reduce the power consumption using the unit pixel arrays compared to the conventional active pixel arrays. In addition, this proposed block-based CMOS imaging system can decrease the blooming phenomenon around the light source.

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