A Time-of-Flight CMOS Image Sensor with 4-Tap Lateral-Electric-Field Charge Modulators

Taichi KASUGAI† Sang-Man HAN† Hanh TRANG† Taishi TAKASAWA† Satoshi AOYAMA‡
Keita YASUTOMI† Keiichiro KAGAWA† and Shoji KAWAHITO†

†Research Institute of Electronics, Shizuoka University
3-5-1 Johoku, Naka-ku, Hamamatsu, Shizuoka, 432-8011 Japan
‡Brookman Technology, Daihatsujisho Bldg. 10F
125 Daikumachi, Naka-ku, Hamamatsu, Shizuoka, 430-0936, Japan

E-mail: †{tkasu, hansm, hanhtr, ttakasawa, kyasu, kagawa, kawahito}@idl.rie.shizuoka.ac.jp,
‡saoyama@brookmantech.com

Abstract This paper presents a CMOS ToF range imager with 4-tap charge modulator using pinned-photodiode high-speed lock-in pixels. The proposed lock-in pixel structure using lateral electric field (LEF) control is suitable for implementing a multiple-tap charge modulator while achieving high-speed charge transfer for high time resolution. In this presentation, we report the design, implementation and evaluation results of the ToF range imager using the 4-tap LEF modulator.

Keywords CMOS image sensor, Time-of-Flight, 3D range image, Lateral-Electric-Field Charge Modulator

1. Introduction

Time-of-Flight (ToF) range imagers have a wide range of application such as gesture-based remote controllers, amusements, 3D mice, 3D scanner, robot eyes, security systems and car-mounted camera. Various developments of ToF range imagers have been reported [1-5]. However, the reported CMOS ToF range imagers use single-tap or two-tap lock-in pixels, which require multi frames for background light cancelling.

This paper presents a CMOS ToF range imager with 4-tap lateral electric field charge modulator (LEFM) [6][7] using pinned-photodiode high-speed lock-in pixels. The proposed lock-in pixel structure using LEF control is suitable for implementing a multiple-tap charge modulator while achieving high-speed charge transfer for high time resolution. A CMOS ToF range imager with the multiple-tap charge modulators is expected to have background light cancelling capability in one frame and to improve range resolution with shifted short light pulses.

2. Pixel and ToF imager design

2.1. Lock-in pixel with LEFM

Fig. 1 shows the charge modulator using LEF control with 2-tap outputs and a Drain. In this charge modulator, 3 sets of gates (G1, G2, and GD) for applying lateral electric field to the channel region are used. The gates are not used for draining photo charge, but used for controlling electric field. For example, when the G1 is ON and the others are OFF, the potential of the LEFM (see profiles of X-X' and Y-Y') attracts photo electrons generated in the aperture region to be transferred to FD1. Similarly, photo electrons are transferred to FD2 or Drain by applying ON level to G2, GD, respectively, and OFF levels to the others. During signal readout, GD is ON and other gates are OFF for preventing the influence of background light. The doping concentration of the p-type epitaxial layer and surface p^+ layer for hole pinning are optimized for realizing large potential modulation in the pinned-photodiode. In this work, we have investigated the charge modulator having 4-tap outputs (FD1, FD2, FD3 and FD4) and 5 sets of gate (G1, G2, G3, G4 and Drain).

2.2. Operating principles

The timing diagram with a small duty ratio light pulse is shown in Fig. 2. The gate pulse width of G1, G2, G3 and G4 is given by R_DT_C, where T_C is the cycle time and R_D is duty ratio of the gate pulse to the cycle time. Then, the gate pulse width of GD is given by $(1-4R_D)T_C$. The signal light pulse width and the time of flight of the received light are denoted by T_0 and T_d, respectively. The difference of the amount of charges between the two FDs (FD2, FD3) reflects the time-of-flight of light pulse. The range is calculated by the delay-dependent charges. The equation for estimating the range in each pixel is given by

$$\mathbf{L} = \frac{\mathbf{cT_0}}{\mathbf{2}} \cdot \frac{\mathbf{S_2}}{\mathbf{S_2 + S_3}} \tag{1}$$

where c is the speed of light, S_2 and S_3 are outputs of FD2 and FD3, respectively.

Actually, the background light charge may disturb the accuracy of the range calculation. In order to cancel the background light, FD1 is used for taking background light charges only. By subtracting the output of FD1 from FD2 and FD3, the background light is canceled. Furthermore, range resolution is improved without reducing measurement range of the ToF imager by using FD3 and FD4 in measurement.

3. Demodulation Contrast

The sensor architecture is shown in Fig. 3. The TOF imager consists of a 160×240 pixel array, vertical and horizontal shift register, analog-to-digital converter (ADC), and LEF charge modulator driver. Each pixel has four FDs which are shared by twelve charge modulators. Each of the four outputs from each pixel are connected each of the column ADC and are converted to digital codes in parallel using high-resolution folding integration/cyclic ADCs [8].

Fig. 4 shows a measured demodulation contrast under the various gate pulse width, R_DT_C. These measurement results are obtained by average of 10 frames in 10×10 pixels in the center of the array. The frame rate is 15fps. The signal light pulse, T_0 is set to 13ns. The high demodulation contrast of 80% is achieved even when the gate pulse width is 20ns.

4. Conclusion

This paper presented a CMOS ToF range imager with 4-tap LEFM using pinned-photodiode high-speed lock-in pixels. A CMOS ToF range imager with multiple-tap charge modulators offer background light cancelling capability in one frame and improve range resolution with shifted short light pulses. The high demodulation contrast of 80% is achieved by the developed ToF range imager.

5. Acknowledgements

This work was partly supported by the JSPS Grant-in-Aid for Scientific Research (S), No. 25220905 of JSPS and JST COI STREAM.

6. References

[1] R. Lange, et al., "Demodulation Pixels in CCD and CMOS technologies for Time-of-Flight Ranging," Proc. SPIE, vol. 3965, pp. 177-188, 2000.

[2] S. Kawahito, et al., "A CMOS time-of-flight range image sensor with gates-on-field-oxide structure," IEEE Sensors J., vol. 7, no. 12, pp. 1578-1586, Dec. 2007.

[3] D. Stoppa, et al., "A Range Image Sensor Based on 10um Lock-In Pixels in 0.18um CMOS Imaging Technology," IEEE J. Solid-State Circuits, vol. 46, no. 1, pp. 248-258, Jan. 2011.

[4] O. Shcherbakova, et al., "3D camera based on linear-mode gain-modulated avalanche photodiodes," ISSCC Dig. Tech. Papers, pp. 490-491, Feb. 2013.

[5] A. Payne, et al., "A 512×424 CMOS 3D Time-of-Flight image sensor with multi-frequency photo-demodulation up to 130MHz and 2GS/s ADC," ISSCC Dig. Tech. Papers, pp. 134-135, Feb. 2014.

[6] S. Kawahito, et al., "CMOS Lock-in Pixel Image Sensors with Lateral Eelectric Field Cotrol for Time-Resolved Imaging," Proc. 2013 Int. Image Sensor Workshop (IISW), pp. 361-364, Jun. 2013.

[7] S-M. Han, et al., "A 413×240-pixel sub-centimeter resolution Time-of-Flight CMOS image sensor with in-pixel background canceling using lateral-electric-field charge modulators," ISSCC Dig. Tech. Papers, pp. 130-131, Feb. 2014.

[8] M-W. Seo, et al., "A Low-Noise High Intrascene Dynamic Range CMOS Image Sensor With a 13 to 19b Variable-Resolution Column-Parallel Folding-Integration/Cyclic ADC," IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 272-283, Jan. 2012.

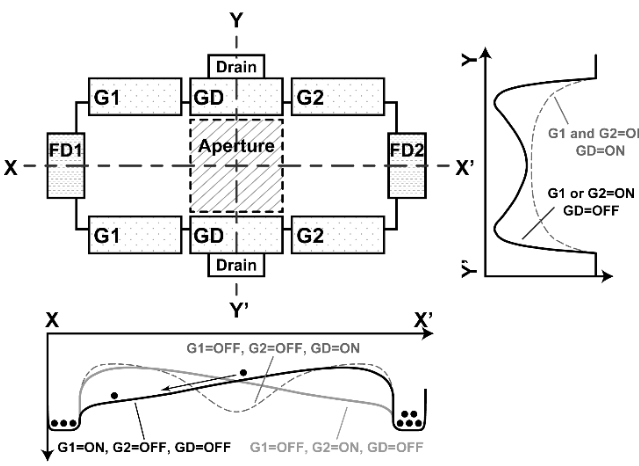

Figure 1: 2-Tap LEFM with Drain

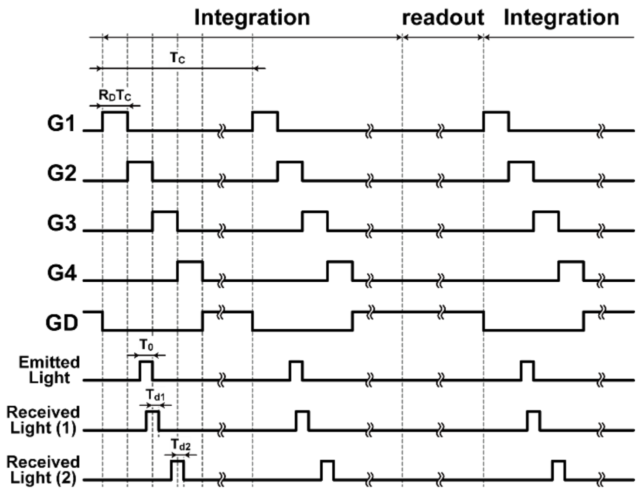

Figure 2: Timing diagram for the lock-in pixel operation

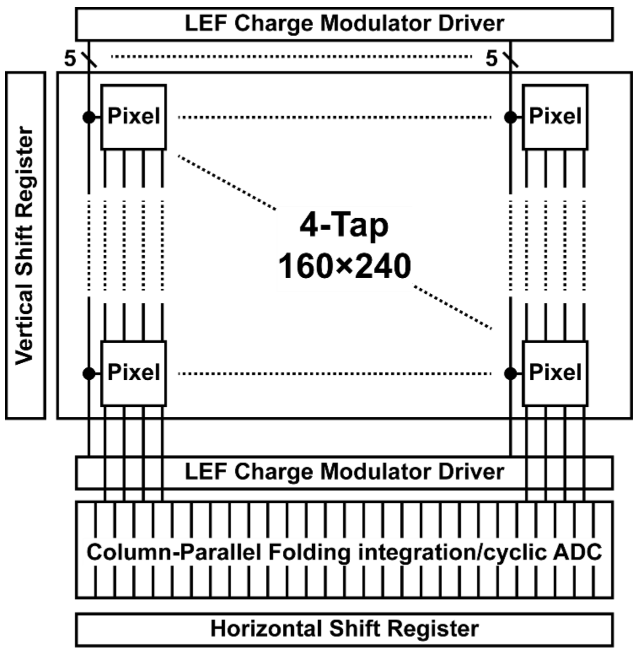

Figure 3: Sensor architecture

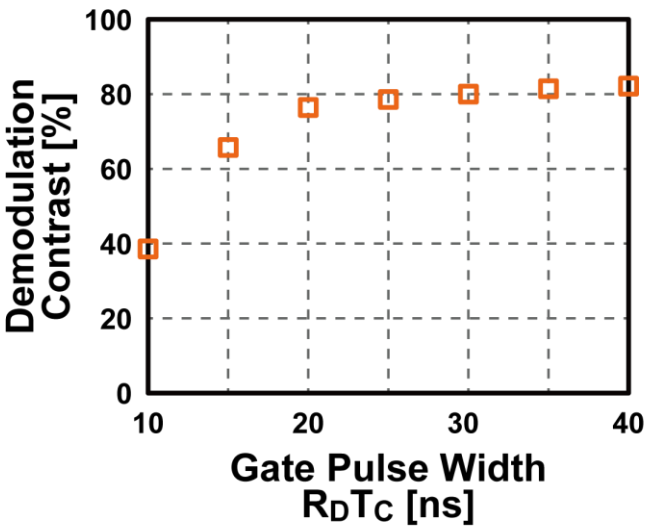

Figure 4: Demodulation contrast