Design and implementation of multiple-focal plane CMOS image sensor

Hiroyuki HAKOISHI†, Toshinori Otaka†, and Takayuki HAMAMOTO†

†Graduate School of Engineering, Tokyo University of Science
Niijuku 6-3-1, Katsushika-ku, Tokyo, 125-8585 Japan

E-mail: †{hakoishi,otaka,hamamoto}@isl.ee.kagu.tus.ac.jp

Abstract We propose a multiple-focal plane CMOS image sensor to obtain multi-view images using a single device. The image sensor has 12 small focal planes and can simultaneously capture multi-view images by controlling them individually. Using this image sensor, we can obtain the multi-view images by a system that is smaller than conventional camera array systems. In this paper, we describe the architecture of the proposed multiple-focal plane CMOS image sensor and the specifications of a prototype chip.

Key words CMOS image sensor, multiple-focal plane, distance estimation, stereo matching

1. Introduction

Stereo matching is a well-known technique for obtaining 3D information from multi-view images, and there are various methods for obtaining high-accuracy 3D information using stereo matching. For example, methods using multi-view images captured with different exposure times or various baselines were investigated [1][2]. However, in order to implement these methods in real time, it is necessary to use large systems such as camera array. As a result, the size of the imaging system would be large, and the power consumption of the imaging system increases [3].

We propose a multiple-focal plane image sensor to obtain multi-view images with a single device. The image sensor has 12 focal planes, and each of them has a read-out circuit and drive circuits. Thus, the image sensor can capture a multiple images simultaneously by controlling each small focal plane individually. Therefore, by placing a lens in each small focal plane, it is possible to obtain multi-view images at the same time.

In this paper, we describe the architecture of the proposed multiple-focal plane image sensor and the specifications of a prototype chip.

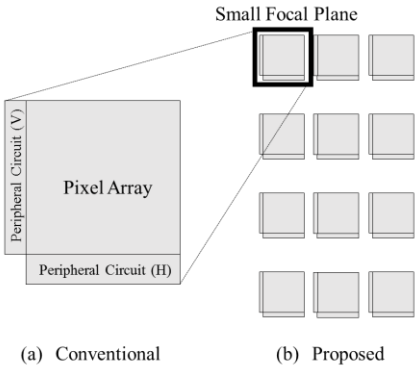

Figure 1: Sensor architecture.

2. Multiple-Focal Plane Image Sensor

2.1 Chip Architecture

As shown in Figure 1(a), a conventional image sensor has a single focal plane. On the other hand, as shown in Figure 1(b), the proposed multiple-focal plane image sensor has 12 small focal planes. This image sensor can read out images at the same time from all small focal planes, because each small focal plane has its own read-out circuit. Therefore, by placing a lens in each small focal plane, it is possible to obtain multi-view images as with camera array systems.

2.2 Architecture of the Small Focal Plane

Figure 2 shows the architecture of the small focal plane. Each small focal plane has a pixel array that consists of 64 × 64 3-transistor pixels, horizontal and vertical shift registers, a reset controller, a level shifter, and an analog readout circuit. An analog readout circuit consists of column readout circuits and an analog buffer. Each small focal plane can obtain images captured by different exposure times and different frame rates, because each small focal plane has its own horizontal and vertical shift registers, reset controller, and readout circuits.

In the 3-transistor pixels, reset noise cannot be removed because correlated double sampling cannot be performed. Therefore, this image sensor implements a hard reset operation by boosting the reset pulse at the level shifters, to reduce the reset noise due to variation in the threshold voltage of the reset transistors.

3. Specifications of Prototype Chip

In order to verify the operation of the image sensor, we designed a prototype chip. Figure 3 shows an overview of the layout, and Table 1 shows the specifications of the prototype chip. This prototype chip was fabricated in a ROHM-0.18 μm 1P5M process, and the die size of this chip is 2520 μm × 5180 μm. There are 12 small focal planes in the prototype chip and each of them has a 64 × 64 pixel array that uses a 7 μm pitch 3-transistor pixel circuit. The aperture ratio of the chip is 35%, and the maximum frame rate is 300 fps. In addition, analog-to-digital (AD) conversion is performed by the chip AD converter mounted on the outside of the chip.

4. Conclusion and Future Work

In this paper, we proposed the multiple-focal plane CMOS image sensor to obtain multi-view images using a single device, and we described the design and implementation of the proposed image sensor.

As forthcoming challenges, we will verify the operation of the prototype chip and consider a method to obtain 3D information using the proposed image sensor.

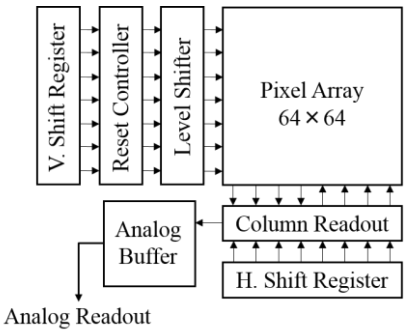

Figure 2: Architecture of the small focal plane.

Table 1: Chip specifications

Process	ROHM-0.18 μm 1P5M CMOS
Die Size	2520 μm × 5180 μm
Pixel Architecture	7 μm × 7 μm 3-Transistor pixel
Pixel Count	64×64 /Small Focal Plane
Small Focal Plane Count	12
Aperture Ratio	35%
Maximum Frame Rate	300fps

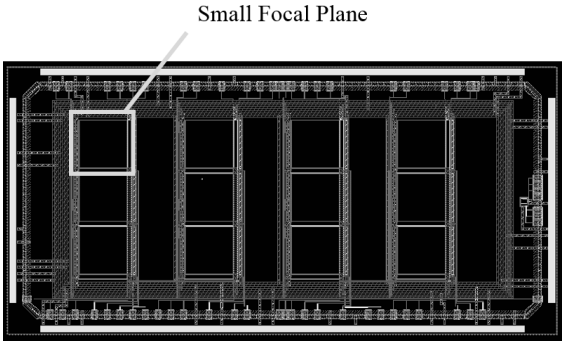

Figure 3: Layout of the prototype chip.

References

[1] M. Okutomi, T. Kanade: “A Multiple-Baseline Stereo”, IEEE Trans. Pattern Analysis and Machine Intelligence, vol. 15, No.4, pp. 355–363, Apr. 1993

[2] A. Troccoli, S. Bing Kang, S. Seitz: “Multi-view multi-exposure stereo”, IEEE 3D Data Processing, Visualization and Transmission, pp. 861-868, Jun. 2006

[3] KB. Cho *et al.*: “A 12MP 16-Focal Plane CMOS Image Sensor with 1.75μm Pixel: Architecture and Implementation”, International Images Sensor Workshop, 8.05, Jun. 2013