A low-noise stimulated Raman scattering CMOS imager using high-speed lock-in pixels

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Abstract We demonstrate a low-noise stimulated Raman scattering (SRS) CMOS imager using high-speed lock-in pixels. To detect small SRS signal under an extremely large offset due to probing laser signal of which the ratio is 10^{-5}, a lock-in pixel using a high-speed demodulator, low-pass filter, and multiple-sampling amplifier is designed. The residual offset and low-frequency noise are reduced by two steps; one is sampling phase adjusting in the multiple-sampling amplifier and the other is a double modulation technique. The double modulation effectively reduces the offset and low-frequency noise, or 1/f noise. A SRS CMOS imager chip for the proof of concept is implemented and a successful operation is demonstrated. The detectable AC signal level under the large DC offset is measured to be smaller than ratio of 10^{-4}. This finding suggests that the detection of a very small SRS signal from a biological sample is feasible using this technique.

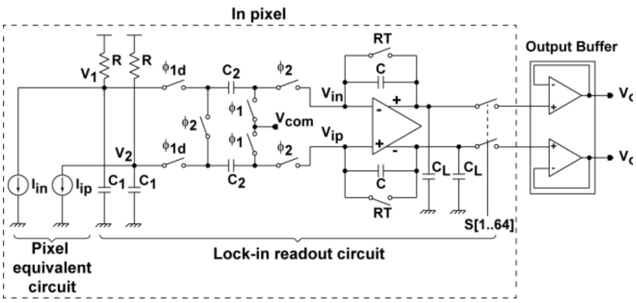
Keywords: stimulated Raman scattering (SRS), lock-in pixels, noise reduction

1. Introduction

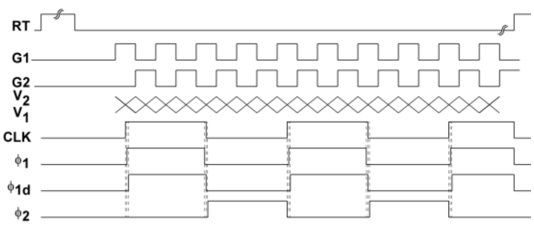
Recent advances in coherent spectroscopy have made stimulated Raman scattering (SRS) emerged as a label and nonresonant-background-free imaging technique. SRS non-invasively offers imaging contrast mechanism of biological samples [1][2]. SRS operates with two laser beams, pump beam (ωp) and Stoke beam (ωs), to interact with the sample, which is in contrast with spontaneous Raman scattering which uses only a single laser beam. Once the frequency difference, Ω = ωp - ωs, also known as Raman shift, coincides with a particular molecular resonance frequency, stimulated excitation occurs. With the resulting pump signal exists at the same wavelength as the incident laser source, the weak SRS signal which is 10^{-4} to 10^{-5} times smaller than the input signal is hardly distinguishable. Despite this, high-speed modulation lock-in pixels [3][4] can be used to extract the SRS signal. This paper introduces the SRS acquisition and noise reduction techniques.

2. Imager and the Operation

The architecture of the lock-in pixel is shown in Fig. 1(a), which consists of pixel equivalent circuit of the modulator, low pass filter, sample and holding circuitry, and multiple-sampling amplifier. Fig. 1(b) shows the timing operation of the lock-in pixel circuit. Initially, the amplifier is reset through the switches RT, in which all other clocks are in OFF state. Switches ϕ1 are then turned ON to allow capacitors C2 to be set to the reference Vcom level. After a small delay, switches ϕ1d are turned ON in order for capacitors C2 to be charged. Both ϕ1 and ϕ1d are then turned OFF one after another before switches ϕ2 are turned ON for charges in C2 to be transferred to capacitors C for integration.

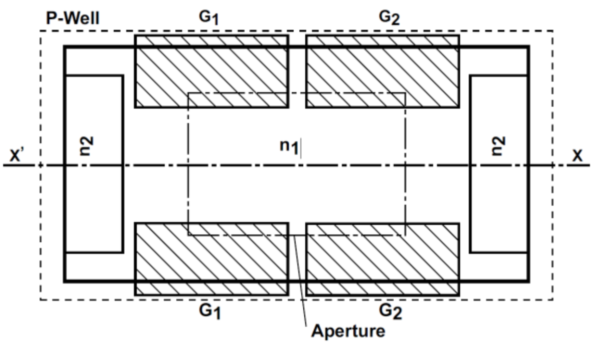


(a)

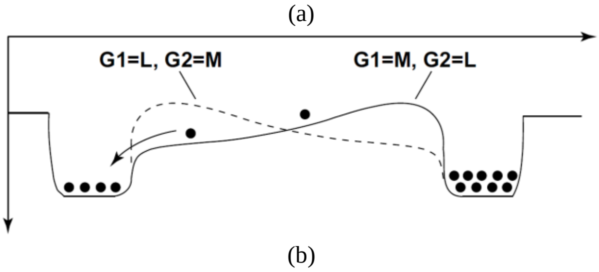


(b)

Fig. 1: Lock-in pixel (a) schematic diagram
(b) timing diagram



(a)



(b)

Fig. 2: Lateral Electric Field Charge Modulator (a) top view
(b) potential profile

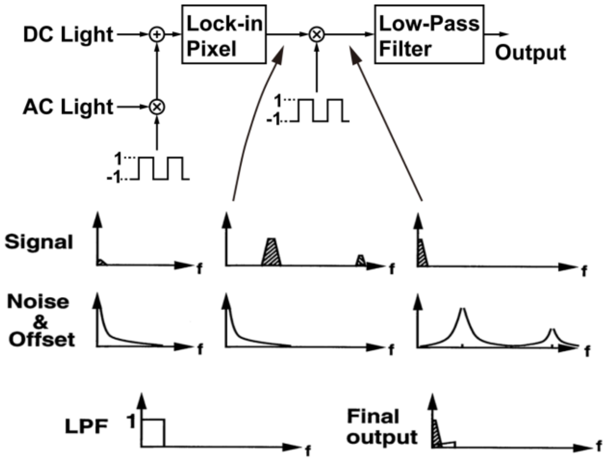
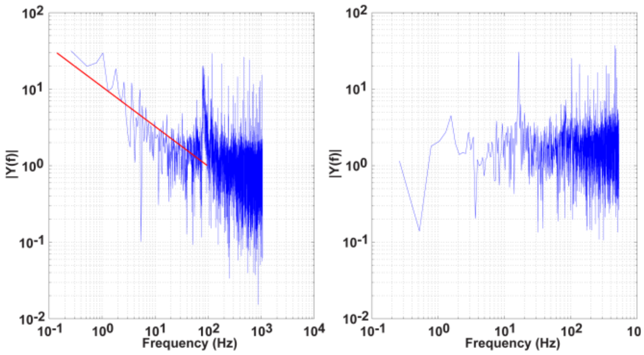


Fig. 3: Double modulation methodology



(a) (b)

Fig. 4: Effect of noise reduction (a) without double modulation (b) with double modulation

Fig. 2(a) shows the lateral electric field modulator (LEFM), which uses two gates, G_1 and G_2, for applying lateral electric field to control the horizontal direction of electron flow, rather than photo charge draining. The modulation is performed by applying a medium voltage to one gate and low voltage to another, as depicted in Fig. 2(b). A strong electric field is created in this way which leads to very high transfer rate of lower than 100ps.

3. Noise Reduction Techniques and Results

The reduction of residual offset and low-frequency noise are performed in two steps. The first is the sampling phase adjustment where the phase delay of the demodulated pixel output signal and the readout clock $\phi1$, $\phi1d$ and $\phi2$ are carefully adjusted to ensure that the offset signal is cancelled and to achieve high dynamic range. The differential output of the amplifier should be equal to zero during the absence of signal.

A double modulation noise reduction technique is the next step to overcome the low-frequency noise, as shown in Fig. 3. Initially, AC light signal is multiplied by the square wave signal. After this first modulation, the signal is transposed to a higher frequency while the noise and offset components remained. The signal is then amplified and upon second modulation, demodulated back to the baseband. At the same time, the noise component is transposed to high frequency. This technique effectively separate the signal and noise to low and high-frequency components, respectively. The higher frequency noise components are then removed by low-pass filter.

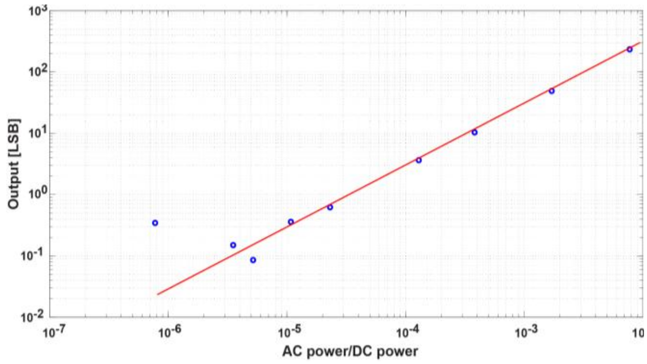


Fig. 5: Ratio of AC power / DC power

4. Experimental Results

A SRS CMOS image sensor chip has been fabricated using 0.11µm CMOS image-sensor process technology to evaluate the performance. Fig. 4(a) and (b) illustrate the Fast Fourier Transform (FFT) of the measured signal noise with and without double modulation, respectively. Noise is evident in the low-frequency region without double modulation, while the noise is greatly reduced with double modulation technique applied.

Fig. 5 shows the plot of an average value from 6 measurements of the ratio of the AC (pump) signal to the DC (Stoke) signal. Ratio of approximately 10^{-5} is achieved, which is vital in very weak SRS signal detection.

5. Conclusion

The paper presents the verification of the SRS CMOS imager prototype. The performance of the noise reduction techniques was developed and verified. The imager achieved the AC signal to DC signal power ratio of 10^{-5}, which is an essential region to obtain the SRS signal, and consequently further improves the dynamic range of the SRS CMOS imager.

References

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