A 12-bit Folding-Integration/Cyclic ADC using DMOS capacitors for CMOS image sensors

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Abstract This paper presents a 12-bit folding-integration/cyclic (FI/Cyclic) ADC using depletion-mode MOS (DMOS) capacitors for CMOS image sensors (CISs). It has been verified by circuit simulation that the differential non-linearity (DNL) of the FI/Cyclic ADC caused by the voltage dependency of DMOS capacitor is very small.

Keywords: folding-integration/cyclic ADC, DMOS capacitor, split sampling capacitors, DNL.

1. Introduction

The column-parallel analog-to-digital converter (ADC) is a most promising ADC architecture for CMOS Image sensors (CISs). A single-slope (SS), successive approximation (SAR), and cyclic ADCs are popular for the column-parallel ADC [1][2][4]. Recently, for attaining very low noise, high gray resolution and high dynamic range, the column-parallel folding-integration/cyclic (FI/Cyclic) for CISs is developed.

Usually, Metal-insulator-metal (MIM) and Metal-oxide-metal (MOM) capacitors are used for a high-resolution column-parallel ADC. The depletion-mode MOS (DMOS) capacitor is not so popular due to its large voltage dependency of the capacitance, which results in a large non-linearity of the ADC. However, the higher capacitance density of DMOS capacitor is very useful for reducing the silicon area of the chip.

This paper presents a 12-bit FI/Cyclic ADC employing DMOS capacitors as its sampling and feedback capacitors. The 1.5b cyclic ADC with the equally divided DMOS sampling capacitors in the 1.5b ADC for internal mid-point reference generation can greatly reduce the DNL caused by the voltage dependency of DMOS capacitors. A low DNL is very important for the column-parallel ADC used for CISs, because the quality of image is not sensitive to the integral non-linearity (INL) but sensitive to the DNL of the ADC.

2. DMOS capacitor and its application in FI/Cylic ADC as sampling and feedback capacitors

The DMOS capacitor is a capacitor based on a MOSFET the channel of which has a high doping of same impurities as those of the source and drain as shown in Fig. 1. To use this MOSFET as a capacitor, the source and drain are connected together and the capacitance between the gate (G) to source/drain (S/D) terminals is used. The high channel doping greatly reduces the applied voltage dependency of the G-to-S/D capacitance.

The capacitance of the DMOS capacitor is expressed as a first-order function of the applied voltage [3], as Eq. (1) shows,

$$C(V_X)=C_0(1+a_1V_X) \quad (1)$$

where V_X is the applied voltage difference of G-to-S/D, C_0 is the constant capacitance when V_X is equal to zero and a_1 is the voltage dependency coefficient. Hence, the amount of change of the charge stored in a DMOS capacitor ΔQ if it is charge from the voltage V_1 to V_2 is expressed as

$$\Delta Q=\int_{V_1}^{V_2} C_0(1+a_1V_X)dV_X = C_0[(V_2-V_1)+\frac{a_1}{2}(V_2^2-V_1^2)] \quad (2)$$

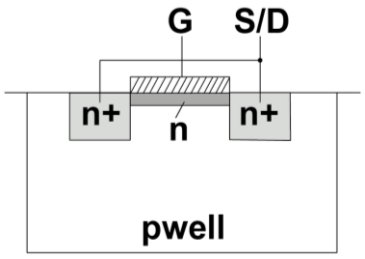

Fig. 1. Structure of DMOS.

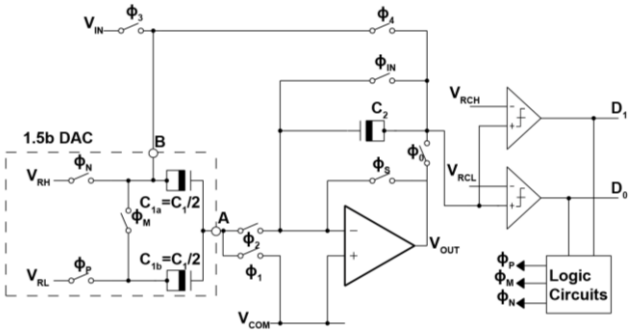

Fig. 2. Cyclic ADC using DMOS capacitors with split sampling capacitors. (C_{1a} = C_{2a} = $C_1/2$ = $C_2/2$)

The operation of the cyclic ADC using DMOS capacitors is divided into two phases: in the sampling phase, the input signal (which is from the residue of the previous stage FI ADC) or output of the residue amplifier is sampled and 1.5b sub-A/D conversion is carried out; in the residue generation phase, the residue is generated by 1.5b DAC and an amplifier. In the sampling phase, the residue amplifier output is sampled by input capacitors, C_{1a} and C_{1b}, and then in the residue generation phase, the S/D terminals of C_{1a} and C_{1b} are connected to references in the 1.5b DAC and the charge in C_{1a} and C_{1b} is transferred to C_2 [5]-[8].

With the 1.5b DAC with proposed split sampling DMOS capacitors, an accurate mid-point reference voltage is generated by

$$V_{Rm}(i)=\begin{cases} V_{RHm}=V_{RH}+a_1{V_{RH}}^2/2 & (D(i)=2) \\ V_{RMm}=(V_{RH}+V_{RL})/2+a_1({V_{RH}}^2+{V_{RL}}^2)/2 & (D(i)=1) \\ V_{RLm}=V_{RL}+a_1{V_{RL}}^2/2 & (D(i)=0) \end{cases} \quad (3).$$

However, compared with the importance of cyclic ADC using split sampling DMOS capacitors, the similar configuration of FI

ADC is not necessary. In the other word, both 1-bit and 1.5-bit sub-ADC for FI ADC are acceptable [9][10].

3. Circuit simulation results

A 4-bit FI ADC and 9-bit cyclic ADC using DMOS capacitors is designed. The resolution of FI/Cyclic ADC is 4+9-1=12 bit. The input range of FI/Cyclic ADC is from 300 mV to 900 mV. For observing the DNL characteristics of FI/Cyclic ADC, 60 input points are simulated and the step between two points is set to 1 LSB, which means $600/2^{12}$=0.1465 mV. For comparing the influence of the voltage dependency of DMOS capacitor, the same FI/Cyclic ADC with ideal capacitors which have no voltage dependency is also used.

As Fig. 3 shows, only 1 input point of 60 points misses its output digital code in FI/Cyclic ADC using ideal capacitors. After replacing ideal capacitors by DMOS capacitors, the DNL of FI/Cyclic ADC is not increasing as Fig. 4 shows. The DNL of the column FI/Cyclic ADC may cause vertical fixed pattern noise and the increase of temporal random noise due to modulation of random noise by the DNL. Therefore, in the application of the column ADC to low-noise CISs, the DNL have to be limited as small as possible. Since the voltage dependency of DMOS capacitors does not influence the DNL of FI/Cyclic ADC, DMOS capacitors can replace traditional MIM capacitors due to its higher capacitance density.

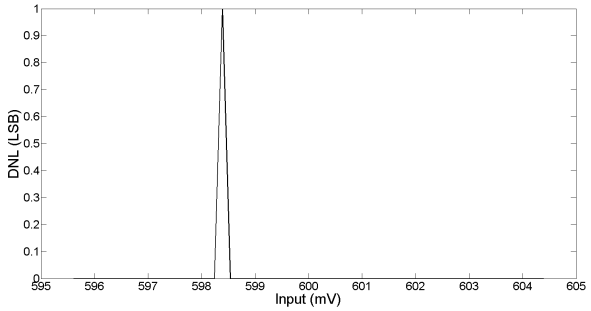

Fig. 3. Partial DNL of FI/Cyclic ADC using ideal capacitors.

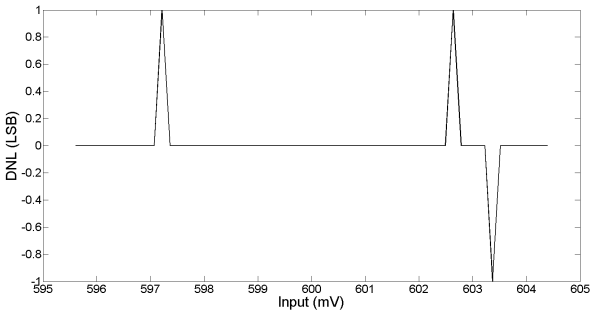

Fig. 4. Partial DNL of FI/Cyclic ADC using DMOS capacitors.

4. Conclusion

By using cyclic ADC with split sampling DMOS capacitors, the DNL of the 12-bit FI/Cyclic ADC using DMOS capacitors is not increasing, compared with the same FI/Cyclic ADC using ideal capacitors.

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