A 4T-PWM CMOS image sensor for low power

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Abstract Low power operation is essential in the applications of CMOS image sensors to Internet of Things (IoT). Focusing on the potential of low power operation, we are developing a pulse-width-modulation pixel based on the 4T-APS to realize low-noise and high sensitivity imaging as well. In this report, feasibility of the 4T-PWM performing pixel-level single-slope ADC is examined, and pixel operation is verified with test circuits.

Key words CMOS image sensor, pulse-width-modulation, low power consumption, TDC

1. Introduction

Applications to monitor ambient information for Internet of Things (IoT) or trillion sensors are attracting a great attention. Low power operation is essential to drive the device with energy harvesting or a small battery.

A pixel readout scheme based on pulse width modulation (PWM) in CMOS image sensors is promising to realize low power operation while keeping the sensor performance[1]. This method has been studied with a 3-transistor pixel structure in the previous works. However, it is not suitable for high quality imaging in dim light conditions because the dark current of photodiode (PD) is large. In this report, a PWM pixel based on the 4-transistor pixel using a pinned photodiode, that is 4T-PWM, is presented, which realizes low dark current. Preliminary experiments are also shown.

2. 4T-PWM image sensor

Fig. 1 shows the pixel circuit of the 4T-PWM. The significant feature of this pixel is a common source amplifier used as a comparator in the pixel. Thus, we realize a PWM pixel with the same number of transistors as that in the normal active pixel sensor (APS), typically 4. One additional capacitor which applies a ramp signal to the floating diffusion (FD) node to perform the PWM pixel readout is prepared.

Fig. 2 shows a timing diagram. Firstly, the voltage of FD (V_{FD}) is reset during the pixel reset period with the ramp signal (V_{RAMP}) set to be low. In the charge transfer period, V_{FD} is boosted to a high voltage by pulling V_{RAMP} up to the highest level to perform complete charge transfer from PD to FD. In the ADC period, V_{RAMP} increases linearly from the lowest voltage to the highest one. When V_{FD} reaches the threshold voltage of the in-pixel comparator, the pixel output voltage (V_{PIXOUT}) turns low. The time from the beginning of the ramp to the comparator output change is defined as a pulse width, which linearly changes according to the incident light intensity.

We have to pay attention to the operation condition for complete charge transfer when the PWM method is introduced into the 4T-APS. The requirement to the FD voltage is expressed as follows:

$$V_{FD,\,MAX} \sim V_{TH}+G_{RP}\cdot \Delta V_{RP} \geqq V_{DEP}+V_{MGN}+\Delta V_{SIG\,MAX}, \qquad (1)$$

where $V_{FD,\,MAX}$ is the FD voltage necessary for complete charge transfer, V_{TH} is a reset level, G_{RP} is a gain of the ramp signal, and ΔV_{RP} is the amplitude of the ramp signal. $V_{FD,\,MAX}$ has to be selected to be larger than the sum of the depletion potential, V_{DEP}, the electric potential margin between PD and FD, V_{MGN}, and the saturation signal level, $\Delta V_{SIG\,MAX}$. In addition, the amplitude of the ramp signal, ΔV_{RP}, is dependent on the power supply voltage, V_{DD}, and the gain of the ramp signal, G_{RP}, is represented by

$$G_{RP}=\Delta V_{FD}/\Delta V_{RP} < 1, \qquad (2)$$

where ΔV_{FD} is the amplitude at FD. Selection of V_{TH} is very important because it determines not only reset level but the boosting voltage which is limited by the amplitude of the ramp signal. Although boosting is necessary for operation of 4T-PWM, it is limited to the high-impedance nodes such as V_{RAMP} and TX.

Therefore, it is possible to reduce the overall power consumption[2].

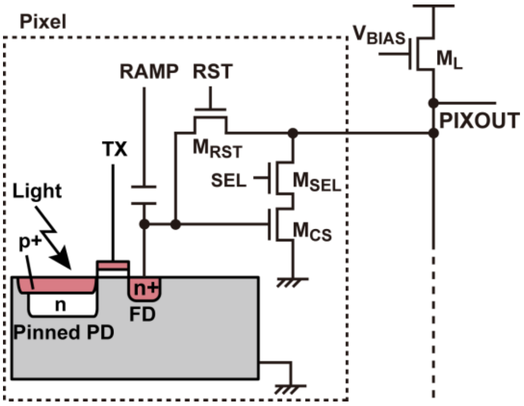

Fig. 1. Pixel circuit.

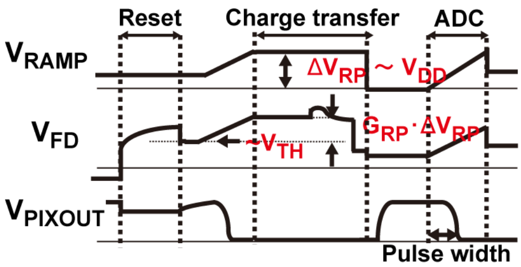

Fig. 2. Timing diagram.

3. Chip design

We examined the feasibility of the proposed pixel from the viewpoint of layout. Fig. 3 shows an example of pixel layout. The pixel pitch is 2.8μm based on 2-pixel sharing. The ramp capacity is embodied with parasitic inter-metal capacitance. A test sensor including the pixel and column digital circuits was designed. Table 1 shows the specifications of the image sensor which is assumed in this test chip design. Based on these specification, test pixels were fabricated in a 0.11μm CMOS image sensor technology.

Table 1. Assumed specifications.

Pixel pitch	2.8μm
Number of pixels	HD (2K×1K)
Frame rate	60fps
1H	15μs

4. Experimental result

Fig. 4 shows a preliminary experimental result of the prototype sensor. The PWM pixel readout is performed. Firstly V_{RAMP} is set to 0.4V and V_{FD} is reset. Then, V_{FD} is raised for complete charge transfer by setting V_{RAMP} to 3.3V. In the readout period, the ramp signal is linearly increased from 0V to 2.4V. Several pixel output waveforms for different illuminations are superimposed in Fig. 4. It is shown that the pulse width increases as the illumination becomes stronger.

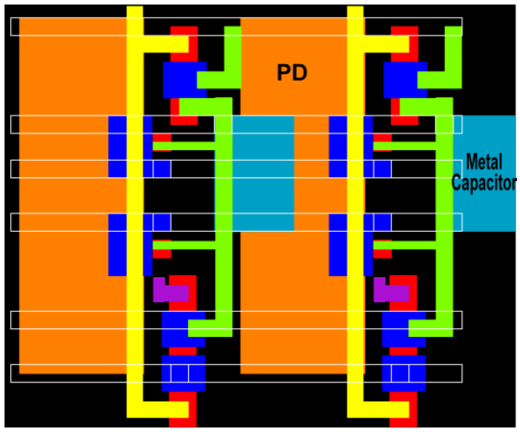

Fig. 3. Pixel layout.

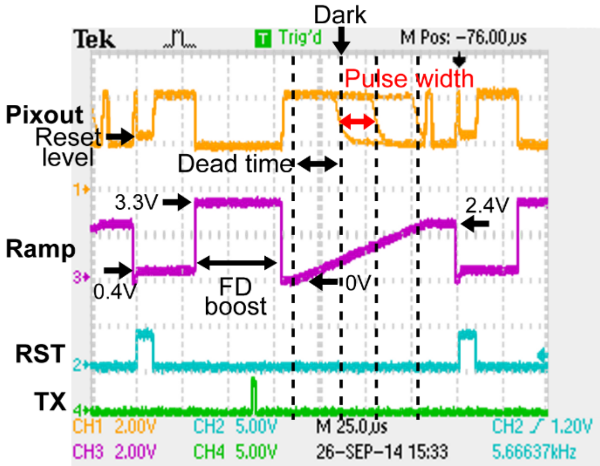

Fig. 4. Measured waveforms.

5. Conclusion

We applied the PWM pixel readout method to 4T-APS with a pinned photodiode for high quality imaging as well as low power consumption. The operation of the 4T-PWM pixel was confirmed experimentally with a test sensor.

6. Acknowledgement

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7. References

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