A Resolution-Reconfigurable 12b-to-8b Successive-Approximation ADC for CMOS Image Sensor

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Abstract This paper presents resolution-reconfigurable Successive-Approximation Analog-to-Digital Converter (SA ADC) for CMOS Image Sensor (CIS). Bridge capacitor enables Capacitive DAC(CDAC) to be narrow. ADC resolution can be selected 12-bit or 8-bit by controlling the MSB switch. In 8-bit mode, since 4-bit MSB capacitors of large sizes are not in use, power consumption is reduced. The power consumption and linearity performances from post-layout simulations of this SA ADC is shown.

Key words SA ADC, power consumption, CDAC, resolution-reconfigurable

1. Introduction

Recently, pixel-resolution of CMOS image sensor (CIS) is required to be more than that of full high-definition(Full HD = 1,920 * 1,080 pixels), and low-power consumption is a fundamental demand for battery-operated applications such as wireless surveillance systems. The power consumption of an Analog-to-Digital Converter(ADC) takes up a large part of the total CMOS imager. There are many types of ADC such as Single-slope, Successive-Approximation(SA), Cyclic, and Sigma-delta[1].

SA ADC has been utilized in various high-speed image sensors because n-bit A/D conversion requires only n clock cycles. Furthermore, the overall power dissipation of SA ADC can be quite low, since it requires only capacitors, switches, and a comparator, and since it does not require an op-amp. In this paper, SA ADC architecture is explored at simulation level for low-power CMOS imager designs such as for wireless surveillance system applications[2].

For power reduction, the resolution-reconfigurable operation from 8-bit to 12-bit is applied depending on the event detection. Moreover, for concerns in minimizing area, capacitive DAC (CDAC) is constructed using a bridge capacitor to implement 12-bit high resolution SA ADC in a small area.

2. Circuit Implementation

Fig.1 shows a conceptual block diagram of CIS system. Since the size of CDAC of a single-channel SA ADC is too large to be integrated in few micrometers of pitch, the proposed CIS system has a multi-column-parallel architecture, rather than the full column-parallel architecture.

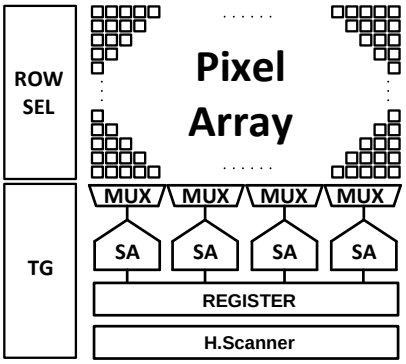

Fig.1. Conceptual block diagram of CMOS image sensor with multi-column-parallel SA ADC

The proposed SA ADC is shown in Fig.2. The size of CDAC is reduced by employing a bridge capacitor(C_A) in between the MSB and the LSB sides. It is also advantageous to the power consumption and to the speed of reference switching. However, the linearity of SA ADC can be vulnerable by the parasitic capacitors in LSB side, so it should be designed to minimize them[3].

In applications such as CCTV surveillance and dashboard cameras, it is very wasteful in power that column ADCs operates in high resolution mode while the system is in a standby state. In the proposed design, the resolution-reconfigurable of 12b-to-8b SA ADC is controlled using a switch located in the MSB side of CDAC as shown in Fig.2. When an event happens, the SA ADC operates in a 12b mode, so as to produce high quality images. On the other hand, if no sudden event has been detected, a

low-power 8b mode A/D conversion is conducted. The size of the mode control switch is decided to optimize the settling speed of DAC switching in the 12b mode.

Fig.3(a) shows the global shift registers used for generating clocks for A/D conversions. The mode control clock (ϕ_{MODE}) enables shift register to change its timing outputs depending on the event detections, as shown in Fig.3(b) with the A/D conversion mode reconfigured.

3. Simulation results

The prototype ADC is fabricated in a 0.18um 1P5M CMOS process. Assumming a pixel pitch of 2.6um and 20 columns per a ADC, one channel SA ADC is deigned 50um wide as shown in Fig.4. CDAC is implemented using metal-finger capacitors, and the mode control switch is located in between the MSB and the LSB capacitor arrays.

The proposed SA ADC operates in a 1.8V supply with 12b-to-8b reconfiguration modes at 1MS/s conversion speed. The post-layout simulation results of one channel SA ADC is shown in Fig.5. In a 12-bit mode, SFDR and SNDR are 81.1dB and 70.5dB, respectively, while, in a 8-bit mode, those are 58.7dB and 46.5dB. The power consumption of SA ADC is 110uW and 77uW in a 12-bit and a 8-bit modes, respectively, with 30% power saving reduction from 12b to 8b resolution reconfiguration.

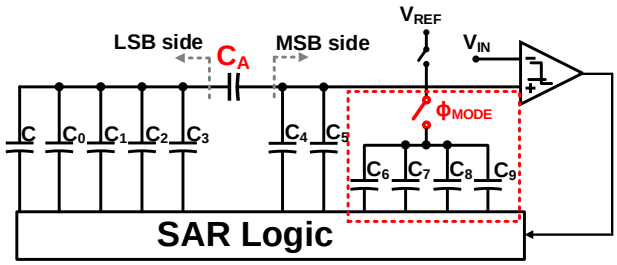

Fig.2. Proposed SA ADC

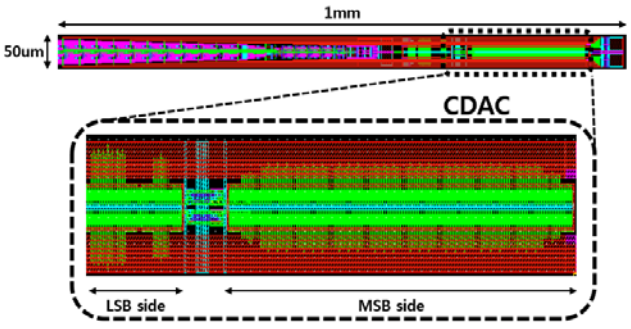

Fig.4. Layout of single-channel SA ADC

4. Conclusion

A resolution-reconfigurable 12b-to-8b SA ADC for CMOS image sensor applications is proposed. Thanks to the bridge capacitor, the CDAC is designed in a size-efficient manner that helped result in a narrow-pitched SA ADC design for a high resolution. The mode control switch, located in the MSB side of CDAC, is used to control the resolution of SA ADC to reduce power consumption in CCTV surveillance and dashboard camera applications.

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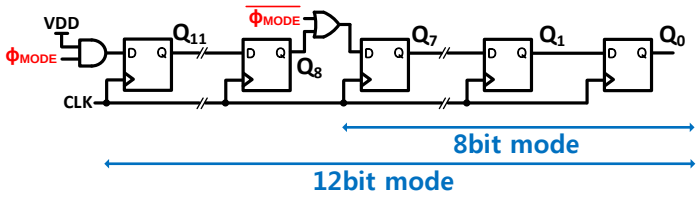
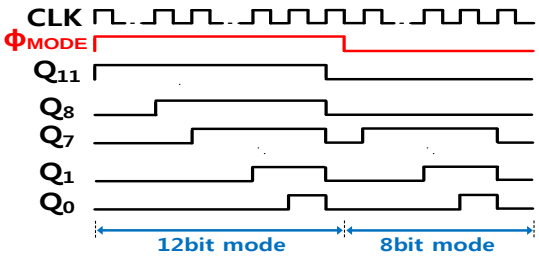
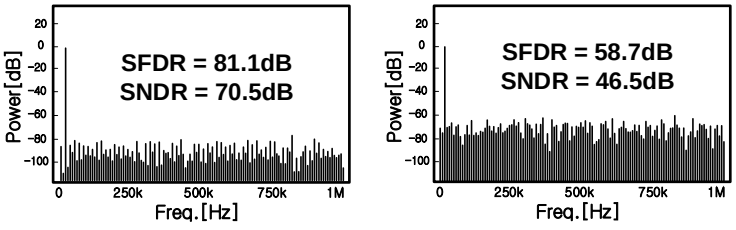


(a)



(b)

Fig.3. Resolution-reconfigurable shift register & timing diagram



(a) 12bit mode **(b) 8bit mode**

Fig.5. FFT results of post-layout simulation