[Invited] A 2-D/3-D image sensor with PPD-based lock-in pixels

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Abstract This paper presents an image sensor with PPD-based lock-in pixels to provide high-quality 2-D color image and high-accuracy 3-D depth map in a time-multiplexed manner. The prototype chip demonstrates the demodulation of 20 MHz time-of -flight signal with the contrast of 52.8%.

Keywords: CMOS image sensor, depth, lock-in pixel, pinned-photodiode, time-division, time-of-flight

1. Introduction

The interest and demand on 3-D cameras to provide depth information is getting increased in several applications such as the interactive user interface through the gesture control, unmanned vehicle and robot vision since the depth information doesn't only supply the distance to the object but also enables to track it without complex vision algorithm. Time-of-Flight (ToF) technique is one of most suitable candidates for acquiring the 3-D image. Its main advantage is that all pixels can capture their corresponding depth data in real-time. However, most of image sensors based on ToF principle provide only the depth data with much lower resolution than commercial 2-D cameras [1]-[3]. Therefore, another normal image sensor for capturing color information is necessary to reconstruct 3-D scene including color and depth data. Complicated image registration is also required to compensate different field of view of each of 2-D and 3-D image, not being favorable for real-time applications.

To address this issue, image sensor architectures for capturing both 2-D and 3-D images in a single chip have been presented in recent year [4]-[6]. There are two architectures to implement the 2-D/3-D image sensor. One is a space-division multiplexing architecture in which some pixels are dedicated to measure the depth information [4]. Fig. 1(a) shows a conceptual pixel array

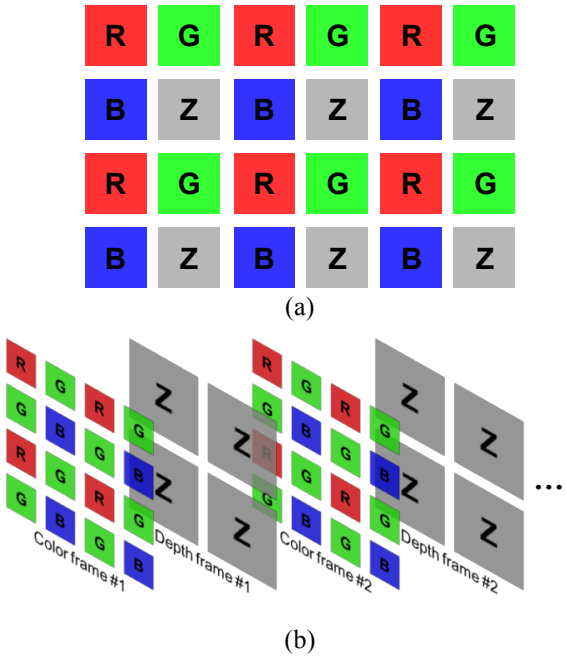

Fig. 1. 2-D/3-D imaging architecture with (a) the space-division multiplexing and (b) the time-division multiplexing.

with the space-division multiplexing architecture. Every Gb pixel in the bayer pattern is swapped over Z pixel. Because the operation principle and required photodiode of the Z pixel are quite different from those of the R/G/B pixels, simple replacement may not be possible so that the previous research [4] introduces interlaced RGBZ pixel array. The other is a time-division multiplexing architecture in which all pixels can capture both images alternately in each frame as shown in Fig. 1(b) conceptually [5], [6]. The complete separation of both different imaging modes simplifies the pixel design and optimizes the sensor operations at a particular frame.

In this paper, the time-division 2-D/3-D CMOS imager based on standard pinned-photodiode (PPD) device for obtaining both color and depth images is presented. The proposed pixel has two transfer gates for the lock-in capability to demodulate ToF signal. Eight-shared pixel architecture is employed to provide high-resolution color image and to improve the accuracy of the depth map by hierarchical binning operation at the expense of sacrificing a resolution.

2. Sensing Architecture

It is desirable to incorporate a small-size pixel with high pinning voltage for a high-quality color image, whereas a large-size pixel with low pinning voltage is required to generate accurate depth data. To overcome this contradiction, we propose two architectures; one is a split PPD for high spatial resolution, low noise, high sensitivity and high speed charge transfer capability, and the other is a hierarchical binning to increase the signal to noise ratio (SNR). Fig. 2 shows the overall architecture of the proposed sensor consisting of a pixel array, two readout circuit blocks and two row drivers with the micrograph of fabricated prototype sensor. Each pixel can provide its own

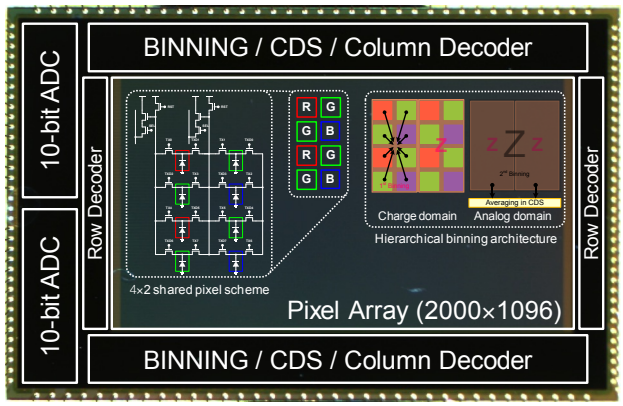

Fig. 2. Overall architecture with the micrograph of fabricated sensor.

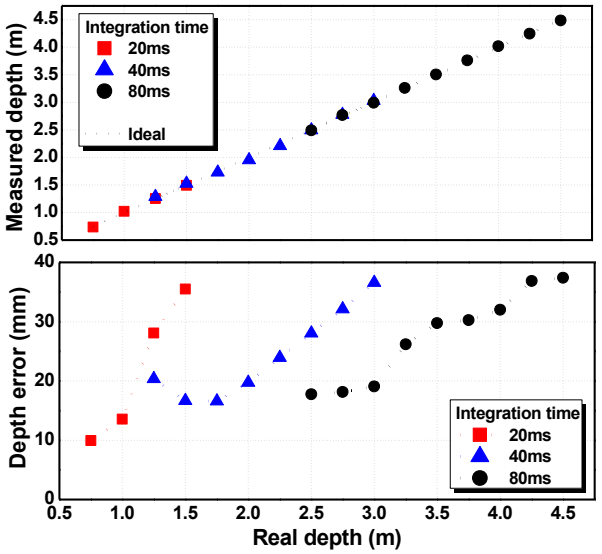

Fig. 3. Measurement results of extracted depth and its inaccuracy with different integration times from 0.75 to 4.5 m.

color information and 4 by 4 pixels are merged to a single depth pixel by the hierarchical binning scheme as represented in Fig. 2. In the depth image mode, two transfer gates are alternately turn on and off synchronized with modulated emitting light. Because eight pixels share a single floating diffusion node, generated electrons by reflected light are accumulated inherently in the charge domain. Every other column line is averaged in analog domain, increasing SNR once again. One of two transfer gates is activated in the color image mode and its operation is exactly the same as that of the conventional normal 4-T pixel.

The pixel pitch is 3.65 μm with 38.5% of the drawn fill factor. Even though a transport distance for the electron is short, the charge transfer speed may not be fast enough to demodulate over 10 MHz TOF signal because there is no electrical field in the middle of the PPD. To improve it, we propose two more techniques: one is a pinning potential adjustment and the other is a load distribution of TX signal line. Since the pinning potential level influences the quality of the color and depth images oppositely, it should be optimized [7]. We choose about 0.7 V pinning potential which is lower than typical value in conventional CMOS image sensor. Additionally, we divide the row signal lines for the transfer gates by two for reducing RC parasitic components by four times. These two signal lines are controlled by separate drivers deployed in the left and right side of the array as shown in Fig. 2. It is verified the 20 MHz operation using SPICE simulation with parasitic components.

3. Measurement Results

The prototype 2-D/3-D image sensor is fabricated using a 0.11-μm 1P 4M CIS process and fully characterized. No additional process for improving the depth extraction has been introduced. The size of the prototype is 9.7 × 6.2 mm^2 with 2000 × 1096 pixel array. 64 IR LEDs with 850 nm wavelength as the active light source is synchronized with the sensor by an external FPGA on a test board. Because the near IR is invisible to human eyes and transparent to the conventional color filter array, it is typical emitter in 3-D camera based on ToF principle.

In order to evaluate the performance of 3-D imaging, the demodulation contrast is measured and proposed pixel structure shows about 52.8% at 20 MHz frequency. In addition, 30 consecutive frames are captured to analyze the depth accuracy. The target object is the white flat panel located from 0.75 m to

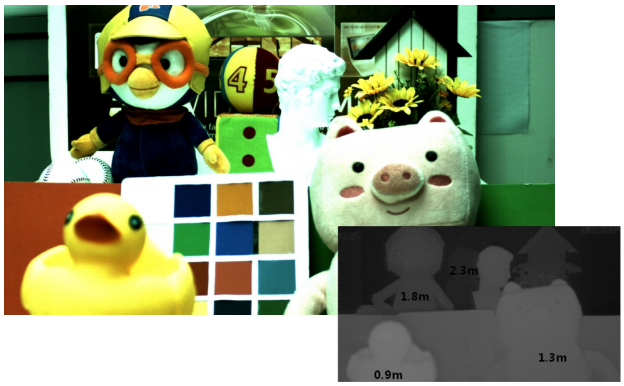

Fig. 4. Color and depth image taken from the prototype sensor.

4.5 m per every 0.25 m distance. Fig. 3 shows the measurement results with 20, 40 and 80 ms integration time to cover the full range. After 1st-order calibration to compensate the intrinsic phase delay between the emitter and the transfer gates, the non-linearity error is about 0.93% and the depth error is less than 38 mm at 4.5 m distance.

Fig. 4 shows the color and depth images taken from the prototype chip at indoor environment. A full-HD color image is reproduced by conventional image processing algorithms. The frame rate in the color image mode is 30 fps. The depth image with squeezed resolution owing to the binning operation clearly distinguishes four objects located at 0.9, 1.3, 1.8 and 2.3 m distance. The frame rate is about 14 fps with 30 ms integration time because two raw images are needed to the depth calculation.

4. Conclusion

A CMOS image sensor with the time-multiplexing capturing architecture is presented. Both 2-D and 3-D image modes are totally separated, easily optimizing the pixel configuration to each image. The proposed pixel architecture enables fast charge transfer, realizing the demodulation of 20 MHz ToF signal with over 50% contrast. The prototype sensor can successfully acquire a full-HD color image as well as a reliable depth map.

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