[Invited Talk] Radiation image sensor with SOI technology

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Abstract Radiation imaging sensors using Silicon-On-Insulator (SOI) technology have been developed. By using the SOI wafer, thick sensing region and CMOS readout circuit are implemented in a single die. Special process to realize such detector is developed in collaboration with a semiconductor company. The detector can be sensitive to many kinds of radiations, so various kinds of detectors are being developed through Multi Project Wafer (MPW) runs operated by us. The SOI pixel detectors can achieve not only high-resolution and good-sensitivity imaging sensor, but also unique detectors necessary for scientific applications which include functions of trigger, ADC, TDC etc. in a pixel. Recent results and present status are described.

Key words SOI, radiation, imaging, sensor, pixel

1. Introduction

In high-energy accelerator experiments, semiconductor radiation detectors are indispensable entity to measure track and energy of elementary particles. For example, in CERN ATLAS experiment [1], which leads to the discovery of Higgs particle, more than 150 m^2 silicon strip and pixel detectors are used. However the present pixel detectors are hybrid of silicon sensor and readout LSI bonded with millions of metal bumps. Thus this method introduces unwanted materials in the detector and increases the production cost.

We have been developing monolithic pixel detectors by using Silicon-On-Insulator (SOI) technology. Fig. 1 shows a schematic view of the SOIPIX detector. The SOI wafer used is composed of a thick, high-resistive substrate (sensor part) and a thin low-resistive Si layer (CMOS circuitry) separated by a buried oxide (BOX) layer. Dopants of p and n type are implanted to the substrate to create p-n junctions and contacts/vias between the sensing nodes and top circuits are formed through the BOX. The main advantages of the SOIPIX are;

- There is no mechanical bump bonding, so obstacles, which will cause multiple scattering, are eliminated and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10fF), so large conversion gain and low noise operation are possible.
- Full CMOS circuitry can be implemented in the pixel, thus local data processing is possible.
- Cross section of single event effects caused by radiation is very small.
- A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- SOI transistors are known to work over a very large temperature range from 1K[2] to 600K.

Since the SOI detectors have sensitivity to many kinds of radiations such as charged particles, X-ray and infrared light, many researchers are joining in our collaboration [3] to develop their own detectors. We have been operating Multi Project Wafer (MPW) runs of this process periodically (~twice/year) to ease the development of many kinds of chips.

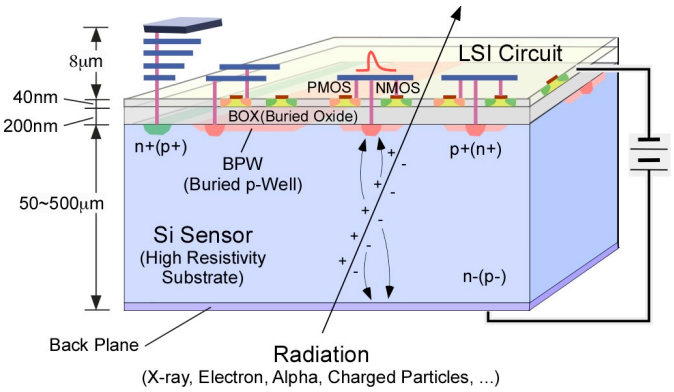

Fig. 1. Schematic view of the SOI Pixel Detector.

2. SOI Pixel Process

The process is developed based on a 0.2μm Fully-Depleted SOI CMOS process [4] of Lapis Semiconductor Co. Ltd. It is 1 poly and 5 metal layer process, and diameter of the wafer is 8 inch.

One of the main difficulties to build this kind of radiation sensors using the SOI wafer is a back-gate effect. Since the sensor and the transistors are located very near (~200 nm), transistors become conductive when high voltage is applied to the sensor (back-gate effect). To shield the electric field coming from the sensing region to the transistor location, we introduced Buried Well (BW) process. We implant p (n)-type dopant through the top Si layer to create a buried p (n)-well region (BPW (BNW)) under the BOX. The BW regions are connected to a fixed voltage or input preamolifiers, so the transistor characteristics are not affected from the sensor voltage.

As for the backside of the wafer, following processes are

performed normally; i) mechanical grind to desired thickness, ii) wet etching by 40μm, iii) implant of n (p) dopant to n (p)-substrate (depth ~ 0.5μm), iv) Aluminum plating (~200 nm). Applications, which require thin dead layer such as low-energy X-ray measurements, will use different backside processing.

We have been mainly using high-resistive SOI wafer from standard products of SOITEC Co., which is made in Czochralski (Cz) method (called HR1 wafer, ~700 Ωcm resistivity). However, in many case, it is desirable to get much higher resistivity to create thicker depletion depth with lower voltage, so we have also developed Floating Zone (FZ)-SOI wafer in which substrate has higher resistivity.

With 500 μm thick substrate, more than 90 % detection efficiency is achieved for 2~12 keV X-rays and 10 % for 30 keV X-rays.

3. Pixel Detectors

There are many activities for the SOI pixel detectors, but here only two examples are shown.

Integration Type Pixel Detector (INTPIX)

Main SOI detectors developed so far are integration-type pixel detectors [5]. The circuit is similar to that of the CMOS optical imager. Smallest size of the pixel we have developed is 8 μm square and largest detector has about 2 Meg pixels. Most of the integration-type pixels have correlated double sampling (CDS) circuit in each pixel or in column location. A photograph of the detector (called INTPIX4) and an example of X-ray image taken by the detector is shown in Fig. 2.

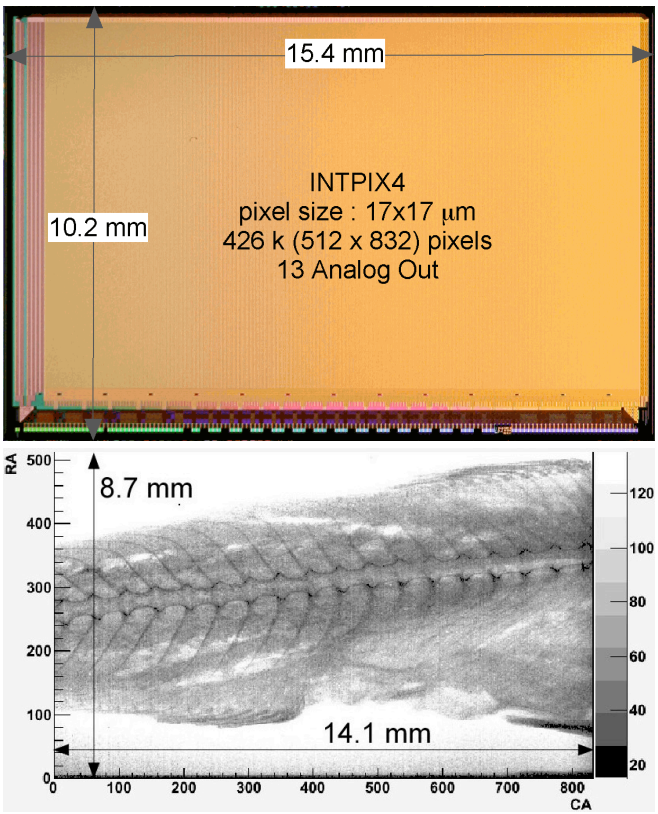

Fig. 2. (top) Photograph of the INTPIX4 detector. (bottom) an example of X-ray image taken by the detector.

The INTPIX4 detector has 13 parallel analog output and gain of ~13 μV/e-. It shows Contrast Transfer Function (CTF) of 78% for 20 line pair/mm.

X-ray Detector for Astrophysics (XRPIX)

The XRPIX detector [6] is beeing developed to use in X-ray astronomical satellite by Kyoto Univ. and KEK group. The basic structure of the detector is same as that of the integration type detector, but it also has a trigger generation function (Fig. 3) within the pixel. By using the trigger function and taking anti-coincidence with surrounding active shield system, background event caused by charged particles can be removed.

In addition to source-follower type pixel same as the INTPIX, Charge Sensitive Amplifier (CSA) type pixel detector is developed recently. The CSA type pixel shows higher gain and much better resolution compared to source follower type, and achieved noise level of 33 e- while source follower type has 76 e- noise level at -50 °C.

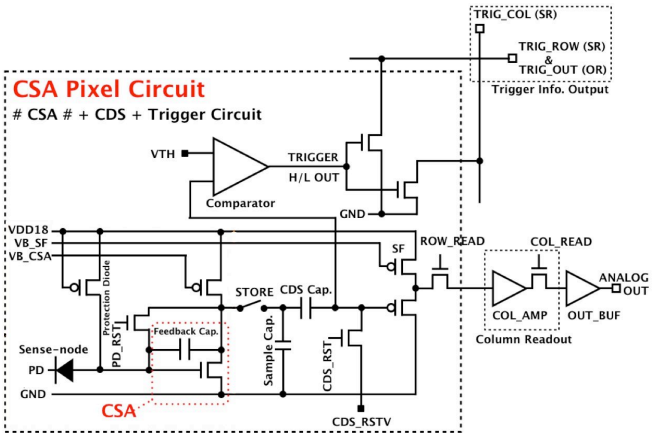

Fig. 3. Block diagram of the XRPIX detector with CSA amp.

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5. References

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