NIR SPADs and fast-gating circuits

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Outline

- InGaAs/InP SPAD
  - Device structure
  - Performance

- Circuits for InGaAs/InP SPAD
  - SPAD with integrated quenching resistor
  - GHz sinusoidal gating
  - Integrated fast-gated active quenching circuit (ASIC)
InGaAs/InP SPAD
Single-photon counting in the NIR (1 – 1.6 µm)

- Quantum Information Processing and Communication
- Quantum Key Distribution (QKD)
- Eye safe ranging (LIDAR)
- Unconventional (ghost, non-line-of-sight, ...) imaging
- Time-resolved diffused optical spectroscopy
- Photodynamic therapy (PDT) for cancer treatment
- Optical testing of VLSI circuits
- Photonics research in the 1 µm – 1.6 µm range

Detector + electronics tailored for the specific application!
Photons up to ~ 1.6 µm → $E_g < 0.8$ eV → **InGaAs** ($E_g \sim 0.75$ eV)  
But low $E_g$ means:

- higher noise → **cooling** is mandatory ($T \sim 230$ K)
- strong tunneling → higher $E_g$ material is required for avalanche → **InP** with $E_g \sim 1.35$ eV

**Separate Absorption, Charge and Multiplication (SACM)**

- **Absorption:** $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($E_g \sim 0.75$ eV)
- **Charge:** highly-doped **InP** ($E_g \sim 1.35$ eV)
- **Multiplication:** **InP** ($E_g \sim 1.35$ eV)

**Planar technology (no MESA)** for lower noise and higher reliability

**Front-illuminated** structure → Well-defined collection area

**Back-illuminated** structure → Suitable for arrays
InGaAs/InP SPAD

(Front-illuminated structure)
Design of InGaAs/InP SPAD

- Optimized double Zn diffusion (depths and diameters)
  - good uniformity in the active area ($\Delta V_{BD} < 4\%$)
  - no activation in the periphery

$\rightarrow$ Uniform sensitivity and low timing jitter

(Electric field simulation at 200 K & $V_{EX} = 5$ V)
Fabricated InGaAs/InP SPAD

(SEM cross-section) (top view)
I-V curve at low temperature

Low dark current: \( I_{\text{dark}} \sim 10 \text{ pA} @ V_{\text{BD}} - 1 \text{ V} \), sharp breakdown knee, large \( V_{\text{BD}} - V_{\text{PT}} \) difference

Temperature = 225 K
Active area diameter = 25 µm
Gated-mode operation

- SPAD is enabled during **Gate-ON time**
- SPAD is held OFF to empty traps → reduce afterpulsing
- **Gate period** $T_{GATE} = T_{ON} + T_{OFF}$
Good photon detection efficiency:
- 40% @ $\lambda = 1000$ nm, $V_{EX} = 5$ V
- 25% @ $\lambda = 1550$ nm, $V_{EX} = 5$ V
- still 3% @ $\lambda = 1700$ nm, $V_{EX} = 5$ V
Active area uniformity

$V_{EX} = 3\, V$

- Uniform sensitivity within the active area
- Sharp edges

Uniformity improves at higher excess bias
(due to saturation of avalanche triggering probability)
Low dark-count-rate InGaAs/InP SPAD

- DCR scales with active area $\rightarrow$ bulk origin (while dark current scales with perimeter, i.e. it is peripheral leakage)
- 10 $\mu$m InGaAs/InP SPAD with DCR of few kcps
- 10 $\mu$m SPADs have been fiber pigtailed (Micro Photon Devices – MPD)
Impact of design on dark count rate

25 times lower DCR at a given PDE by improving SPAD design

→ There is room for further improvement!
Temporal response

Sharp and “clean” time response \( \text{FWHM} < 80 \text{ ps} @ 7 \text{ V} \)

- Near Gaussian distribution
- Short exponential tail \( (\tau = 58 \text{ ps}) \)
Main drawback of InGaAs/InP SPADs: **afterpulsing**

- Some avalanche carriers get trapped in deep levels in InP multiplication region
- Delayed release triggers “afterpulse” avalanches

➔ **Limitation to maximum count rate**

Here is an example where different traps release carriers with different time constants (10’s or even 100’s μs!)

Temperature = 225 K
Excess bias = 5 V
$T_{ON} = 20$ ns

- Experimental data
- Exponential fitting:
  - $\tau_1 = 9$ μs
  - $\tau_2 = 22$ μs
  - $\tau_3 = 322$ μs
Circuits for high count rate InGaAs/InP SPAD systems
Afterpulsing reduction techniques for higher count rate

Reduce concentration of deep levels
→ challenging task (improved fabrication process)

Long hold-off time before re-arming
→ not an option at high rates

Reduce avalanche carriers

- **fast quenching** (monolithically integrated passive quenching or ASIC)
  → either gated or free-running mode
  → moderately high count rates (1–10 MHz)

- **short gates** (<< 1 ns): → very high (> 100 MHz) count rates
  → complex RF transients suppression
  → non-flat sensitivity

\[ \text{max count rate} = \frac{1}{T_{\text{hold-off}}} \]
SPAD with integrated quenching resistor
Others’ implementation (PLI NFAD):
- Thin film resistors (up to MΩ)
- Additional fabrication steps and masks required
- Slow re-arm (100 ns ÷ 1 μs)

PoliMi implementation:
- No additional fabrication steps:
  Zn shallow diffusion exploited
- kΩ resistor: - quasi-quenching
  - faster re-arm (< 100 ns)
Significant afterpulsing reduction

**Good temporal response**
- Faster recovery time with $\tau = 10$ ns

**Anode recovery transient**
- $V_{\text{EX}} = 7$ V
- $V_{\text{EX}} = 3$ V

**Excess bias**
- 2.5 V, 5 V, 7 V

**InGaAs module with**
- standard InGaAs/InP SPADs from the same wafer

### Graphs
1. DCR (cps) vs. Hold-off (µs) for:
   - InGaAs/InP SPADs with integrated resistor ($L/W = 50$)
   - InGaAs/InP SPADs with standard InGaAs/InP SPADs from the same wafer

2. Normalized counts (a.u.) vs. Time (ns) for:
   - $3$ V
   - $5$ V
   - $7$ V
   - Excess bias: 2.5 V, 5 V, 7 V

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**Specifications**
- **Temp:** 225 K
- **Freq:** 1 MHz
- **Gate-on:** 50 ns
- **Excess bias:** 2.5 V, 5 V, 7 V
- **L/W:** 50 (R ~ 50 kΩ)
- **Temperature:** 225 K
- **L/W:** 50 (R ~ 50 kΩ)
- **Anode recovery transient**
- **$\tau_{\text{RECOVERY}}$ ~ 10 ns**
Design of a compact module

Detector, front-end electronics and cooling housed in a small case

- Easy integration in optical setups
- Easy to use and configurable
GHz sinusoidal gating with SPAD-dummy balancing approach
Gating of InGaAs/InP SPADs

Square-wave gate

✓ Flat sensitivity (few %)
✓ Low time jitter (< 100 ps)

High avalanche charge
Low count rate

GHz sine-wave gate

✓ Short quenching time
✓ Very high count rate

Complex systems
Non-flat sensitivity

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Gigahertz sinusoidal gating - requirements

Gate signal at $f_G > 1 \text{ GHz}$ for fast avalanche quenching

$f_G$ tunable in a wide range (900-1400 MHz) for:
- Synchronization with different external laser systems
- Best trade-off between afterpulsing and detection efficiency

Adjustable excess bias:
- for optimizing PDE, DCR, afterpulsing, timing jitter
- Up to 7 V (27 dBm!)

Long-term stability
- Feedback for gate feed-through rejection

Suitable for rack mounting
PoliMi “SPAD-dummy” balanced configuration

- SPAD – Dummy couple
- Two gate sinusoidal signals in anti-phase for cancelling capacitive feedthrough
- Tunable wideband components (amplitude matching within 0.1%, phase matching within 0.05°)

Detectable avalanche
PoliMi sine-wave gate results:
(compared to square-gate system with similar SPAD)

At the same low afterpulsing probability: 1.5 % 1.5 % (*)
✓ Very high count rate 650 Mcps < 100 kcps
✓ Good peak detection efficiency ~ 30 % ~ 30 %
✓ Narrow temporal response < 70 ps < 70 ps

All results with 7 V excess bias unless specified – (*) $T_{ON} = 5 \text{ ns}$, $T_{HO} = 10 \mu\text{s}$
Gigahertz sinusoidal gating of InGaAs/InP SPAD

**Afterpulsing probability**

- Excess bias voltage, $V_{EX}$ (V)
- Afterpulsing probability (%)
- $f_{GATE} = 1.3$ GHz
- $T = 240$ K

**Photon detection efficiency**

- Wavelength, $\lambda = 1550$ nm
- $V_{EX}$ values: 7 V, 6 V, 5 V, 4 V
- Photon Detection Efficiency (%)
- Time (ps)

**Linearity**

- Input photon flux (a.u.)
- Count rate (cps)

**Temporal response**

- $V_{EX} = 7$ V
- $\lambda = 1550$ nm
- FWHM = 65 ps
Main board of the new system:

- All the basic blocks on board:
  - Gate generation
  - Gate amplification
  - Avalanche readout
  - Feedback control system

- PLL with multiple outputs generates both gate signals (800 – 1500 MHz)

- Programmable gain amplifier to set gate amplitude (up to $V_{EX} = 7$ V)

- Readout amplifiers with 3 GHz bandwidth and ultrafast comparator
SiGe integrated circuit for fast gating SPADs
Integrated circuit (SiGe BiCMOS technology):

- SPAD front-end based on “SPAD-dummy” approach
- Quenching time < 1 ns
- Very fast transition times (< 200 ps @ $V_{EX} = 5$ V)
- High repetition rate (up to 250 MHz)
- Low timing jitter (FWHM < 90 ps with InGaAs/InP SPAD, intrinsic < 20 ps)
- Mounted in a 12 pin TO-8 package → compact module
- Ready for arrays!
• Very fast rise/fall edges (< 200 ps @ $V_{EX} = 5$ V) $\rightarrow$ short gate (300 ps)
• Flat sensitivity ($\pm$15%) inside long gate windows
• Free-running mode available

Long gate (8 ns)

Short gate (300 ps)
Effective reduction of avalanche charge
→ lower afterpulsing even with long gate

![Graph showing SPAD Current vs Time for Discrete-components module and Fast-gated chip with V_{EX} = 5 V, T = 230 K, T_{ON} = 20 ns]

- Discrete-components module
- Fast-gated chip

![Graph showing Afterpulsing probability vs Time for Discrete-components module and Fast-gated chip with V_{EX} = 5 V, T = 230 K, T_{ON} = 20 ns]

- Discrete-components module
- Fast-gated chip

5X reduction of afterpulsing with long gate
Compact module built around integrated fast-gated chip

Compact module based on integrated circuit & InGaAs/InP SPAD

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum gate repetition rate</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Hold-off time</td>
<td>0.003 ÷ 1300 µs</td>
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<tr>
<td>Gate width</td>
<td>0.3 ÷ 1000 ns</td>
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<tr>
<td>SPAD temperature</td>
<td>205 ÷ 290 K</td>
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<tr>
<td>Size</td>
<td>40 x 50 x 70 mm³</td>
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</tbody>
</table>
Conclusions

- **InGaAs/InP SPAD:**
  PoliMi experimental results (@ $V_{EX} = 5\, V$):
  - Low DCR (~ $10^3$ at 225 K)
  - Good detection efficiency (30 % @ 1550 nm)
  - Moderately low afterpulsing
  - Low timing jitter (FWHM < 90 ps)

- **Circuits for high-count-rate InGaAs/InP SPAD system:**
  - SPAD with integrated quenching resistor
  - GHz sinusoidal gate (SPAD-dummy balancing approach)
    - Very low afterpulsing (< 1.5%)
    - High count rate (> 600 Mcount/s)
  - Compact modules based on fast-gating ASIC
    - Trade-off between standard modules and GHz gating

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Waiting for you at Single Photon Workshop 2019 in Milano!