Outline

- CMOS SPAD – motivation
- Two ended vs. Single Ended SPAD (bulk isolated)
- P+/N two ended SPAD and its optimization
- Application of P+/N two ended SPAD
- NIR enhanced N+/P SPAD scheme
- QE optimization device and optics
- SiPM and its density optimization
- Source Follower as an amplifier
Single Photon Detection

- OOPs – the wrong presentation, this is 4T pinned photo diode pixel – 1e noise, very high sensitivity
- So, why SPAD – People say, it’s all about timing …

Images at starry night – 0.6 mili-Lux!!!!

(10 micron pixels)

5 meters

10 meters

15 meters
Stand alone SPAD can be well optimized
- using minimal mask count
- any desirable operating voltage
- High performance

SPAD embedded in CMOS/CIS process
- Somewhat inferior for the features above,
  However:
- Allows monolithic on chip quenching, readout, and other circuitry
- Enable CIS optimized pixel on same chip with SPADs
Can one add low voltage circuitry in series to the SPAD?

- Single Ended SPAD can have better NIR response but it’s harder to use fancy quenching
- “Two Ended” SPAD

Problems:
- Single Ended SPAD can have better NIR response but it’s harder to use fancy quenching
P+/N “Two Ended” SPAD optimization

Schematic cross section of the SPAD

Simulated Doping Concentration on a vertical cut line
TCAD Process Simulation Results-

Simulated half SPAD structure (Doping Concentration)

- Avoiding Early Edge Breakdown by Virtual Guard ring

Simulated SPAD IV curve

- BV~19V
- BV~13.9
- BV~12V

Avoiding Early Edge Breakdown by Virtual Guard ring
Electrical Fields and Impact Ionization Rate

Simulated electrical fields at -14V on the Anode (process A)

Simulated Impact Ionization rate at -14V on the Anode (process A)

Simulated electrical fields on the vertical cut line (A, -24V, B, -18V, C, -14V on the Anode)

Simulated Impact Ionization rate on the vertical cut line (A, -24V, B, -18V, C, -14V on the Anode)
DCR vs. Excess Bias (room temperature)

- DCR is exponential in excess voltage
- Inversely depends on breakdown voltage

**Measured DCR density vs. Excess bias at room temperature**

<table>
<thead>
<tr>
<th>Process split</th>
<th>BV [V]</th>
<th>DCR Density [Hz/um²], RT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-12.41</td>
<td>21</td>
</tr>
<tr>
<td>B</td>
<td>-14.54</td>
<td>4.6</td>
</tr>
<tr>
<td>C</td>
<td>-20.13</td>
<td>1.5</td>
</tr>
</tbody>
</table>

At 3.3V excess bias:
Photon Detection Efficiency Spectrum and Excess Bias dependency

- PDE linearly dependant on excess voltage
- Low PDE for NIR

Measured PDE vs. Excess bias (passive quenching circuit)

<table>
<thead>
<tr>
<th>Process split</th>
<th>BV [V]</th>
<th>PDE [%] Blue 470nm</th>
<th>PDE [%] Green 530nm</th>
<th>PDE [%] Red 660nm</th>
<th>PDE [%] NIR 880nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-12.41</td>
<td>20.93</td>
<td>15.93</td>
<td>7.3</td>
<td>2.03</td>
</tr>
<tr>
<td>B</td>
<td>-14.54</td>
<td>16.13</td>
<td>12.69</td>
<td>6.63</td>
<td>1.55</td>
</tr>
<tr>
<td>C</td>
<td>-20.13</td>
<td>12.07</td>
<td>9.09</td>
<td>6.91</td>
<td>1.33</td>
</tr>
</tbody>
</table>
P+/N  SPAD Application – Gunshot Detection

Application works in visible light

2nd Generation can be monolithic since TowerJazz can join CIS pinned photodiode and SPAD within the same process

**System Description**

1) Commercial high resolution CMOS imager for the spatial SPAD synchronization
2) FPGA commercial carrier board used for operating the SPAD image sensor and signal processing of its output data
3) A CMOS SPAD image sensor placed on a mezzanine board
4) Specially-designed opto-mechanical system for the SPAD image sensor.
5) Narrow-band optical filter

Muzzle flash emits photons at $\lambda=766$[nm]
Device and Pixel Architecture

- SPAD pixel Layout
- 64x64 SPAD Imager Layout
- SPAD pixel Block Diagram
N+/P Single Ended SPAD

- Implemented on 5.5µm epi – 30Ωcm
- Note bulk to epi doping gradient
TCAD Process Simulations Results -

- Low fields on diode edge – avoiding edge breakdown

Simulated half SPAD structure (Doping Concentration)

Simulated electrical fields at 21V on the Cathode
Electrical Fields (magnitude) - simulated -

- Electrical field is small out of multiplication region
- Good agreement of IV curve between simulations and measurements

Simulated electrical fields and potential on the vertical cut line (21V on the Cathode)

Simulated and Measured SPAD IV curve
- PDE at 905nm 3.2% averaged on cell pitch
- Low DCR
- Acceptable DCR even for 100C!

Meas. by Niclass 2015
- DCR is weakly dependant on excess voltage
- Jitter is small and suitable to automotive demands

Measured mean DCR density vs. Excess Bias, room temperature

timing response @ 5V Excess Bias to a 635nm laser diode emitting 100 psec overall timing jitter of ~160 psec FWHM.
SPAD with depleted low doped region

- Reach-Through SPAD
- Quit old concept
- From: Opto-Electr Rev. 5 no. 2 1997

Cross Section

Field Profile

Doping Profile
Fully depleted 9µm High Res SPAD Simulations

- Similar SPAD structure – starting material and implants change
- Breakdown - simulated 36V measured 38V
- Significant field deep in the epi -
- Average QE at 905nm enhanced from 3.2% to 4.6%

![Simulated Potential vs. depth](image1)

![Simulated Field vs. depth](image2)

![Edge Optimization](image3)
SiPM – Silicon Photo Multiplier

- Array of SPADs
- Hard wired or capacitively coupled SPADS
- Benefits:
  - Timing + number of photons
- Cons
  - Slower rise time
  - Sensitive to “screaming” SPADs
  - More prone to X-talk
Optimization of Layout Of an SiPM

- Guard Ring is minimized
- Rounded corners instead of circles
- High Resistivity poly resistors 10kΩ/
- Fine optimization of cell size
  - Fill Factor
  - Microlenses
  - Capacitance
- No evidence for screaming SPADs nor for cross talk
Elevated Microlenses Optics

- SPAD suffers from low fill factor
- SPAD diodes pitch is relatively large – hard to make effective microlenses
- For long focal length lenses should be put high above the B/E
- Tower developed large elevated microlenses
- With elevated microlenses we expect effective QE of about 7%
- Targeting effective QE of 10% at 905nm after further device optimization

Normalized PDE mapping of SPAD area, Niclass 2014

Elevated “Big” Microlenses
Dead time and Active Quenching

- SPAD capacitance is between 10fF-30fF depends on layout
- RC time with 250kΩ resistor is below 10ns, which is probably good enough for Automotive applications
- We are working on “tricky” quenching circuits that can improve by shortening and better defining the dead time
Capacitive Coupled Monostable Recovery Circuit
Summary

- CMOS-SPAD was developed on platform supporting 0.18µm CMOS (1.8V/3.3V or 1.8V/5.0V) and CIS state of the art pixels
- “Single Ended” and “Two Ended” version were developed
- Optimization was mostly focused on effective PDE in the NIR – Layout, Starting Material, Implant Scheme, and pixel optics
- Some special process modules were developed i.e. super high resistor, large microlenses and microlens elevation
References