EFFECTS OF RADIATION ON CHARGE-COUPLED DEVICES*

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The effects of 1-MeV electron irradiation upon the performance of two-phase, polysilicon-aluminum gate CCDs will be reported. Both n- and p-surface channel and n-buried-channel devices were investigated using 64- and 128-stage line arrays. Characteristics measured as a function of radiation dose include: transfer inefficiency, threshold voltage, field effect mobility, interface state density, full-well signal level and dark current. Surface-channel devices were found to degrade considerably at less than 10^5 rads (Si) due to the large increase in the fast interface state density caused by radiation. Buried-channel devices maintained efficient operation to the highest dose levels used [5×10^5 rads (Si)].

I. INTRODUCTION

Since CCDs consist of arrays of MOS capacitors, it is expected that many of the permanent radiation effects seen in MOS devices and circuits will also occur in CCDs; namely, oxide charge (Q_{ox}) buildup and increase in fast interface state density (N_{ss}). However, the effects of these interface changes upon CCD performance are expected to differ considerably from their effect upon MOSFET performance. This is basically because a MOSFET operates in

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thermal equilibrium with an infinite supply of charge from the source, while a CCD operates in nonthermal equilibrium with a fixed amount of charge as a signal. Surface-channel CCDs (SCCCDs) are very sensitive to fast interface state levels but relatively insensitive to threshold voltage changes. Both SCCCDs and buried-channel CCDs (BCCCDs) are sensitive to dark current levels. The situation is just reversed for MOSFETs.

This paper reports the results of a study of the effects of radiation (1-MeV electrons) on CCDs, both surface- and buried-channel, to establish both the nature of the radiation effects and a baseline for the radiation tolerance of present-day (unhardened) CCD technology. The test vehicles used were two-phase linear CCD registers with 64 and 128 stages, with polysilicon-aluminum gate construction (Ref. 1). Figure 1 shows a cross-sectional view of a surface-channel device along with a photomicrograph of a 128-stage register.

II. SURFACE CHANNEL RESULTS

Figure 2 shows a plot of the threshold voltage of the polysilicon and aluminum gates vs. radiation dose for an n-channel SCCCD. The negative shift in threshold voltage indicates a buildup of positive oxide charge of 1.9×10^{11} charges/cm^2 for the polysilicon gates and 2.7×10^{11} charges/cm^2 for the aluminum gates after a dose of 10^5 rads (Si). This oxide charge buildup necessitated changes in dc operating points of the various control gates and phase electrodes to maintain full signal levels and proper fat zero levels. However, since all gates are accessible, it is possible to do this.

More serious, however, is the buildup of fast interface state density. N_{ss} was measured by varying the number of zeros between strings of ones (Ref. 2). N_{ss} is proportional to the slope of ϵ vs. ln (n_{zero}), where n_{zero} is the number of zeros between ones. This type of plot is shown in Figure 3; each curve corresponds to a different dose. Figure 4 is a plot of N_{ss} determined in this manner vs. dose and indicates the sharp increase in N_{ss} from 10^{10} to 10^{11} $(cm^2\text{-eV})^{-1}$ which occurs between 10^4 and 10^5 rads (Si). This increase in N_{ss} results in an increased transfer inefficiency (ϵ), as shown in Figure 5, for all levels of fat zero. Since the lowest inefficiency attainable is limited by edge effect trapping (Ref. 3), it is not surprising that the 30% fat zero curve increases by an order of magnitude when N_{ss} does the same. The seriousness of this effect would be increased when narrower channel devices are used as would be the case

with imagers or memories. This increase in transfer inefficiency due to radiation-induced buildup of N_{ss} severely restricts the usefulness of surface-channel CCDs in a radiation environment. It also suggests that buried-channel devices should be superior in this respect since they are free of interface state trapping effects.

III. BURIED-CHANNEL RESULTS

Similar oxide charge buildup is also observed in BCCDs, as indicated in Figure 6, which is a plot of the channel turn-on voltage vs. dose. While this effect does not affect transfer efficiency, it does affect maximum well size (signal) unless changes are made in the dc operating points of the phase electrodes. This is illustrated in Figure 7, which shows the maximum signal vs. dose for the initial dc conditions and for conditions adjusted for maximum signal. No serious degradation in full-well signal is observed if adjustment is made.

Figure 8 shows transfer inefficiency vs. dose for n-channel BCCDs. No significant increase in ϵ is observed up to 10^5 rads (Si), indicating that no interface trapping is occurring. Some increase is observed at 3×10^5 rads, but the absolute level remains satisfactory for most applications. Finally, Figure 9 shows dark current vs. dose for several different devices as measured by continuous operation and in an integration mode. No serious increases are observed up to 3×10^5 rads (Si). Neutron irradiation and the resulting displacement damage may adversely affect dark current, however.

IV. SUMMARY AND CONCLUSIONS

Typical MOS radiation effects were observed: oxide charge and fast interface state density buildup. The increased interface state density severely degraded transfer efficiency in surface-channel devices but had little or no effect on buried-channel devices. Oxide charge buildup required adjustment of dc operating points to maintain signal level. Since all gates of CCDs are externally accessible, it appears feasible to automatically adjust dc levels using on-chip threshold tracking circuits. If this is done in conjunction with buried-channel devices, it appears that CCDs can be as radiation hard as adjacent MOS circuits and should maintain satisfactory performance at least to the 5×10^5 rad (Si) level. Displacement damage caused by neutron damage could increase dark current levels and should be experimentally investigated.

REFERENCES

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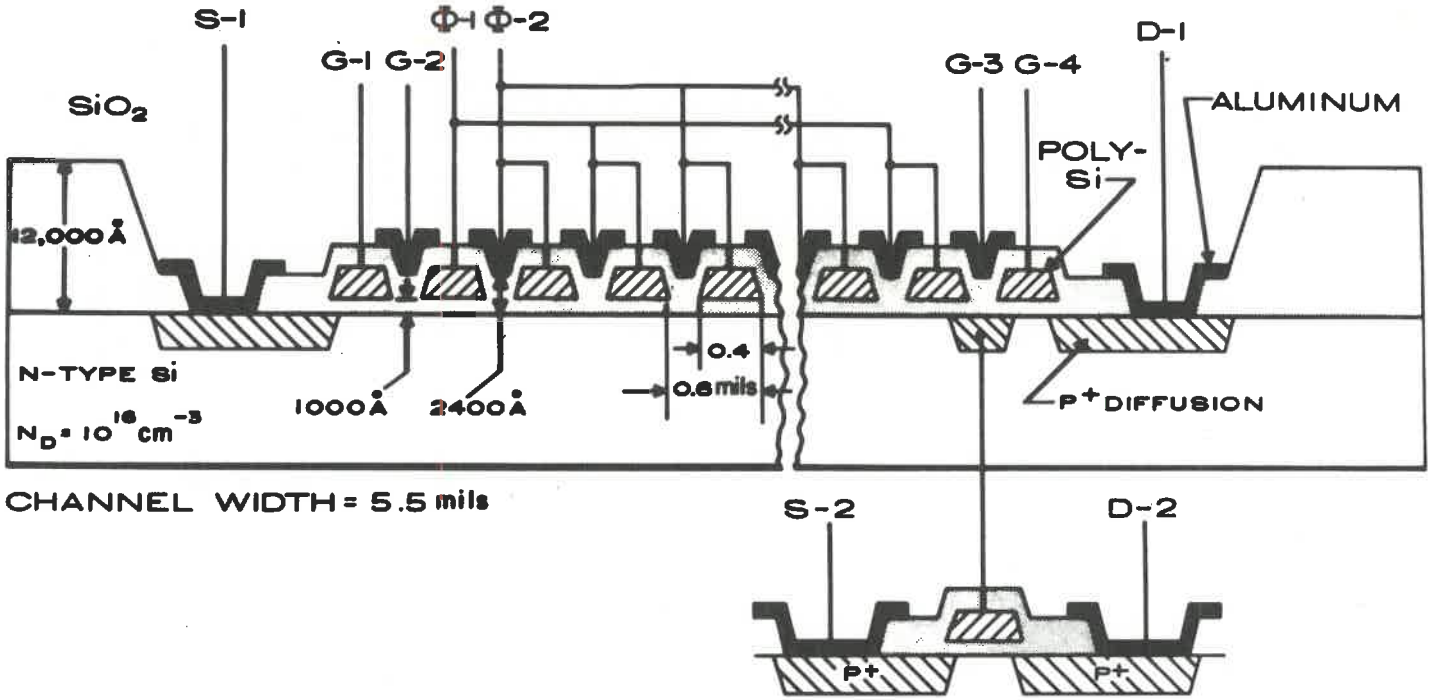
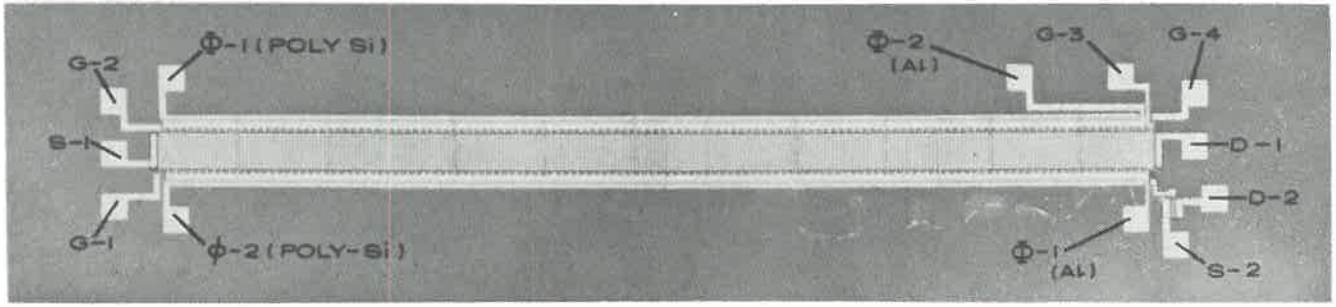
2. J. E. Carnes and W. F. Kosonocky, "Fast Interface States Losses in Charge-Coupled Devices," Appl. Phys. Ltrs. 20, 261, April 1, 1972.

3. M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of Charge-Coupled Devices," IEEE Trans. on Elec. Dev. ED-20, 45, Jan. 1973.





128 STAGE SHIFT REGISTER

Figure 1. Cross section of two-phase surface-channel CCD

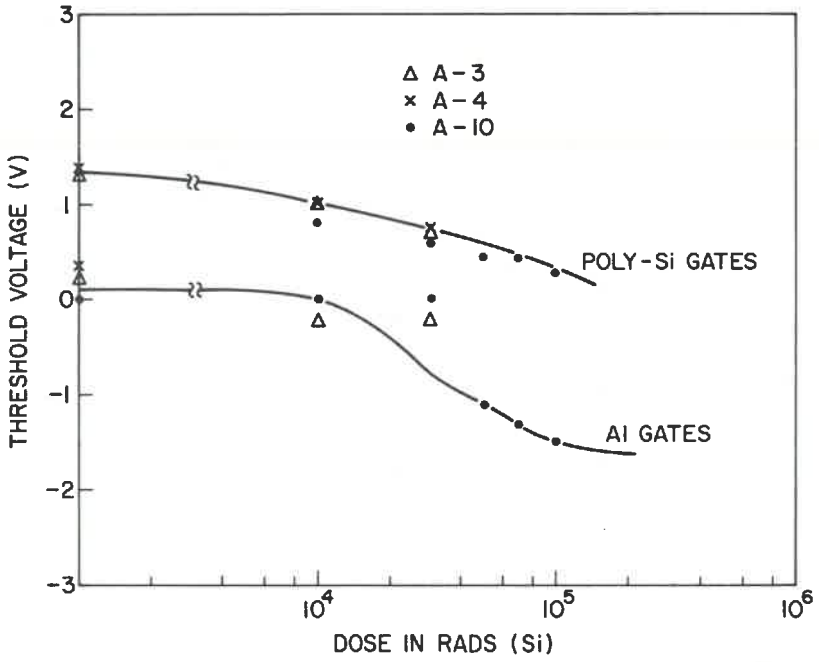


Figure 2. Gate threshold voltage vs. irradiation (n-channel, 128 stages)

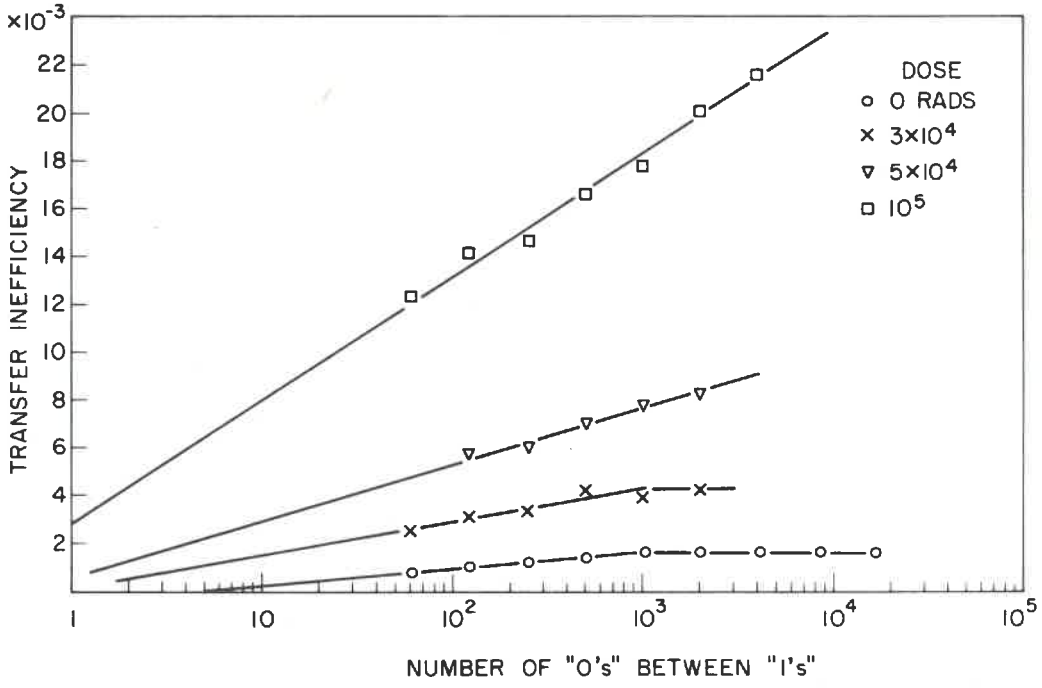


Figure 3. Transfer inefficiency vs. log (n_{zero}) (n-channel, 128 stages, device A10)

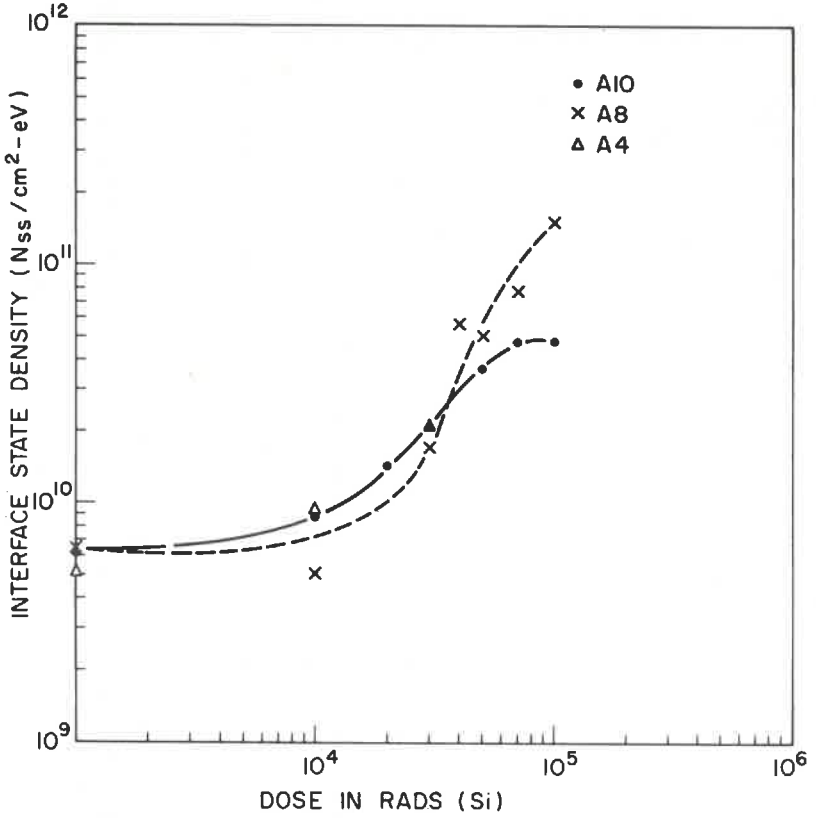


Figure 4. Interface state density vs. irradiation (n-channel, 128 stages)

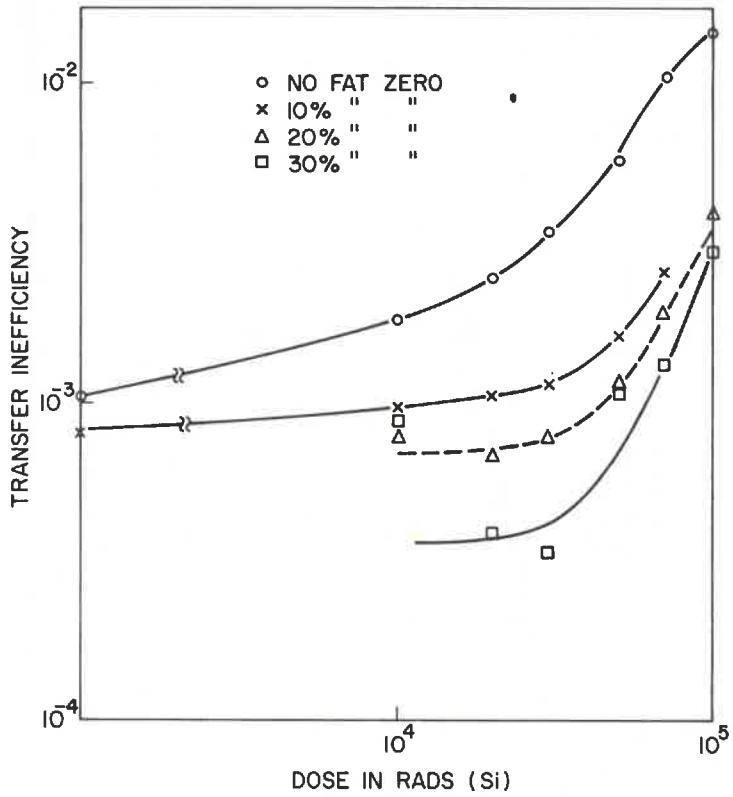


Figure 5. Transfer inefficiency vs. irradiation (n-channel, 128 stages, with fat zero)

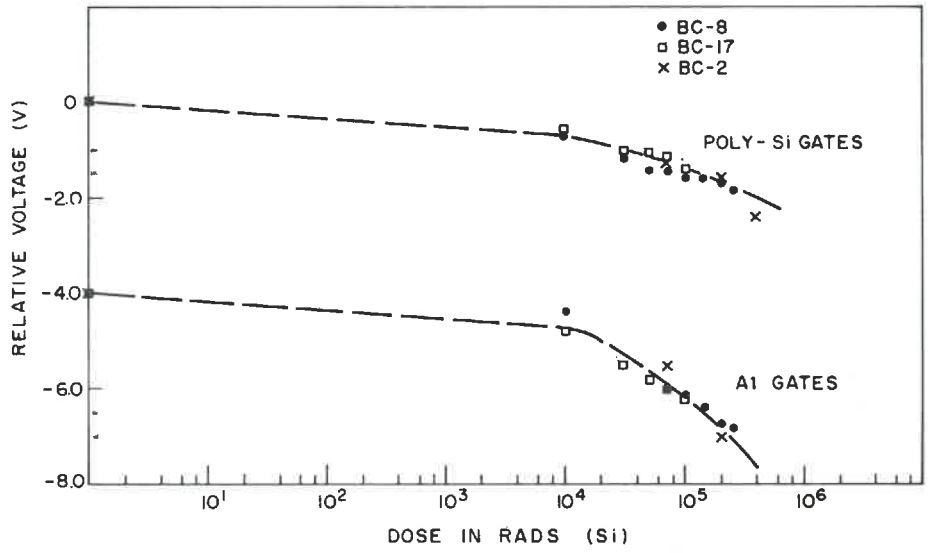


Figure 6. Channel turn-on voltage vs. irradiation (buried channel, 64 stages)

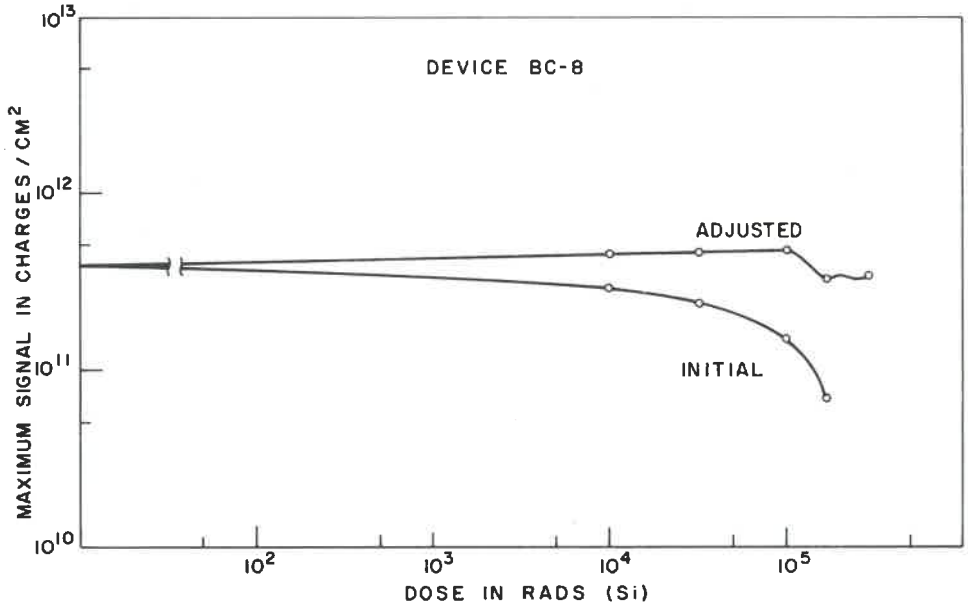


Figure 7. Maximum charge density vs. irradiation (buried-channel device)

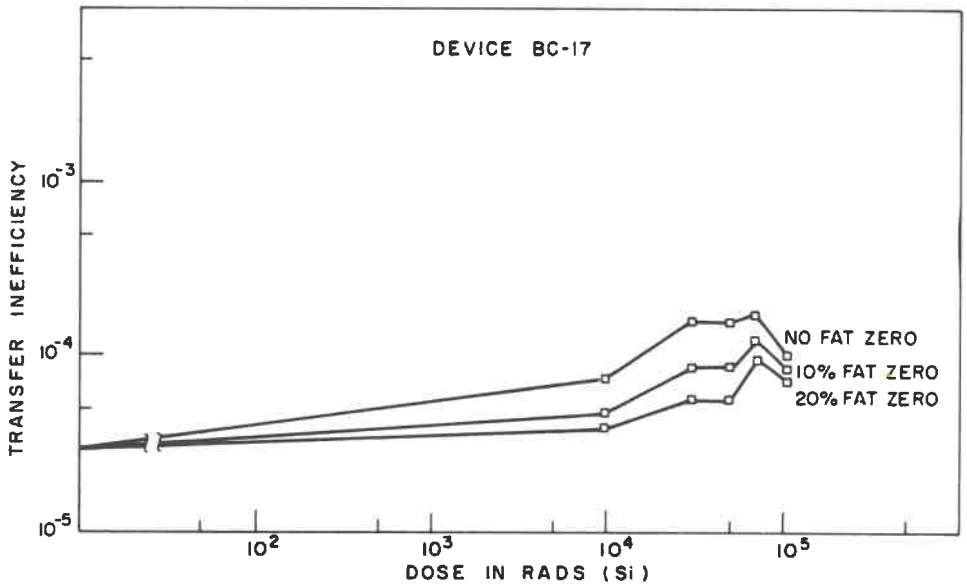


Figure 8. Transfer inefficiency vs. irradiation (buried-channel device)

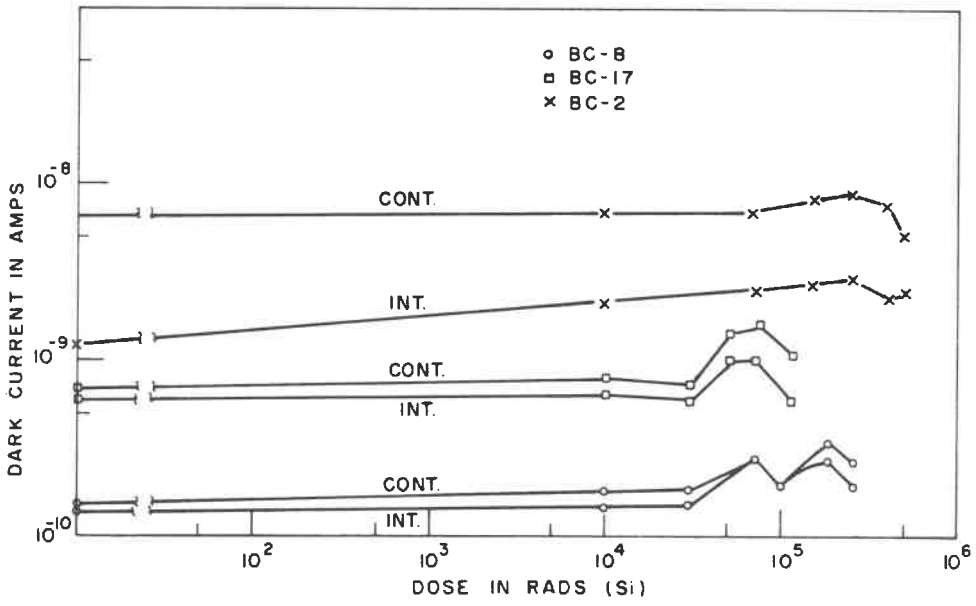


Figure 9. Dark current vs. irradiation (buried channel, 64 stages)