

# 1 GHz Multiple Output 128x256 Element Area Array

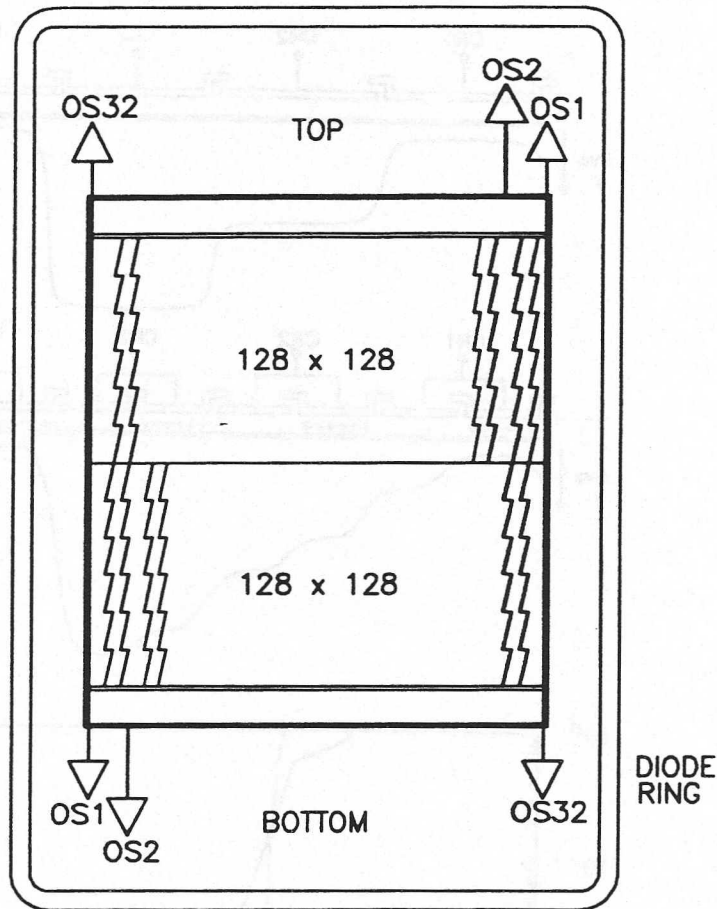
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## Abstract

A high speed imager capable of a 1 Gigahertz <sup>pixel</sup> ~~frame~~ rate was developed with 80 $\mu$ m x 80 $\mu$ m pixels. A photodiode, interline transfer pixel architecture is used with lateral antiblooming and exposure control capability. A special multi-phase readout shift register and parallel to serial transfer structure are designed for high charge transfer efficiency operation across a large 80 $\mu$ m pitch at high speed. The charge transfer efficiency is modelled analytically as well as with a 2-dimensional transient device simulator for both a conventional 4 phase and the special multiphase shift register.

A total of 64 outputs each designed to operate at 16 MHz are distributed around the array. In order to minimize power dissipation, a single output MOSFET operating in conjunction with an off-chip transimpedance amplifier was used. The configuration is compared to a conventional two stage source follower with respect to bandwidth, noise and physical size.



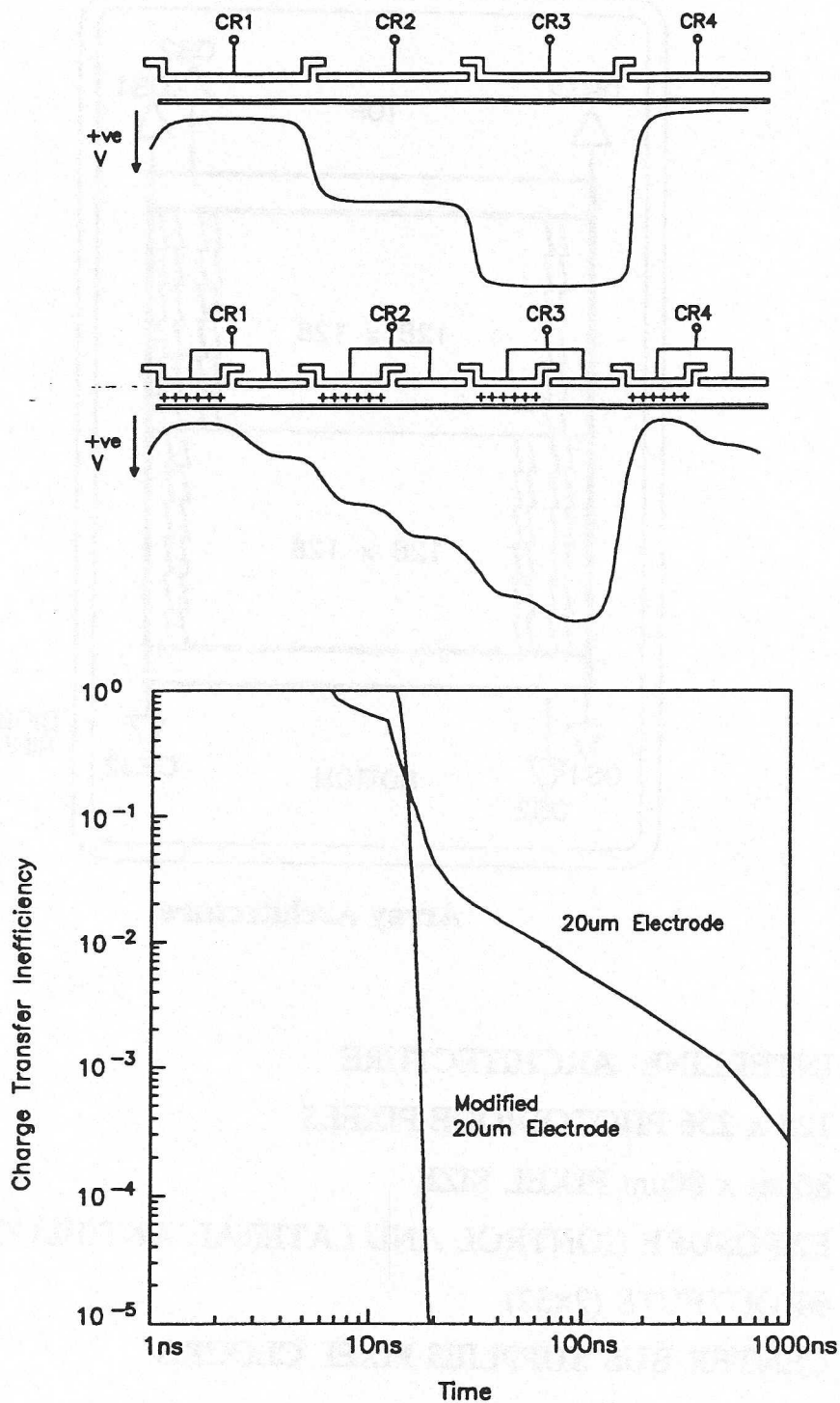
**Array Architecture**

- **INTERLINE ARCHITECTURE**
- **128 x 256 PHOTODIODE PIXELS**
- **80 $\mu$ m x 80 $\mu$ m PIXEL SIZE**
- **EXPOSURE CONTROL AND LATERAL ANTIBLOOMING**
- **64 OUTPUTS (2x32)**
- **CENTER BUS SUPPLIES PIXEL CLOCKS**

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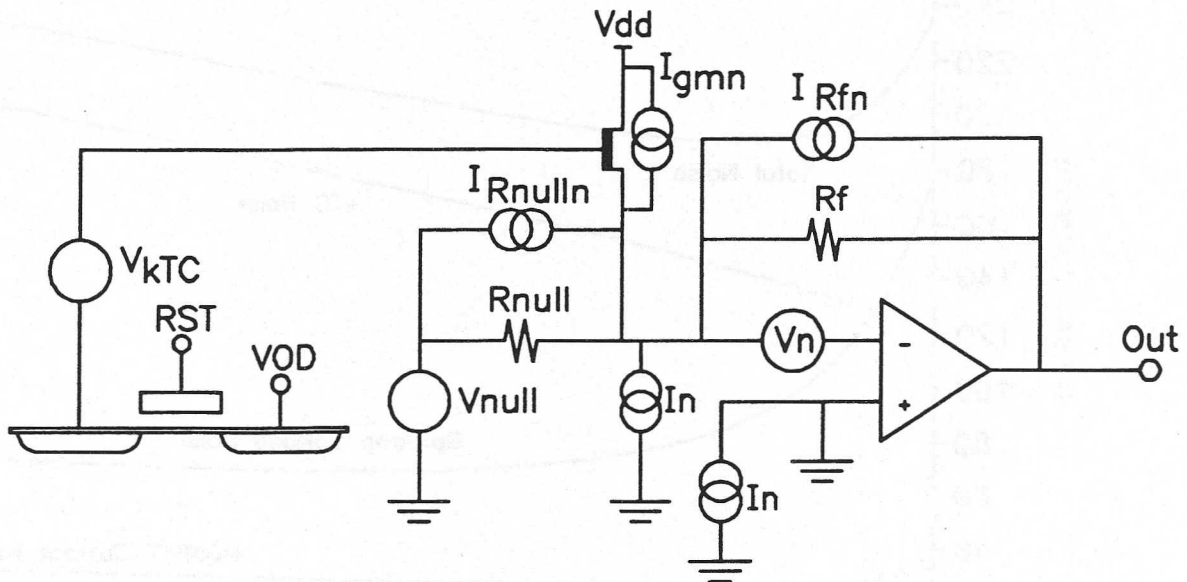
# MODIFIED HCCD STRUCTURE



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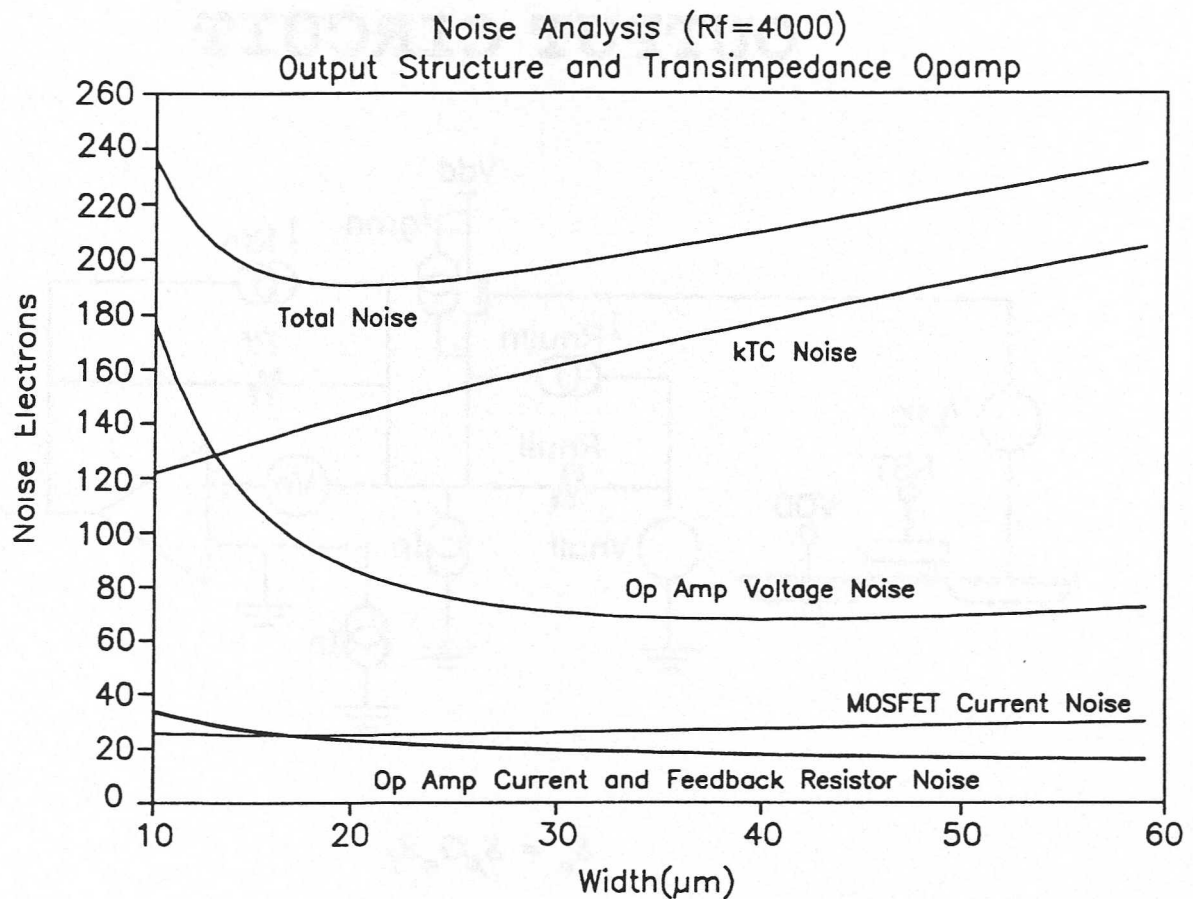
# OUTPUT CIRCUIT



$$S_o = S_{fd} G_m R_f$$

- A 25 $\mu$ m/5 $\mu$ m ON-CHIP SINGLE MOSFET IS CONNECTED TO AN OFF-CHIP OPAMP YIELDING A CURRENT MODE HIGH SPEED (10ns EDGES) CONFIGURATION THAT OCCUPIES LITTLE PHYSICAL SPACE ON-CHIP
- USING THE TRANSIMPEDANCE APPROACH WITH A 4000 $\Omega$  FEEDBACK RESISTOR THE TOTAL CONVERSION EFFICIENCY IS 2.4 $\mu$ V/e COMPARED TO 0.8 $\mu$ V/e IF THE ON-CHIP MOSFET IS CONFIGURED AS A SOURCE FOLLOWER WITH A MUCH LOWER BANDWIDTH
- CONFIGURATION OPERATES WITH REDUCED ON-CHIP POWER DISSIPATION

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- PLOT OF FLOATING DIFFUSION NOISE ELECTRONS TO MOSFET WIDTH (LENGTH =  $5\mu\text{m}$ )
- AT  $W = 25\mu\text{m}$  NOISE IS AT ITS MINIMUM - 190 ELECTRONS
- AS  $W$  INCREASE BEYOND  $25\mu\text{m}$ , kTC NOISE DOMINATES
- IF CDS IS USED TO ELIMINATE kTC COMPONENT, A LARGER  $W$  INCREASES GM AND THUS TOTAL CONVERSION EFFICIENCY
- FOR HIGH SPEED OPERATION, NOISE IS COMPARABLE TO A TWO STAGE SOURCE FOLLOWER

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