A Floating Gate Wide Dynamic Range Photodetector

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Abstract

It is well reported that a profiled MOSFET biased in the subthreshold region of operation with the source diffusion floating and illuminated, operates as a photodetector with extended dynamic range[1]. However, this detector has a serious limitation in that transfer of the signal charge from the detector to the readout CCD is done through a MOSFET operating in the saturation region and thus is slow and incomplete. This limitation manifests itself as image lag from an illuminated integration period into a subsequent dark integration period. For many applications this is unacceptable.

A similar structure was proposed[2] that replaces the diffusion source with a virtual source formed by a MOS capacitor. The intent of the virtual source was to implement a structure from which all of the collected signal charge could be quickly and completely transferred into the readout CCD.

In this presentation the authors would like to present the design and operation of a profiled MOSFET with a virtual source, biased in the subthreshold region of operation. The method for feeding back a voltage signal, dependent on the amount of signal charge collected, to the MOSFET gate, implementing signal charge compression, is discussed. A simple circuit representation is simulated to show the extent of dynamic range and the results are compared to measurement.

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[1]"A Novel Wide Dynamic Range Silicon Photodetector and Linear Array", Chamberlain and Lee, *IEEE Trans. ED*, ED-31, 1984

[2]"Acousto-Optic Detector Considerations", Washkurak et al. *IEEE CCD Workshop*, June 1991

WIDE DYNAMIC RANGE DETECTORS

DESIGN GOALS

- Integrate at Low Light Levels

(0-30dB)[1]

- Compress at High Light Levels

(30-60dB)

- Minimize Image Lag
- Maximize Low End Sensitivity
- Obtain Functionality at Short Integration Times (1μs)

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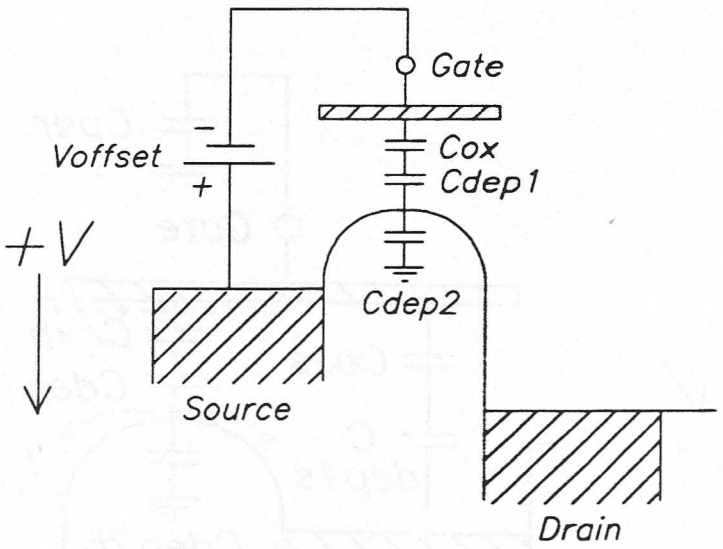
[1]dB refers to the ratio of maximum detectable to minimum detectable light intensity:

$$DR = 10 \log \left[\frac{H_{MAX}}{H_{MIN}} \right]$$

BURIED CHANNEL
VARIABLE BARRIER COMPRESSION

- The Source Potential Directly Sets the Base of the Barrier
- The Gate Potential Indirectly Sets the Peak of the Barrier Through the Series Capacitor Divider Network



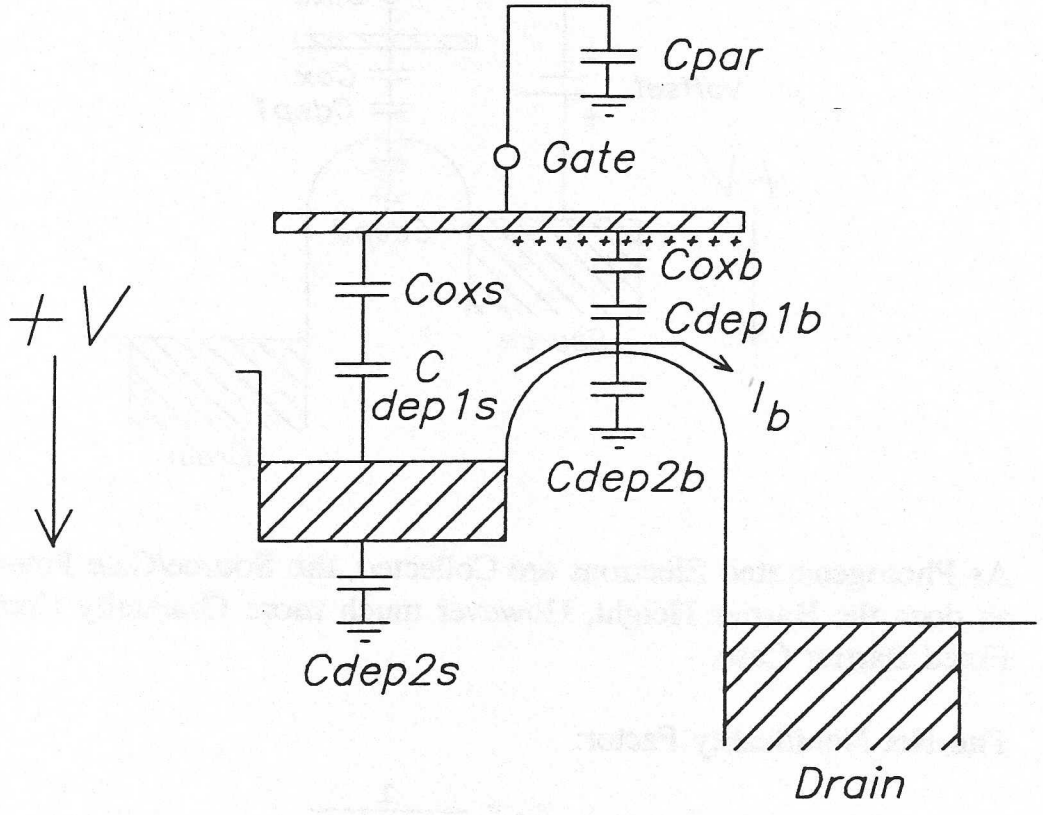
- As Photogenerated Electrons are Collected, the Source/Gate Potential Reduces as does the Barrier Height, However much more Gradually Compared to the Fixed Barrier Case.
- The Net Nonideality Factor:

$$\eta_S = \frac{1}{\frac{1}{\eta_{BH}} - \frac{1}{\eta_G}}$$

- Resulting η_S is 8.36. This Corresponds to 501mV/Decade

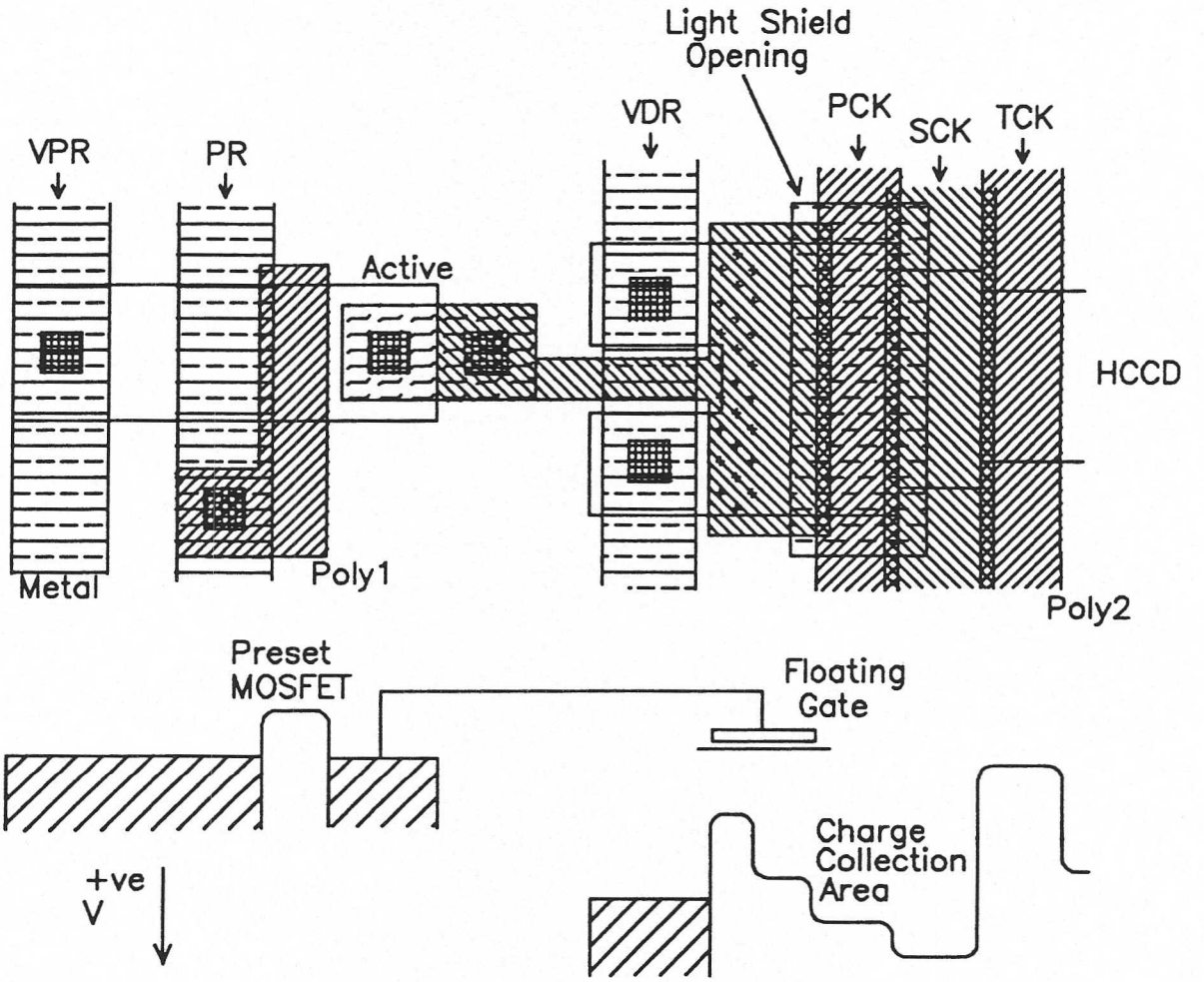
NEW FLOATING GATE STRUCTURE

- Structure uses a Polygate Collection Well for Image Lag Free Operation
- Structure uses a Charged Capacitor to Establish the Required Source/Gate Bias
- Structure uses a Buried Channel Barrier for Interface State Trap Free Operation



- As Collection Well fill up with Photogenerated Electrons, the Gate Potential is Pushed Up by the Series Combination of C_{oxs} and C_{dep1s}. C_{par} loads the Gate Electrode, therefore, it Should be Minimized

IMPLEMENTATION OF FLOATING GATE STRUCTURE



- The Floating Gate is Preset with the PR/VPR MOSFET Structure. Two Additional Gates PCK (Partition Clock) and TCK (Transfer Clock) are used to Enhance the Charge Collection Area.