

CMOS APS with autoscaling and customized wide dynamic range

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Abstract

A 64x64 element CMOS active pixel sensor (APS) with autoscaling and customized wide dynamic-range linear output is reported. The chip features a new architecture enabling multiple non destructive readouts per pixel per frame. When utilizing these multiple readouts real time feedback, each pixel in the field of view can automatically set an independent exposure time, according to its illumination, enabling a customized, large increase in the dynamic range.

In recent CMOS and CMD solutions it has already been shown that we could achieve an ultra high wide dynamic range using two outputs per frame [1, 2]. However, this will work well if the illumination levels are suited to one of the two integration times. If the illumination ranges somewhere in between we will not get an accurate reading. Several outputs could be read for different integration times. Still, an additional frame memory for each extra reading is required, and also some synchronization process needs to be done since the readings will be set apart in their starting point.

The architecture of the new approach is shown in Fig. 1. Every row is read through the regular output chain, at the lower part, and in addition is compared with an appropriate threshold, at certain time points. If a pixel value exceeds the threshold, a conditional reset is given at that time point for that pixel. The binary information concerning having the reset applied or not is saved in digital storage so that the exact illumination level could be scaled appropriately. This way the pixel value could be described as a floating point representation, where the exponent will describe the scaling factor for the actual integration time and the mantissa will be the regular A/D output, ie $VALUE = MAN * (T/X^{EXP})$, where VALUE is the pixel value which consists of the MAN (Mantissa, the analog or digitized output value), multiplied by the actual integration time, which is a function of the full integration time, T. The full integration time is divided by a constant X, for example 2, to the power of EXP. EXP is the exponent value, describing the scaling factor, ie which part of the integration time is actually effective. This value is read out at the upper part.

In the proposed solution, the additional hardware required will be placed in the periphery, and the information could be output with minimal effect on spatial and temporal resolution. The spatial resolution would be slightly modified since the desired ability to independently reset each pixel requires an additional transistor per pixel [3]. Concerning the temporal resolution - for a certain pixel we should check at different time points to get the exponential (scaling) term. Equivalently, we could look at the pixels of different rows to get the same information. We could look at row n at time=0 to get the mantissa (i.e. the regular A/D output) for row n, while we could look at the pixels in row n-N/2 (where N is the total number of rows that set the frame time) to get the first exponent bit (W1) for that row. We could also look at row n-N/4 to get the second bit (W2) for that row, at n-N/8 to get the third bit, etc. Thus, at the cost of a customized number of comparisons, we could automatically get the required information, and scale the mantissa accordingly.

Fig. 2 describes the proposed approach via a combined time-space diagram, where the axes represent the row and time, respectively. W1, W2, etc, represent the exponent bits, i.e. W1 represents the point of decision, T-T/2, whether to reset or not for the first time, W2 for the next point and so forth. The equivalent is shown at point n-N/2 in the spatial domain, i.e. that row should be used for the decision concerning W1, the first point as described above in the time domain.

Fig. 3 shows the autoscaling CMOS APS 64x64 test chip, which was designed using the HP 0.5 μ m n-well process available through MOSIS, the specifications and expected performance .

References

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2. Nakamura T. and Saitoh K., "Recent progress of CMD imaging", Proc. of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Bruges, Belgium, June 5-7, 1997.
3. O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, E. Fossum, "CMOS active pixel sensor star tracker with regional electronic shutter", IEEE J. Solid State Circuits, Vol. 32, No. 2, pp. 285-288, February 1997.

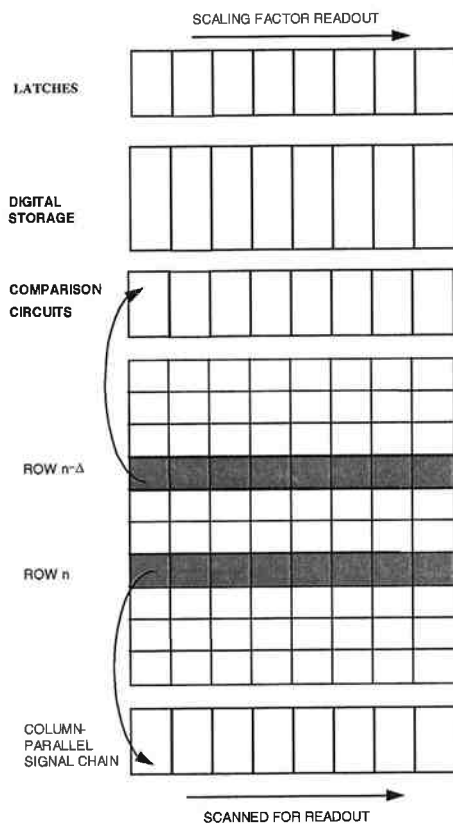


Fig. 1: Autoscaling CMOS APS architecture.

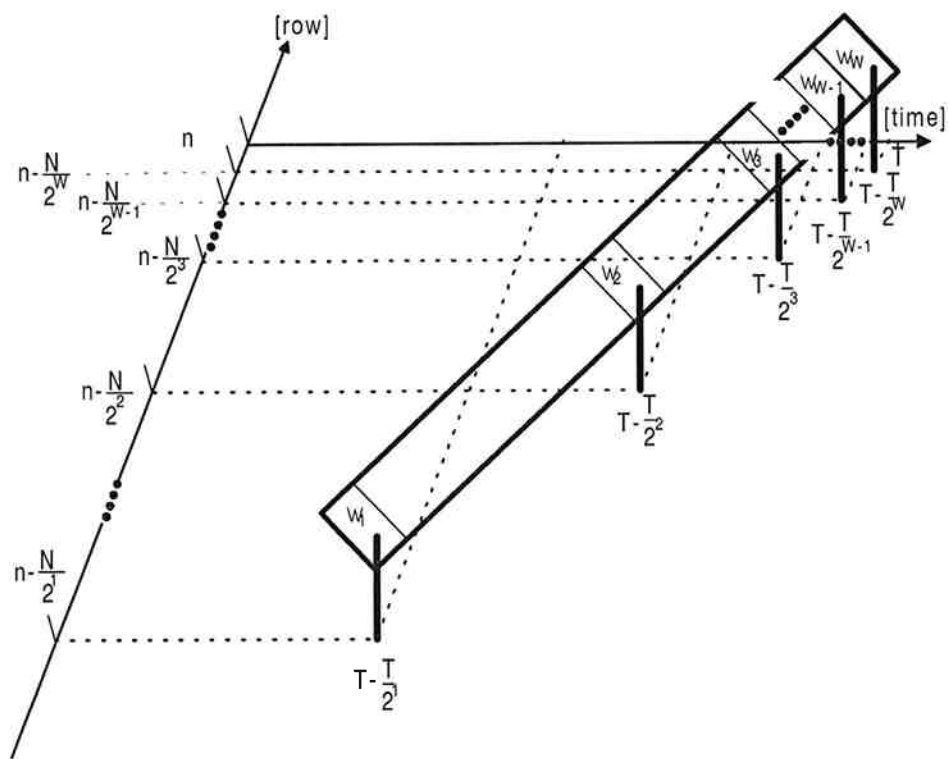
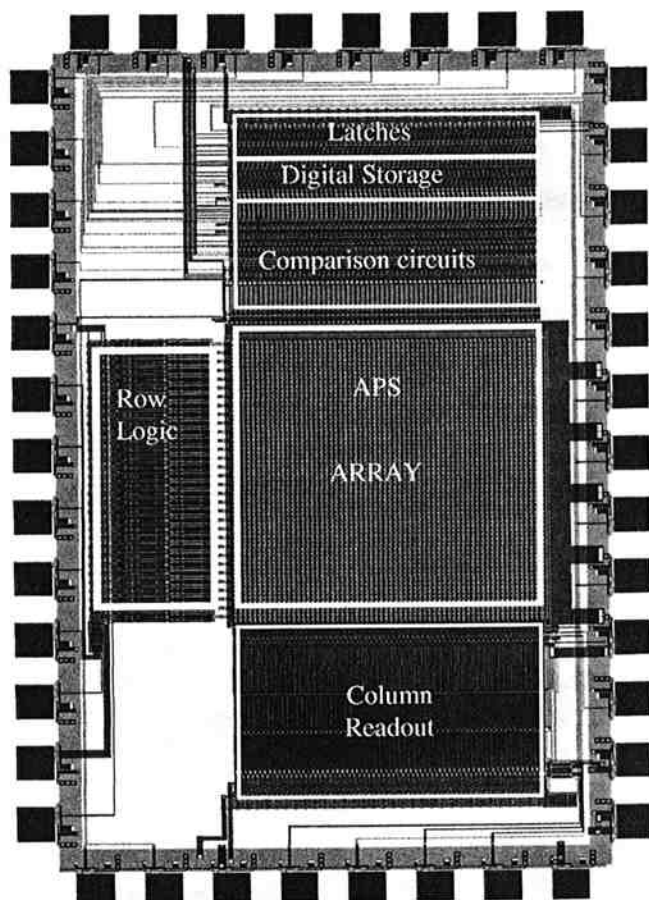


Fig. 2: The new approach description via a combined time-space diagram.

Autoscaling CMOS APS – test chip



Chip specifications and expected performance:

64x64	Array size
14.4um	Pixel size
0.5um HP nwell	Process
37%	Fill factor
2	Number of extended bits

Fig. 3: Test chip layout, specifications and expected performance.