2007 INTERNATIONAL IMAGE SENSOR WORKSHOP

June 7-10, 2007
The Cliff House Resort & Spa
Ogunquit, Maine USA

Organized by:

ImageSensors Inc.
www.imagesensors.org

Technical Co-Sponsors:

IEEE Electron Devices Society
Institute of Television Engineers of Japan (ITEJ)
Jet Propulsion Laboratory
Siimpel Corporation
Walter Kosonocky Award

Welcome to the 2007 International Image Sensor Workshop

It is a pleasure to extend a hearty welcome to all of you to the 2007 International Image Sensor Workshop at The Cliff House Resort & Spa in Ogunquit, Maine USA. As you have noticed the workshop (formerly titled IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors) has a new name – International Image Sensor Workshop. It is organized by ImageSensors Inc., a non-profit Public-benefit organization.

It is 21 years since the first workshop took place in 1986 at Columbia University's Arden House in Harriman, New York. Much has changed in these 21 years. Electronic imaging has undergone an explosive growth. The workshop (held every other year) has firmly established itself as the key forum on image sensor technology – discussing recent research results on a wide variety of image sensors, providing in-depth discussion and insight on technical issues of common concern, and stimulating thinking about new research directions and activities. The 2007 workshop – 11th in the series – continues in the same tradition, but with a new name. Considering the world-wide popularity and stature of this forum, and the breadth of image sensor related topics covered in the workshop, the International Image Sensor Workshop is certainly a more appropriate name for this forum.

For the statistically minded, we had a record number of abstracts submitted to the 2007 workshop – 110 in total. It will also have a record number of papers presented - 88 in all, consisting of 32 regular papers, 38 poster papers, 12 short papers, and 6 discussion/tutorial papers. 32 of these papers are from the continent of Asia, 26 from North America, and 30 from Europe, including a number of papers that consist of authors from multiple continents.

We have a diverse and exciting program. We have added an extra day to the 2007 workshop to permit longer discussions and more informal meeting time. In addition, we have introduced a new category of papers called discussion/educational papers. The purpose of these presentations is to stimulate discussion in areas of emerging technologies and/or in areas of common interest that are just outside the normal scope of the workshop. To further facilitate discussion, we have devoted 10 minutes for Q&A after each regular paper. There is also a period devoted entirely for poster viewing and discussion with the authors. We hope that active interaction and exchange of information among the participants will only make the workshop even more exciting.

The workshop will feature the 5th Walter Kosonocky Award that was established in memory of a great contributor to the field, who passed away on November 2, 1996.

As in previous years, we have tried to limit attendance to less than 150 people, based on the desire of the organizing committee to keep the workshop small and more personal. Although previous workshops have always sold out, what happened this year was quite unprecedented. Registration got filled up within just a couple of days of opening the pre-registration. Due to this overwhelming demand, we could not offer seats to a number of people who had sent in their

requests. We sincerely apologize to those who could not attend, and hope to see you at next workshop in 2009.

We would like to acknowledge our technical co-sponsors: IEEE Electron Devices Society, Institute of Television Engineers of Japan, Jet Propulsion Laboratory, Siimpel Corporation, and the Walter Kosnocky Award. We are extremely grateful to the Jet Propulsion Laboratory for its financial support in organizing the workshop.

This workshop could not have been organized without contribution from a number of people. I would like to thank Dr. Eric Fossum, Dr. Nobukazu Teranishi, and Dr. Albert Theuwissen of Organizing Committee for their support and guidance in planning the workshop. I would also like to thank all members of the technical program committee for soliciting papers, for ranking them, and for serving as session chairs, and especially Dr. Alex Krymski, the technical program committee chairman, for assisting me with the difficult job of selecting the papers, and putting the together an outstanding program. I am grateful to Ms. Angela McNamee of Siimpel Corporation for her time and enthusiastic support, as well as to my colleagues at the Jet Propulsion Laboratory for their efforts in making this workshop a success. Finally, I would like to express my sincere gratitude to Dr. Eric Fossum - not only for taking care of the local arrangements, and but for supporting and advising me through every detail of the workshop planning and organization.

Best wishes for a great and memorable workshop.

Bedabrata Pain
General Chairman

2007 International Image Sensor Workshop

organized by ImageSensors Inc.

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Nobukazu Teranishi (Matsushita, Japan)
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Angela McNamee (Siimpel, USA)

2007 INTERNATIONAL IMAGE SENSOR WORKSHOP

Ogunquit, ME
June 6-10, 2007

PROGRAM

June 6 (Wed)

18:00-20:00 **Early Registration**

June 7 (Thu)

9:00-10:00 **Registration**

10:00-10:15 **Opening Remarks**
Eric Fossum – Remarks on behalf of the Organizing Committee
Bedabrata Pain – Chairman's remarks

Session 01 **Discussion Session – I**
Session chair: Alex Krymski

10:20-11:00 Image Sensors and Image Quality in Mobile Phones — 1
Juha Alakarhu (Nokia, Tampere, Finland)

Session 02 **Image Sensors with Super-Small Pixels – I**
Session Chair: Johannes Solhusvik

11:00-12:10 A 3 Mega-Pixel Back-illuminated Image Sensor in 1T5 Architecture with 1.45 µm Pixel Pitch — 5
Jens Prima[1], Francois Roy[1], Perceval Coudrain[1], Xavier Gagnard[1], Josep Segura[1], Yvon Cazaux[1], Didier Herault[1], Nicolas Virollet[1], Norbert Moussy[2], Benoit Giffard[2], Pierre Gidon[2] ([1]FTM Imaging, STMicroelectronics, Crolles, France; [2]CEA Léti-MINATEC, Grenoble, France)

11:20-11:40 A 1.75µm Square Pixel IT-CCD using Gate Oxide Insulator Composed by a Single Layer Electrode Structure — 9
Junji Yamane, Yoshiaki Kitano, Keita Suzuki, Keita Hondo, and Nobuhiro Karasawa (Semiconductor Business Group, Sony Corporation; *Sony Semiconductor Kyusyu Corporation, Japan)*

11:40-12:00 Optoelectronic Investigation for High Performance 1.4 µm pixel CMOS Image Sensors — 13
Seong-Ho Cho, Gibum Kim, Hyunpil Noh, Chang-Rok Moon, Kangbok Lee, Kwangok Koh, and Duckhyung Lee (Samsung Electronics Ltd, Yongin-city, Korea)

12:00-12:06 Active Pixel Sensor Arrays in 90/65 nm CMOS-Technologies with Vertically Stacked Photodiodes 16
S. Henker, C. Mayr, J-U. Shlussler, R. Schuffny, U. Ramacher, and A. Heitmann (University of Dresden, Institute of Circuits and Systems, Dresden, Germany)

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R.C. Gutierrez, T.K. Tang and E.R. Fossum (Siimpel Corp, Pasadena, USA)

Session 04 **High Dynamic Range Image Sensors**
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Koichi Mizobuchi[1], Satoru Adachi[1], Tomokazu Yamashita[1], Seiichiro Okamura[1], Hiromichi Oshikubo[1], Nana Akahane[2] and Shigetoshi Sugawa[2] ([1]DISP Development, Texas Instruments Japan, Inashiki, Japan, [2]Gradute School of Engineering, Tohoku University, Sendai, Japan)

14:45-15:05 A 121.8dB Dynamic Range CMOS Image Sensor using Pixel-Variation-Free Midpoint Potential Drive and Overlapping Multiple Exposures 30
Yusuke Oike, Atsushi Toda, Tadayuki Taura, Akihiko Kato, Hiroki Sato, Masanori Kasai, and Tadakuni Narabu (Sony Corporation, Atsugi, Japan)

15:05-15:25 A High Dynamic Range Digital Linlog CMOS Image Sensor Architecture Based on Event Readout of Pixels and Suitable for Low Voltage Operation 34
Alexandre Guilvard[1,2], Pierre Magnan[1],Josep Segura[2], Philippe Martin-Gonthier[1] ([1]Supaero, Toulouse, France; [2]STMicroelectronics, Crolles, France)

15:25-15:45 **Coffee Break**

Session 05 **Discussion Session – III**
Session Chair: Nobukazu Teranishi

15:45-16:25 Performance of Solid-state Image Sensors in Medical X-Ray Applications 38
Inge M. Peters (Dalsa Professional Imaging, Eindhoven, The Netherlands)

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([1]Gigle Semiconductor, Edinburgh, UK; [2]University of Oxford, Oxford, UK; [3]University of Edinburgh, Edinburgh, UK; [4]STMicroelectronics Imaging Division, Edinburgh, UK)

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19:00-21:00 **Dinner**

June 9 (Sat)

Session 12 **Noise/Dark Current in Image Sensors**

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Centre for Scientific and Technological Research, Trento, Italy)

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11:35-11:40 **Closing Remarks**

Image Sensors and Image Quality in Mobile Phones

Juha Alakarhu
Nokia, Technology Platforms, Camera Entity, P.O. Box 1000, FI-33721 Tampere
juha.alakarhu@nokia.com (+358 50 4860226)

Abstract

This paper considers image sensors and image quality in camera phones. A method to estimate the image quality and performance of an image sensor using its key parameters is presented. Subjective image quality and mapping camera technical parameters to its subjective image quality are discussed. The developed performance metrics are used to optimize sensor performance for best possible image quality in camera phones. Finally, the future technology and technology trends are discussed. The main development trend for images sensors is gradually changing from pixel size reduction to performance improvement within the same pixel size. About 30% performance improvement is observed between generations if the pixel size is kept the same. Image sensor is also the key component to offer new features to the user in the future.

1. Introduction

Camera phones offer great benefits to the users by enabling photography, video recording, and content sharing always and everywhere. Besides the camera, modern mobile phones offer an extensive set of features, which require relatively large number of components. This sets tough limits for the size and cost of an individual component. Size and cost are also one of the main challenges in cameras in mobile phones. On the other hand, the very high volumes enable, e.g., using advanced silicon process technology.

There is a wide range of camera phone products (more or less camera driven), and a wide variety of possible camera technologies. Careful product planning and managing technologies are required to map the right technologies and cameras to right products. This paper considers image sensor performance metrics, subjective image quality and sensor optimization. Finally the sensor performance trends and future sensors are discussed.

Image sensor is the key component to enable high image quality even in the challenging mobile phone environment. The performance of image sensors has improved enormously during the past few years. There are promising new technologies to enable similar development also in the future.

2. Performance metric

A reliable sensor performance metric is needed in order to have meaningful discussion on different sensor options, future sensor performance, and effects of different technologies. Comparison of individual technical parameters does not provide general view to the image quality and can be misleading. A more comprehensive performance metric based on low level technical parameters is developed as follows.

First, conversion from photometric units to radiometric units is needed. Irradiation E [W/m^2] is calculated as follows using illuminance E_v [lux], energy spectrum of the illuminant (any unit), and the standard luminosity function V.

Equation 1: Radiometric unit conversion

$$E = \frac{\int s(\lambda)d\lambda}{683\frac{lm}{W}\int s(\lambda)V(\lambda)d\lambda} E_v$$

The number of photons hitting the target can be calculated by multiplying illuminant spectrum per unit wavelength by the irradiance E and diving this by photon energy.

Equation 2: Number of photons.

$$N_{ph}(\lambda) = \frac{\frac{s(\lambda)}{\int s(\lambda)d\lambda}E}{\frac{hc}{\lambda}}$$

The number of electrons generated in each pixel is calculated using lens transmission T, F-number F, target reflectance R, pixel size p, IR cut filter transmittance C, integration time t, full well capacity W, and quantum efficiency Q for each channel c.

Equation 3: Number of signal electrons.

$$S(c) = \min\left(\frac{RT}{4F^2} p^2 t \int N_{ph}(\lambda)C(\lambda)Q(\lambda,c)d\lambda, W\right)$$

The required analog gain is estimated using the green channel signal S(g), exposure target e and maximum analog gain G_m.

Equation 4: Analog gain.

$$G = \max\left(1, \min\left(G_m, \frac{e}{S(g)}\right)\right)$$

Finally, the noises are calculated for each channel using well-know formulas, where r is the readout noise [e], d is the average dark current generation at temperature T [e/s], P is the photo-response non-uniformity relative to the signal, and B is the number of ADC bit.

Equation 5: Main noise sources.

$$n_{ph}(c) = \sqrt{S(c)}$$
$$n_r(c) = r$$
$$n_d(c) = \sqrt{dt}$$
$$n_{prnu}(c) = PS(c)$$
$$n_{ADC}(c) = \frac{W}{2^B G\sqrt{12}}$$

The total noise level for each channel n(c) can be estimated by taking root of squares of each component. The sensor raw signal to noise ratio can be calculated using the presented formulas, but the raw SNR tells little about the achievable image quality of the sensor.

SNR after color matrix correlates better with the resulting image quality, i.e., the required color transform is part of the sensor performance. The color matrix can be derived using the sensor spectral response, e.g., [9].

Simple white balance is applied before the color matrix.

Equation 6: White balancing.

$$S_{WB}(c) = \max(S(c))$$
$$n_{WB}(c) = \frac{\max(S(c))}{S(c)} n(c)$$

The effect of color matrix is calculated as follows. This is only shown for red channel here.

Equation 7: Applying color matrix.

$$S_{CCM}(r) = S_{WB}(r)C_{rr} + S_{WB}(g)C_{rg} + S_{WB}(b)C_{rb}$$
$$n_{ccm}(r) = \sqrt{(S_{WB}(r)C_{rr})^2 + (S_{WB}(g)C_{rg})^2 + (S_{WB}(b)C_{rb})^2}$$

To understand which camera is better in a given condition, the separate channel SNRs are combined single overall SNR. A simple way to do this is to use the luminance coefficients L_r=0.299, L_g=0.587 L_b=0.114 and calculate the combined SNR as follows.

Equation 8: Combined SNR.

$$S = L_r S_{CCM}(r) + L_g S_{CCM}(g) + L_b S_{CCM}(b)$$
$$n = \sqrt{(L_r n_{CCM}(r))^2 + (L_g n_{CCM}(g))^2 + (L_b n_{CCM}(b))^2}$$

The illuminance where a given target SNR is reached is used as a one-number performance metric. SNR=10 commonly used as target SNR. The advantage of using such x value is that comparison of illumination is easier than comparison of SNRs.

The actual SNR in the final output image is obviously different from the calculated SNR, because the calculation does not include several steps of the image processing. This is not a problem since the metric is only used to compare the sensor performances.

There are many open issues in the performance metric and also several simplifications were made when it was derived. The areas for future work are as follows.

- All noise sources are not included. This causes inaccuracy especially in low light.
- All noise sources do not have such statistics that the resulting sum noise could be calculated using the simple formula presented in this paper. Especially dark current hot pixels and line noises cannot be included [1].
- Combining the SNRs as presented here is not exactly correct because the noise components after color matrix are correlated. Furthermore, the Bayer arrangement of the pixels is not taken into account.
- Relative illumination is not taken into account. A possibility include this would be to integrate QE over the whole image area.
- The achievable color accuracy is not taken into account; only the noise effect of the color matrix.
- The noise floor as a function of gain can have more complicated relationship than the simple quantization noise model used here.
- Sensors tend to have many problems that are not included in the metric, such as green imbalance and color shading.

Even with the given limitations, the presented method has been successfully used. Furthermore, when more accurate methods are developed, the accuracy of the input parameters also needs to be improved.

3. Subjective image quality

The ultimate quality measure of a camera is the overall user experience, which includes subjective image quality and usability.

In Nokia, subjective image quality is measured by capturing test images in standard conditions and asking a group of test people to grade the image quality. This way, mean opinion score (MOS) can be calculated for each camera in each condition.

When a future camera is specified, its target performance should include target mean opinion scores. To enable specifying and planning target mean opinion scores, a method to map the technical parameters to mean opinion score is needed. This mapping is extremely challenging since there are many components: flash, optics, image sensor, image

processing. The subjective image quality depends on the quality of each component and how well they operate together.

Figure 1 represents a simple heuristic model for camera head mean opinion score estimation. The x-axis shows a sensor performance metric, such as the one developed in this paper, and the y-axis shows the estimated MOS. The curves link the sensor performance to the MOS for different resolutions of the camera system, including optics, sensor and processing.

The model has been derived based on measured mean opinion scores for various cameras. When the sensor output is noisy, MOS is mainly limited by the sensor performance, i.e., the camera system resolution and contrast do not significantly affect the results. On the other hand, when the sensor outputs clean noise-free image, MOS is mainly limited by the optics performance. This simple model assumes that the image processing platform is kept unchanged, so it needs to be separately tuned for different image processing platforms. Different color temperatures may also need separate tuning.

The main challenges and areas for the future development are as follows.

- Development of the fair sensor performance metric. The challenges listed in the previous section are also valid here. Optics performance estimation also needs similar approach; this is outside the scope of this paper.
- Including the image processing. Formal way of mapping image processing methods to subjective image quality is extremely challenging and may not be possible. Heuristic approach may be always needed.
- Accurate method for mapping the sensor resolution to the x-axis of the model. If the optics resolution and pixel-level SNR is kept unchanged but the resolution of the sensor is changed, how should it be mapped to the model? Image processing complicates calculating the resulting effective SNR.

Even tough there are still open items in the model, the key claim is that there must be link between the technology selections and the final product image quality. The camera development is like running blind, if there are no performance targets, no method to estimate the subjective image quality, or no means to map the technical parameters to the subjective image quality. Comparison of the early performance predictions to the final product performance is also very important channel for feedback and continuous improvement.

4. Image quality optimization

The low light performance is usually mentioned first, when image quality issues are discussed. Still, more important question than whether there is anything visible in 1 lux image is *what exposure is needed to capture the first acceptable image*.

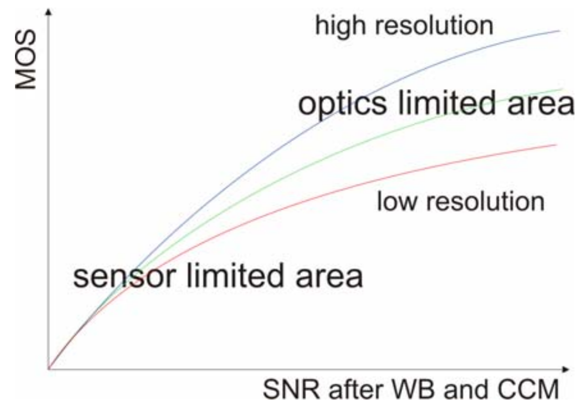

Figure 1: MOS estimation model.

SNR=10 after white balance and color matrix has proven to be a good approximate criteria for first acceptable image in subjective image quality tests. Similar conclusion has been done in ISO standard even though the SNR calculation method is different [3]. More accurate value is not needed, because “first acceptable” is very subjective item and depends also on other camera system parameters.

Optimizing a sensor for the first acceptable image is challenging. In conditions that yield SNR=10, the most dominant noise source is usually photon shot noise, when typical camera phone lens and exposure times are used. Therefore, the SNR can be significantly improved only by increasing quantum efficiency and reducing crosstalk (crosstalk is reduced to enable smaller CCM coefficients).

Readout noise and dark current are usually so low that further reduction of them would not significantly change the situation, e.g., [7]. Full well capacity does not either affect image quality in SNR=10 conditions. It is also interesting to notice that in most cases crosstalk has much more contribution to the maximum effective SNR than full well capacity or photo response non-uniformity.

An example of a 1.75u pixel optimization is shown in Figure 2. It shows the illumination level to reach SNR=10 for different 1.75u pixel optimizations: standard, 30% reduction of the readout noise, 10% increase of sensitivity (QE), and -0.1 smaller diagonal elements (and +0.05 +0.05 larger off-diagonal elements).

The most important parameters in addition to the basic SNR performance are angular response, line noise characteristics, dynamic range, and color accuracy. Especially angular response – shading and crosstalk performance – need special attention in mobile phones due to the low height camera module optics and resulting high chief ray angles in thin phones.

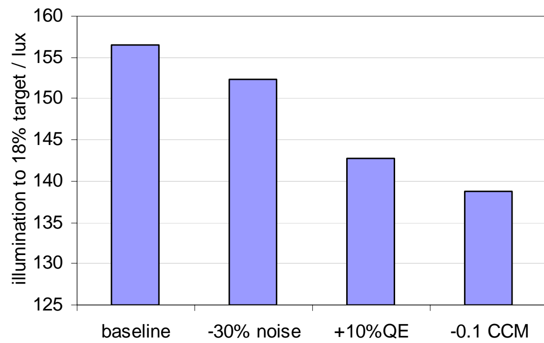

Figure 2: Illumination to reach SNR=10 after WB and CCM for different optimizations of a 1.75u pixel. Calculations use 3200K illuminant, F=2.8/Tr=0.8 lens, and 18% target reflectance.

5. Technology trends

As the contemporary pixel sizes enable large resolutions even in small camera modules, there are two options for the new sensor generations: 1. continue the pixel size reduction, or 2. performance optimization using the same pixel size. The performance comparison of larger and smaller pixel in the same optical format is not straightforward because the larger resolution makes noise less disturbing or enables more downscaling which increases SNR.

Based on historical data, if the pixel size is kept the same, *a new generation technology improves the SNR=10 metric about 30%.* There are already products on the market showing this: the sensor in Nokia N95 is about 30% better than the sensor in Nokia N80, based on the SNR=10 metric. Both products use the same pixel size, but N95 uses a newer pixel generation.

It will be very interesting to see how long the same performance improvement trend can be kept. There is a lot of room since the ideal sensor would have 100% QE and perfect colors with unity color matrix. When traditional technology is used, improving the optical path is very important for QE and angular response [7]. When the limits of the traditional approach are reached, promising new technologies, such as back-side illumination [4] (new in consumer applications), and organic film materials [6] can enable keeping the average trend longer time. Multiplying electrons, enabling effectively zero noise floor or photon-counter approach could be also one potential solution [5].

A very important trend in cameras is also offering new features to the user. Especially high dynamic range [1] and high frame rate technologies [8] are very promising. Still image stabilization would be also a wonderful feature. If backside illumination becomes practical, it will enable more digital processing integrated in to the sensor so that a lot of new digital features become possible for small pixels.

6. Conclusions

Sensor performance has been discussed using a proposed sensor performance metric. QE and crosstalk are currently the most important sensor parameters. A 30% yearly improvement of the proposed SNR metric has been observed. Future shows also very promising technologies for improving them. Image sensor is also the key component to offer new camera features in the future.

References

[1] R. L. Baer, "A model for dark current characterization and simulation," in *Proc. SPIE, Vol. 6068, Sensors, Cameras, and Systems for Scientific / Industrial Applications VII*, Feb. 2006, pp. 37-48.

[2] Y. Egawa, H. Koike, R. Okamoto, H. Yamashita, N. Tanaka, J. Hosokawa, K. Arakawa, H. Ishida, H. Harakawa, T. Sakai, and H. Goto, "A 1/2.5 inch 5.2Mpixel, 96dB Dynamic Range CMOS Image Sensor with Fixed Pattern Noise Free, Double Exposure Time Read-Out Operation," in *Proc. 2nd IEEE Asian Solid-State Circuits Conference,* Nov. 2006.

[3] ISO 12232, Photography – Electronic still-picture cameras – Determination of ISO speed.

[4] B. Pain, T. Cunningham, S. Nikzad, M. Hoenk, T. Jones, B. Hancock, C. Wrigley, "A Back-illuminated Megapixel CMOS Image Sensor," in *Proc. IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, June 2005, pp. 35-38.

[5] M. Rabbins and B. Hadwen, "The Noise Performance of Electron Multiplying Charge-Coupled Devices," *IEEE Trans. On Electron Devices,* vol. 50, no. 5, May 2003.

[6] S. Takada, M. Ihama, M. Inuiya, "CMOS Image Sensor with Organic Photoconductive Layer Having Narrow Absorption Band and Proposal of Stack Type Solid-State Image Sensors," in *Proc. SPIE, Vol. 6068, Sensors, Cameras, and Systems for Scientific / Industrial Applications VII*, Feb. 2006, pp. 86-93.

[7] H. Takahashi, T. Noda, T. Matsuda, T. Watanabe, M. Shinohara, T. Endo, S. Takimoto, R. Mishima, S. Nishimura, K. Sakurai, H. Yuzurihara, S. Inoue, "A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders", in *Digest of Technical papers, 50th IEEE Int. Solid-State Circuits Conference,* Feb. 2007, pp. 510-511.

[8] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, "A 1/1.8-inch 6.4MPixel 60 frames/s CMOS Image Sensor with Seamless Mode Change*," IEEE Journal of Solid-State Circuits,* vol. 41, no. 12, pp. 2998-3006, Dec. 2006.

[9] X. Zhang and D. Brainard, "Bayesian Color Correction Method for Non-Colorimetric Digital Image Sensors," in Proc. 12th Color Imaging Conference: Color Science and Engineering Systems, Technologies, Applications, Nov. 2004, pp. 308-314.

A 3Mega-Pixel back-illuminated image sensor in 1T5 architecture with 1.45µm pixel pitch

Jens Prima[*,1], *Francois Roy*[1], *Perceval Coudrain*[1], *Xavier Gagnard*[1], *Josep Segura*[1], *Yvon Cazaux*[1], *Didier Herault*[1], *Nicolas Virollet*[1]
Norbert Moussy[2], *Benoit Giffard*[2], *Pierre Gidon*[2]
(1) FTM Imaging, STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France
(*) E-mail : jens.prima@st.com, Tel.: +33 4 76 92 51 46, Fax: +33 4 76 92 68 14
(2) CEA Léti-MINATEC, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

Abstract:
A 3Mega-Pixel back illuminated image sensor in 1T5 architecture and 1.45µm pixel pitch has been successfully developed and characterized. A high quantum efficiency over 60% in the visible light spectrum and a low dark current of 1e$^-$/s at 25°C have been achieved due to dedicated frontside and backside process steps such as antireflective layer adaptation, p$^+$ pinning layer and thermal treatment.

Introduction:
CMOS image sensors are gaining a high influence since several years. The main challenge consists in shrinking the pixels without decreasing the pixel performances, as the optical stack and the metal wiring over the surface reduced diode cause optical efficiency issues [1, 2]. The realization of a back-illuminated image sensor offers a fundamental solution, as the backend stack is located under the photodiode [1-3]. We demonstrate a 3 Mega-Pixel back-illuminated image sensor with a 1.45µm pixel pitch in 1T5 architecture, which has a mean dark current of 1e$^-$/s at 25°C and a quantum efficiency (QE) of over 60% in the visible light spectrum.

Pixel Design:
The backside illuminated 3MP image sensor with a 1.45µm pixel pitch has been realized in a 0.13µm front-end CMOS based process. The backend metallisation was processed in 90nm copper based design rules [4]. The principal pixel architecture is a pinned fully depleted noiseless photodiode with transfer gate and reset noise cancellation thanks to correlated double sampling (CDS). Several transistors are shared between neighbouring pixels, resulting in 1T5 pixel architecture [4]. A pixel schematic is shown in figure 1: each pixel has a diode and a transfer gate transistor (TG). In order to increase the fill factor, four pixels are regrouped to one sensing node, which is connected to a reset (RST) transistor and to a source follower (SF) transistor.

Process& Experiments:
The process is realized on silicon on insulator (SOI) starting material. Several SOI thicknesses have been evaluated in order to find an optimum between quantum efficiency and crosstalk.

Dedicated p$^+$ implants are implanted in the pixel area. A vertical p$^+$ implant isolates the pixels from each other, resulting in a lower crosstalk and higher quantum efficiency. Figure 2 shows a relative increase of 20% quantum efficiency with the introduction of the specific p$^+$ implant. In a standard CMOS imager the diode surface potential is pinned to 0V and the photogenerated holes are evacuated by the substrate. On the SOI substrate the diode surface pinning and the hole-evacuation is provided by an additional contact on a p$^+$ implant. The backend consists in 3 metal layers. As the chips are illuminated from the backside, metal lines are allowed to cross directly above the diode area [3]. Furthermore the dielectric backend stack does not have to be optically optimized in terms of total thickness and material composition. After the final metal layer, a passivation layer and subsequent wafer bonding layer (WBL) are deposited. The WBL is planarized and a support wafer is bonded to the processed wafer. Afterwards the processed wafer is back-grinded. The backside surface is covered by an antireflective coating in order to avoid light losses by reflections. Figure 3 shows the simulated transparency with and without antireflective layer. The pads are reopened through the active silicon layer and finally deposited and patterned aluminium in the pads provides a standard surface for test and package purposes. In the next development steps color filters will be realized on the sensor, which is monochrome without micro-lens for the time being. The process flow is summarized in figure 4.

Pixel performances:
The conversion gain of the image sensor is 66µV/e$^-$. The quantum efficiency (QE) has been evaluated as a function of the SOI thickness. Figure 5 shows that a QE gain for wavelength >460nm can be observed for a thick SOI layer, as too thin silicon layers cannot absorb the entire light quantity of longer wavelength according to the absorption law. The Modulation Transfer Function (MTF) for different wavelengths is presented in figure 6. A decrease of the MTF, which is equivalent to an increased crosstalk, can be observed for shorter wavelengths. As the blue light is absorbed near the surface, the photogenerated electrons have to cover a longer distance in order to reach the diode and thus have a higher possibility to

diffuse into the neighbouring pixels, which increases the crosstalk. A decreased crosstalk, which corresponds to a higher MTF, can be reached by a lower substrate thickness, as shown in figure 7. In comparison to figure 5 we can conclude, that a compromise for the substrate thickness has to be made up in terms of pixel crosstalk on the one hand and QE on the other hand. Thicker substrates increase the QE, whereas the crosstalk increases, too.

The full well diode saturation charge is reached at $4000e^-$. An improvement of the saturation could be obtained by diode doping profile optimization. The dark current is $1e^-/s$ at 25°C. Figure 8 shows the dark current as a function of temperature. The low dark current has been achieved thanks to dedicated frontside and backside process steps such as p^+ pinning layer and thermal treatment. Due to a very good charge transfer, the lag is below the measurement threshold. The temporal noise measured in darkness is $5e^-$, the main contributor being the source follower transistor. The principal image sensor parameters are summarized in table 1.

Figure 9 shows a picture, taken by the 3MP back illuminated image sensor with 1.45µm pixel pitch in 1T5 architecture.

Conclusion:

We have demonstrated the feasibility of manufacturing CMOS image sensors with a very small pixel pitch (1.45µm x 1.45µm) in a back illuminated process. A high QE of 60% in the visible light spectrum has been reached. Other image sensor parameters like the conversion gain, the dark current, the lag and the temporal noise have not been deteriorated by the backside process and are comparable to state of the art standard frontside image sensors.

Ongoing work is related to the crosstalk reduction as well as color filter and micro-lens processing.

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References:

[1] B. Pain et al., "A Back-illuminated Megapixel CMOS Image Sensor", Proc. 2005 IEEE Workshop on CCD and Advanced Image Sensors, p. 35

[2] B. Pain, "Fabrication and Initial Results for a Back-illuminated Monolithic APS in a mixed SOI/ Bulk CMOS Technology", Proc. 2005 IEEE Workshop on CCD and Advanced Image Sensors, p. 102

[3] S. Iwabuchi et al., "A Back-Illuminated High Sensitivity Small-Pixel Color CMOS Image Sensor with Flexible Layout of Metal Wiring", p.302, ISSCC 2006

[4] M. Cohen et al., "Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensor", IEDM 2006

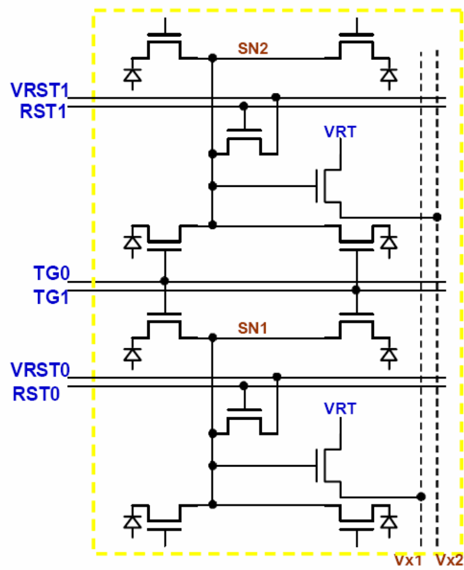


Fig. 1: 1T5 pixel schematic

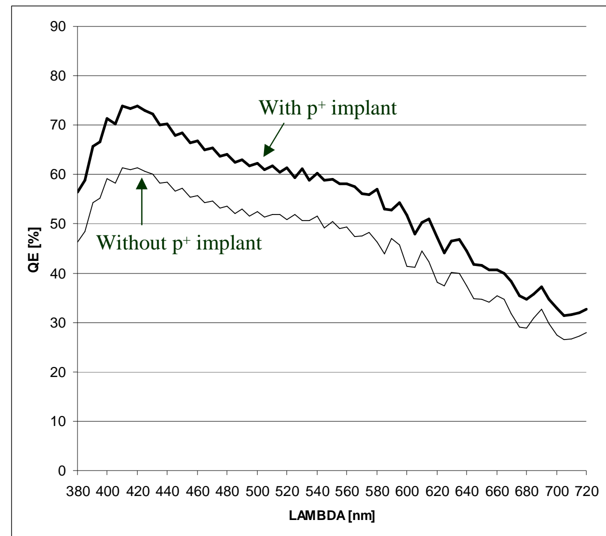


Fig. 2: Influence of p^+ implant on QE

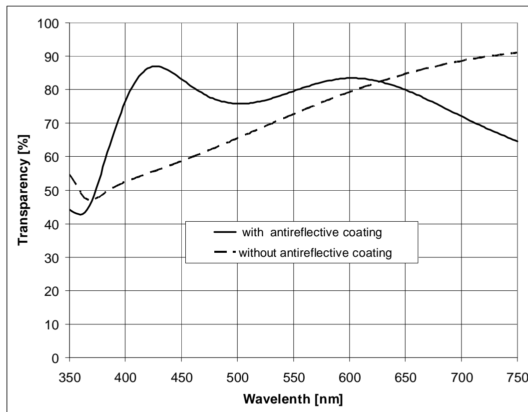


Fig. 3: Transparency with and without antireflective coating

- SOI wafer
- CMOS Imager Process
- Wafer Bonding Layer (WBL) Deposition and Preparation
- Wafer bonding and backside grinding
- Anti-reflective-coating (ARC)
- Pad opening
- (further development: Color Filters and Micro-Lens)

Fig. 4: Process flow

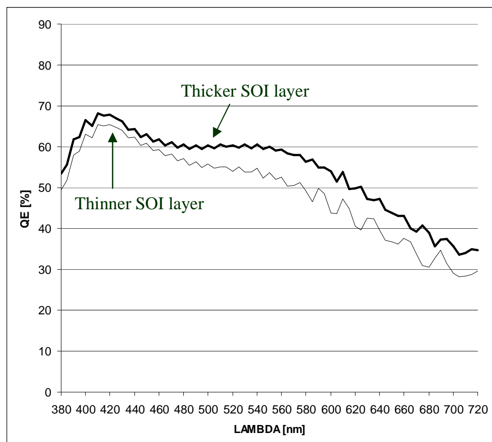


Fig. 5: Influence of SOI thickness on QE

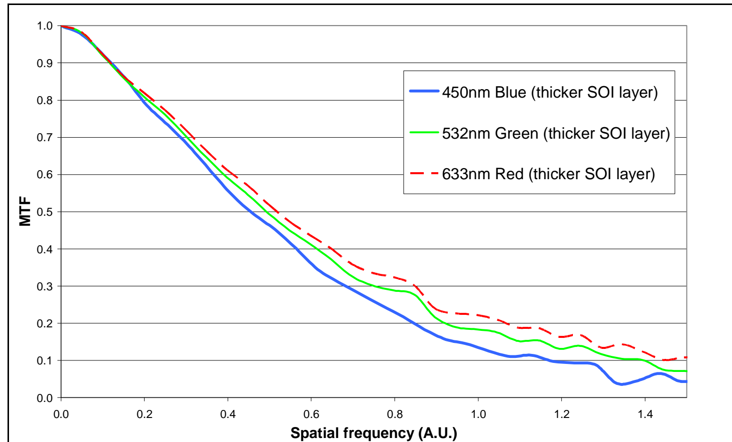


Fig. 6: MTF for thicker substrates at different wavelength

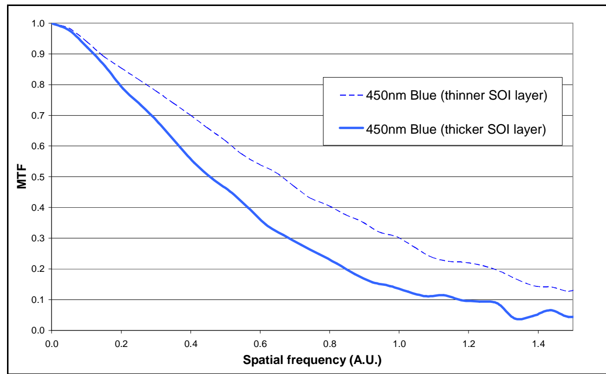


Fig. 7: Comparison of MTF at 450nm for thinner and thicker substrates

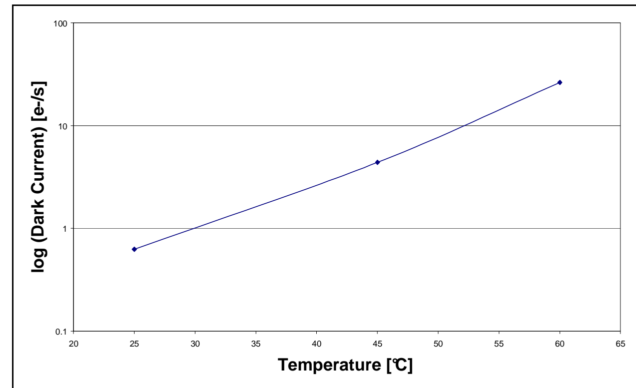


Fig. 8: Temperature dependence of dark current

	1.45µm back illuminated pixel	**Comment**
Saturation charge [e-]	4000	Full Well
Conversion Gain [µV/ e-]	66	
Lag [e-]	0	Charge transfer free of lag
Sensitivity[e-/ Lux s]	6800	3200K + IR cut-off at 650nm
Dark Current at 25°C [e-/s]	1	Mean Value
Temporal Noise [e-]	5	Main contributor: SF
Quantum Efficiency @ 550nm [%]	60	

Table 1: Summary of 1.45µm back illuminated pixel performances

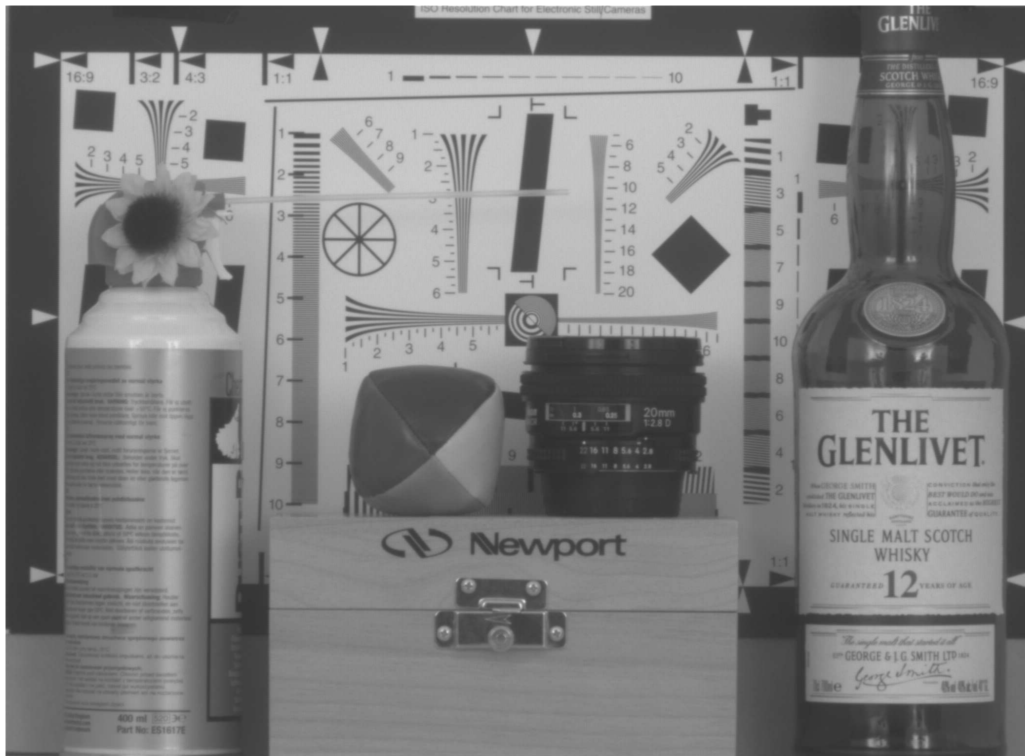


Fig. 9: Monochrome image from 3MP back illuminated array with 1.45µm pixel pitch

A 1.75-µm square pixel IT-CCD having a gate oxide insulator composed by a single-layer electrode structure

Yoshiaki Kitano, Junji Yamane, Keita Suzuki, *Keita Hondo, Nobuhiro Karasawa
Semiconductor Business Group, Sony Corporation
*Sony Semiconductor Kyusyu Corporation, Kumamoto Technology Center

Abstract

We have introduced a gate oxide insulator into a interline transfer CCD (IT-CCD) image sensor by using a single-layer electrode structure. We confirmed that the charge transfer function was not degraded in this structure when subjected to a high electric field, in contrast with conventional gate oxide-nitride-oxide (ONO) structures. We adapted this newly developed structure to a 1.75-µm square pixel IT-CCD image sensor with 8M pixels of 1/2.5-type image format and evaluated its device performance.

1. Introduction

IT-CCD image sensor is still the mainstream in compact digital still cameras (DSCs) since CCDs can produce high quality images even for very small pixel sizes. As Fig.1 shows, the pixel size of DSCs has been continuously reduced. The smallest pixel size of IT-CCD image sensors in the 2007 DSC market is 1.75-µm square.

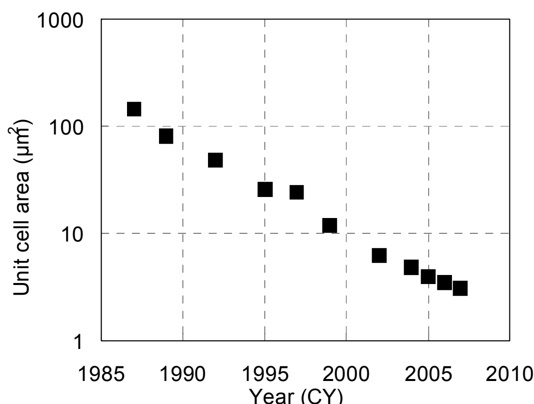


Fig.1 Miniaturization trend of IT-CCD pixel size in SONY.

In spite of a reduction in pixel areas of over 1/40 for the past two decades, the operation voltage of IT-CCD has only been reduced by at most 20%. This is because a high operation voltage is required to maintain a high image quality, in terms of a high saturation output and a high charge transfer efficiency, etc. Thus, the electric field employed in DSCs is increasing year by year. This is in contrast with the development of general semiconductor devices, which follow a scaling law. We find that, if the electric field in DSCs continues to increase at the current rate, degradation of the charge transfer function will soon become a problem for conventional IT-CCDs constructed with an ONO gate insulator.

We propose the use of gate oxide insulators in IT-CCDs for overcoming this problem.

2. Gate ONO insulator on IT-CCD

Over the past two decades, gate ONO structures have been used as insulators for IT-CCD image sensors having multilayer electrodes; one reason for their popularity is that they are convenient from a manufacturing point of view.

As Fig.2 shows, it is difficult to produce a oxide layer having uniform thickness beneath the 1st and 2nd poly-Si electrodes, because of the necessity of employing a second oxide insulator for a multilayer electrodes having a gate oxide structure. In the case of gate ONO insulator, by adding an oxidizing 1st electrode or an oxide

etching step, we can ensure a uniform thickness of the insulator, thereby reducing the ineffective gate voltage swing.

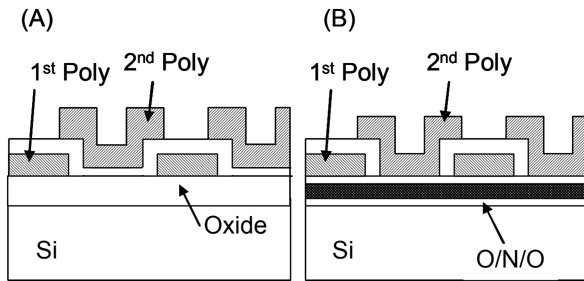


Fig. 2. Cross-sections of (A) gate oxide structure and (B) gate ONO structure and vertical resistor with multi-layer electrode.

However, we found out that such a gate ONO structure potentially can degrade the charge-transfer-efficiency (CTE) due to the high electric field used after charge readout from the photodiode to the vertical register.

Fig.3 shows the shift in the readout voltage as a function of the electric field in a conventional IT-CCD having an ONO gate insulator. This plot indicates that the readout voltage will continue to increase as the electric field is increased. This means that a high electric field will degrade the CTE as the sizes of IT-CCDs are reduced in the future.

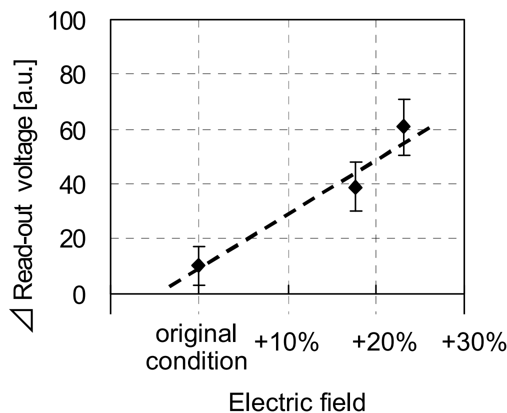


Fig.3 Electric field dependency of ⊿Read-out voltage. (CTE>0.995)

We developed a hypothesis to explain this phenomenon. Fig.4 shows a schematic diagram of the cross-section of a photodiode (PD) and vertical register together with the 1D potential profile of IT-CCD during the electron read out operation respectively. The gate electrode is positively biased so that accumulated electrons drift toward to the vertical register. At this point, few electrons accelerated by the high electric field can be injected and trapped in the silicon nitride (SiN) layer in the ONO insulator, and this can cause a potential shift as Fig.5 shows.

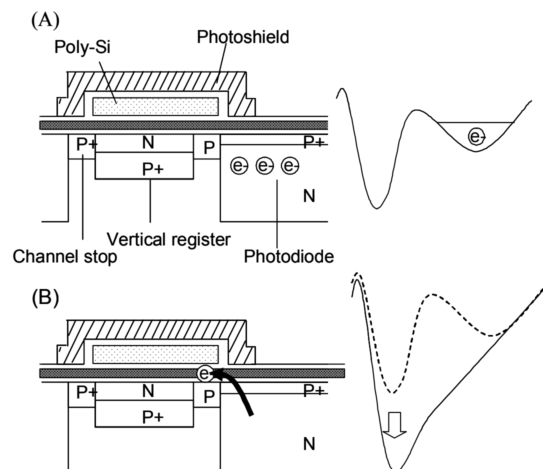


Fig. 4. Schematic of the cross sectional view and 1D potential profile from PD to vertical register during read out operation. (A) At the initial state, PD is fully accumulated by electrons. (B) The gate electrode is positively biased, electrons are flowing toward the vertical register. Few electrons are injected into SiN layer.

This phenomenon has already discussed for the case of SONOS (polysilicon-oxide-nitride-oxide-silicon) transistors under nonvolatile memory operation [1] [2]. Based on experiments, it is thought that the injection leakage current depends the thickness and electric field across each ONO insulator layer, and a variety of considerable number of different mechanisms occur, including FN tunneling, direct tunneling, modified FN tunneling, and trap-assisted tunneling. The leakage current starts to increase when an electric field of over 5 MV/cm is

applied across a 14.5-nm-thick oxide layer on the silicon [3].

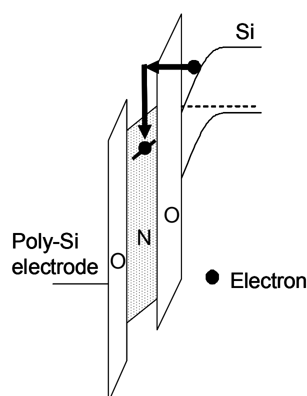


Fig. 5. Energy band diagram depicting electron tunneling and trapping in an ONO insulator.

We found that, even in the case of an IT-CCD having an ONO gate structure that has a thick oxide layer, the possibility of a gate leakage current still exists, and that it can cause significant damage to the charge transfer operation of the IT-CCD when a high electric field is applied.

3. Gate oxide structure

We previously developed and evaluated a 2.20-μm square pixel IT-CCD with a single-layer electrode structure. [4] By using such a structure, we could use an oxide layer as the gate insulator for the IT-CCD, without using a SiN layer. The gate insulator is not etched in the etching process steps during gate electrode formation and does not require reoxidation process steps that are required when constructing a second electrode. There is thus only one kind of insulator under the gate electrode in the image area (see Fig.6).

Such a gate oxide structure can reduce degradation of the charge transfer under high-electric-field operation. This is because charge-transfer degradation is caused by the SiN layer in the gate insulator, as mentioned above.

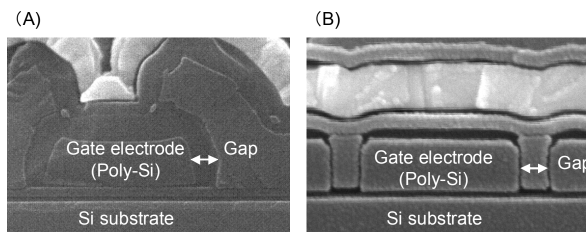


Fig.6 Cross sectional SEM photograph of (A) gate ONO and (B) gate oxide

Fig.7 shows the experimental results obtained. We applied +18% higher biases for charge transfer from the photodiode to the vertical register, and measured the charge transfer efficiency repeatedly. These results show no evidence of charge transfer degradation. We are convinced that gate oxide structures are effective means for overcoming the problem caused by high electric fields, which will become increasingly important as cell sizes are reduced.

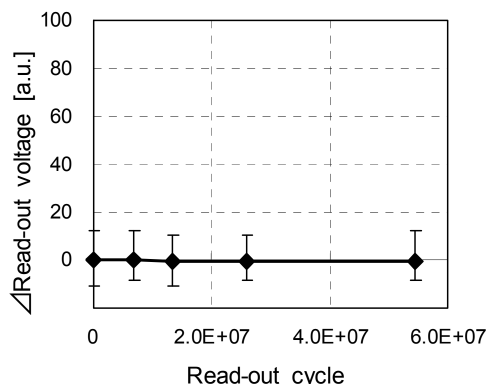


Fig.7 Read-out cycle dependency of ⊿Read-out voltage. (CTE>0.995)

A further advantage of gate oxide devices is that they have a shorter fabrication process compared with conventional ONO devices. The conventional structure requires more process steps, not just for ONO insulator formation for the CCD, but also for oxide insulators for peripheral transistors, necessary for the deposition and removal steps for the oxide and SiN layers. The gate-oxide-structure CCD proposed in this paper can considerably shorten the

process flow steps due to the multi-oxidation process.

4. Device performance

We have developed a 1.75-μm square pixel IT-CCD image sensor with 8M pixel of 1/2.5-type optical format having a gate oxide structure. The operation conditions used and the device characteristics are shown in Table 1.

The device performance is almost the same as a 2.20-μm square pixel single-gate-electrode IT-CCD. We realized a high performance for a very small cell size IT-CCD that is required to maintain image quality.

Table.1 Specifications and characteristics

Parameters	Values
Optical format	1/2.5 type
Chip size (mm x mm)	6.616 x 5.486
Total number of pixels	3336×2484(8.29M)
Number of active pixels	3298×2472(8.15M)
Pixel size (μm x μm)	1.75 x 1.75
Horizontal clock rate (MH	36
VDD / Read-out bias (V)	13/13
vertical transfer / horizontal transfer (V)	-7.5 / 3.3
Saturation output (mV)	420
Sensitivity (mV/Lux)	165

5. Conclusions

A single-layer electrode IT-CCD image sensor having a gate oxide insulator has been developed and applied to a 1/2.5-type 8M pixel high resolution IT-CCD image sensor. We confirmed that there was no degradation of charge transfer for this device, in contrast with ONO gate IT-CCDs. The performance of this newly developed device is very suitable for application to small-pixel image sensors and further reduction in pixel size. This advantage is especially relevant for small pixel sizes, in this study enabling a 1.75-μm square pixel IT-CCD.

6. Acknowledgement

The authors would like to thank all Sony Semiconductor Kyusyu corporation members for their support in device fabrication and Sony LSI Design members for their assistance with device characterization. We would also like to express special thanks to J. Kuroiwa, H. Yoshida, H. Ohki and Y. Keigo for their management support.

7. Reference

[1] J. H. Yi, H. Shin, Y. J. Park, and H. S. Min "Polarity dependent device degradation in SONOS transistors due to gate conduction under nonvolatile memory operations" IEEE Trans. Device and Materials Reliability, vol. 6, pp. 334 – 342, 2006

[2] S. Mori, et. al. "ONO inter-poly dielectric scaling for nonvolatile memory applications" IEEE Trans. Electron Devices, vol. 38, pp. 386 – 391, 1991

[3] M. Aminzadeh, S. Nozaki, and R. V. Gridihar, "Conduction and charge trapping in polysilicon-silicon nitride oxide-silicon structures under positive gate bias," IEEE Trans. Electron Devices, vol. 35, no. 4, pp. 459-467, 1988

[4] N. Karasawa, et. al. "A 2.20-Lm square pixel IT-CCD constructed from single-layer electrode" IEEE Workshop on CCD and Advanced Image Sensor, pp. 210-213, 2005

Optoelectronic Investigation for High Performance 1.4 µm Pixel CMOS Image Sensors

Seong-Ho Cho, Yunki Lee, YuYeon Yu, Gibum Kim, Hongki Kim, Hyunpil Noh, Kangbok Lee, Chang-Rok, Moon, Kwangok Koh, Keehyun Paik*, and Duckhyung Lee

Advanced Technology Research Team, *Computer Aided Engineering, Memory Division, Samsung Electronics Co., Ltd., San #24 Nongseo-Dong, Giheung-Gu, Yongin-City, Gyeonggi-Do, 449-711, KOREA

TEL: +82-31-209-8676, FAX: +82-31-209-3274, e-mail: seongho1.cho@samsung.com

Abstract

We have carefully investigated optoelectronic limitations in pixel shrinkage and successfully integrated 1.4 µm pitch pixel sensors into 8M density CMOS image sensors. In order to overcome these obstacles and so improve device performance with respect to key properties, we have focused on salient design of photon guiding optics and electron collection engineering. We have optimized these sensors to increase the luminance signal of which property determines spectral response of the pixel and image quality.

Introduction

As pixel size shrinks, both the optics related to finite aperture diffraction loss of photons and the electronics to collection of photo-electrons become more important than previous generations. Recently, we have developed the smallest pixel of 1.4 µm and improved its performance based on structural optimization by numerically solving these optoelectronic problems [1]. A key to this work is to employ the narrow local interconnect and tight design rule of metal lines. Thus, we are able to effectively guide on-axis and off-axis light beams through clear metal apertures and reduce optical stack height.

A raw image taken with this pixel sensor is processed throughout different steps of signal processing such as interpolation, auto-white balance, color processing, luminance-coefficient, and Gamma correction [2]. Mostly, we focus on obtaining a high Y-SNR that is defined by luminance signal to noise ratio, measured from a processed image of the Macbeth chart after the signal processing described above. The calculation of the Y-SNR includes the overall characteristics of spectral response, crosstalk, and noise. We improve image quality by maximizing the Y-SNR, instead of fragmentary refinements of pixel characteristics. It is noteworthy that the optimized spectral shape as well as low crosstalk is more important than merely high sensitivity, in order to increase the Y-SNR.

Numerical Simulations and Measurements

Inherently, one of main caveats in small pixels design is finite aperture diffraction loss of photons at the backend structure through which photons focused from the micro-lens are guided. Especially, the aperture size of metal opening and the height of entire metallic layers affect photon delivery, severely changing sensitivity in the 1.4 µm pixels. Due to the limitation of beam delivery in the 1.4 µm pixels, beam shaping through the back-end should be performed. For instance, both the size of the beam waist and the shape of the beam around the metal opening determine the transmission of the impinging light.

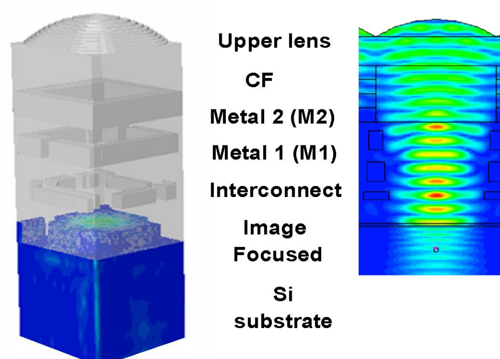


Fig.1. A three dimensional pixel of 1.4 µm pitch and a beam propagation pattern.

By calculating eq. (1) of the Fresnel diffraction through the square aperture of the pixel [3], we recognize that the propagation pattern resembles a circular aperture Fraunhoffer diffraction pattern as the image formed on the Si substrate is shown in Fig. 1,

$$\frac{jk}{2\pi z}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} square(\frac{x'}{l},\frac{y'}{l})\exp[-j\frac{k}{2z}\{(x-x')^2+(y-y')^2\}]dx'dy' \quad (1)$$

where ***square*** is an aperture function, z is a distance from the square aperture to a point in the pixel, k is a wave-vector, and l is the size of the pixel.

We conduct 2D and 3D finite-difference time-domain (FDTD) and beam propagation simulations to estimate optoelectronic photon loss throughout the backend structure and photo-electron conversion at the Si substrate. In a given curvature of the upper-lens, the opening size of the M1 critically affects the transmission of incident light in Fig. 2 as does the M2 opening. The beam loss through M2 drops more quickly than

through M1, since the beam waist is located below M2. Beam shaping is performed by optimizing lens height, equivalent to lens curvature, for efficient beam delivery in on-axis illumination in Fig. 3.

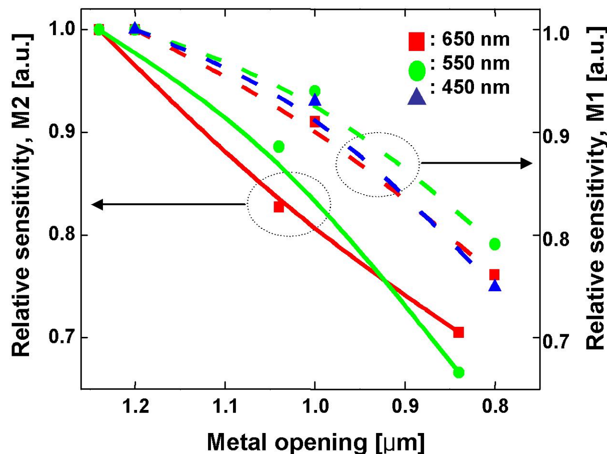


Fig.2. Sensitivity decreases as metal aperture sizes shrink in 3D FDTD simulations.

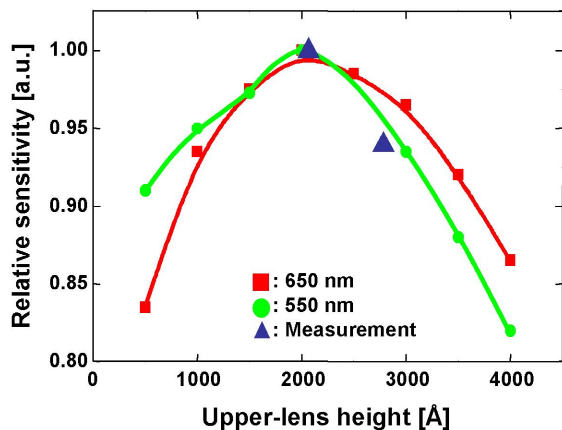


Fig.3. Sensitivity changes as lens thickness varies in 2D beam propagation method.

Fig. 4 shows the relative intensity of off-axis oblique light to three different color pixels. The measurement in Fig. 4 indicates that 3D loss is almost as twice as 2D loss, because of the assumption of infinite dimension along the other axis of the metal line. In this experiment, hand held lasers of three different colors are used. For the optimization of off-axis illumination, the lens and the color filters are shifted to the direction of light incidence.

Another crucial factor for high performance in small pixels is electrical crosstalk. Long wavelength photons deeply penetrate into the Si substrate due to low light absorption compared with other colors, diffusing and drifting to neighbor pixels. Fig. 5 elucidates how red photons move in the deep regions of the pixels. We modify the front-end structure in order to avoid electrical crosstalk between adjacent pixels for which implantation engineering strengthens photo-electron isolation. In addition, another implantation builds up a potential inclination along the flat region of the electrical potential. Thus, an effective collection of stray electrons to their own pixels is made.

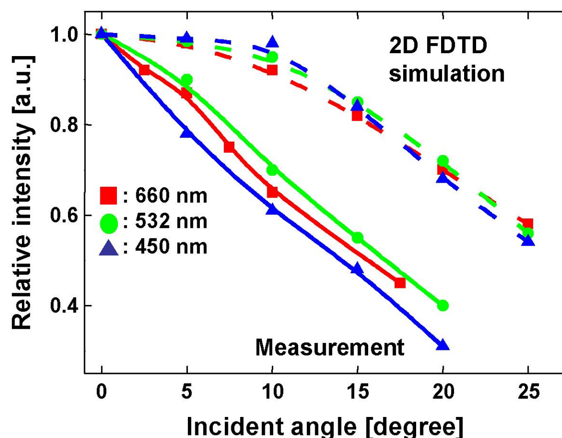


Fig.4. Sensitivity decreases as the incident angle increases.

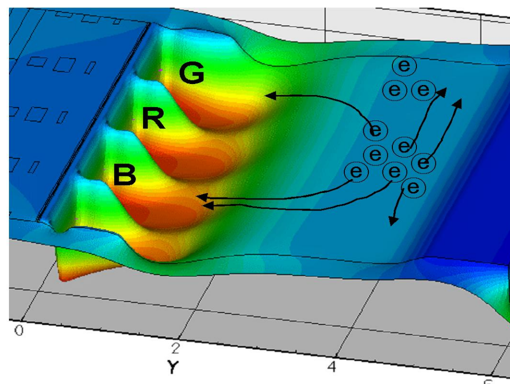


Fig.5. Electrical potential of each color pixel conceptually depicts electrons drift to adjacent pixels.

Fig. 6 shows two different spectra before and after the implantation processing for photodiode (PD) optimization. Using this method, we decrease crosstalk by 27% and increase Y-SNR by 16%, while maintaining the blooming barrier the same as before. Thus, we are confirmed that the potential wells are further stretched toward the flat region in the PD.

Fabrication and Device Performance

According to the simulation results and the design methods explained above, we successfully optimize the design and fabrication of the pixels. Mainly, W local interconnect and 65 nm CMOS design rule are employed to establish clear metal apertures in Fig. 7.

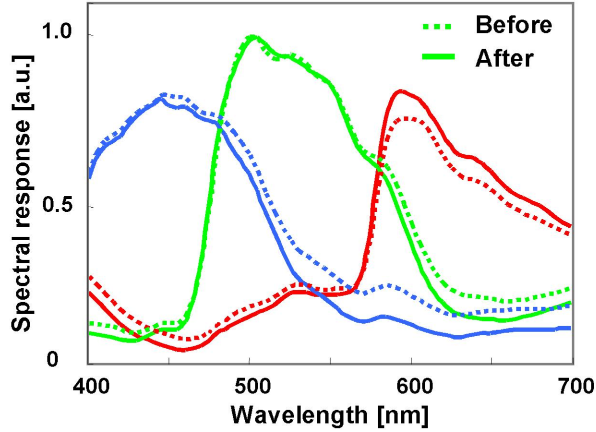


Fig.6. Relative spectral responses before and after photodiode optimization.

Additionally, the usable photodiode area is maximized using a 4-shared pixel structure of 1.75 equivalent transistors per pixel. These two techniques certainly help to maximize the fill factor and reduce optical stack height.

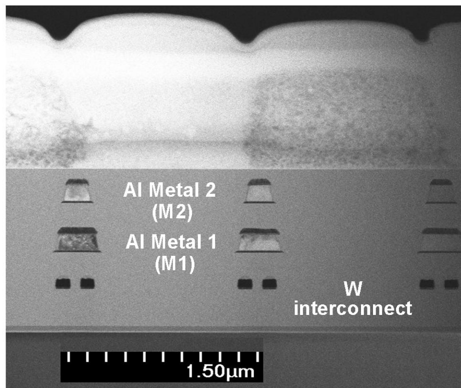


Fig.7. An image of a scanning transmission electron microscope shows a detailed vertical structure of 1.4 μm pitch pixel sensors.

The aspect ratio that is pixel height below micro-lens to pixel pitch becomes as low as 1.7, by reducing the vertical structure. Besides reduced sensitivity with 1.4μm pitch compared to larger pixel size, saturation charges tend to be diminished since the detectable PD area shrinks. As an approach to compensating degraded characteristics in pixel shrinkage, the area of the PD capacitor is especially extended with n-type doping prior to the formation of the poly-Si transfer-gate whose process flow is shown in Table 1. Thanks to this method, saturation charge is increased by 10%, and the image lag is diminished by 50%. Color filters are processed with standard negative resists, and then zero-gap upper-lenses are fabricated. Lens fill factor is approximately 90%. Important pixel parameters are enumerated in Table 2.

Table 1. Brief process flow of a conventional photodiode fabrication scheme vs a new scheme.

Structure	Conventional photodiod	Extended photodiode
Key Process Flow	STI formation	STI formation
	Well and V_t implantation	Well and V_t implantation
	Gate-poly patterning	Photodiode formation
	Photodiode formation	Gate-poly patterning
	Three Al backend steps	Two Al and one W

Table 2. Pixel parameters of 1.4 μm pitch imagers.

Item	Parameter
Number of pixels	3360 x 2476
Dynamic range	58 dB
Sensitivity	4500 e/lux·sec
Dark level @ 60°C	16 LSB/sec
Lag	< 1 LSB
Optical fill factor	60%

For a demonstration of this pixel sensor, we capture an image shown in Fig. 8.

Fig.8. A captured image of 1.4 μm 8M pixel sensors.

Conclusion

In summary, we have investigated crucial problems of low sensitivity and low saturation in 1.4 μm pixel pitch, based on advanced optoelectronic analysis and process architecture for 8M CMOS image sensors, and demonstrated their high performance.

REFERENCES

[1] Chang-Rok Moon, *et al.*, "Detailed process architecture and the characteristics of 1.4 μm pixel CMOS image sensor with 8M density," *Sym. on VLSI Circuits*, Japan, June 2007.

[2] Abbas El Gamal, *et al.*, "CMOS image sensors," *IEEE Circuits & Devices Magazine*, 2005.

[3] Max Born and Emil Wolf., *Principles of Optics*, 6th Ed., Pergamon Press, 1980.

Active Pixel Sensor Arrays in 90/65nm CMOS-Technologies with vertically stacked photodiodes

S.Henker[1], C. Mayr[1], J.-U. Schlüßler[1], R. Schüffny[1], A. Heittmann[2], U. Ramacher[3]

[1] Univ. of Technology Dresden, Institute of Circuits and Systems (IEE), Helmholtzstr. 10, 01062 Dresden, Germany, {henker,mayr,schlue,schueffn}@iee.et.tu-dresden.de, Tel.: ++49 351 463 33602, Fax: ++49 351 463 37794

[2] Qimonda AG, Munich, Germany, Arne.Heittmann@qimonda.com, Tel.: ++49 89 234 52067

[3] Infineon AG, Munich, Germany, Ulrich.Ramacher@infineon.com, Tel.: ++49 89 234 41296

Image sensors using 90nm and 65nm CMOS technology were developed, exhibiting characteristics competitive with commercial sensors in conventional technologies. New pixel configurations with stacked photodiodes and high fill factor have been evaluated. Image sensors in deep-submicron can take full advantage of the technology shrink for digital image restoration, balancing remaining technological deficiencies and offering additional processing capabilities.

Today's CMOS sensors are chiefly fabricated in 0.25µm CMOS technology and incorporate a custom DSP for image enhancements [1]. This work is focusing on evaluation of 90/65nm CMOS technology for active photosensor arrays and analog/mixed signal readout circuits. To compensate for the expected larger insufficiencies of the analog sensor array, advantage can be taken of the shrinking potential of further sub-100nm CMOS technologies to implement image enhancement techniques by digital post processing [2, 3]. Application is aimed at embedded imagers for digital cameras in handhelds and alike, using standard digital processes for Systems on Chip. As far as the authors are aware, this is the first study of pixel sensors in sub-100nm CMOS technologies.

Two active pixel arrays have been fabricated in 90nm and 65nm CMOS process respectively with 6+1 layer metal stack and copper interconnects (Figure 6). The first chip serves for pixel evaluation and contains a total of 21 pixel arrays with different photo diode and reset configurations. Pixel size is 6x6µm and fill factor is varying between 44 and 60%. The second chip has been designed in 65nm CMOS technology to evaluate a larger sensor array and analog and mixed-signal components of the readout data path. It contains a 128x96 pixel array of 6x6µm dual channel pixels with 46% fill factor (Figure 1). Additional a 48x96 pixel array of smaller 3x3µm single channel pixels utilizing embedded transistor reset and 38% fill factor (Figure 2) is inserted. Beside the pixel arrays, the 65nm evaluation chip also includes circuits for analog processing such as several amplifiers, a pipeline ADC and a ΣΔ-ADC and their associated digital controls.

For sensor operation we use linear light energy measurement by integrating a reverse biased junction diode capacitor. The measurement process consists of 3 phases: the resetting of the capacitor to a fixed voltage using a reset element, the integration of the light induced current over a distinct amount of time and the readout of the voltage difference on the capacitor using a readout element. The received light energy is then directly proportional to the voltage change on the capacitor. Reset and readout on pixel level are commonly implemented with a transistor switch respectively a source follower, resulting in a 3T pixel cell [4].

The general problems with imager design on sub-100nm derive mainly from technology constraints [5]: The consequences of transistor scaling are increased leakage due to high doping concentration, steep implant profiles and increased oxide interface trap states caused by shallow trench isolation. Short channel effects significantly increase transistor off-current and some devices also show considerable gate leakage which further discharge integrating and sample&hold capacitors [5]. For purpose of comparison, we use different transistor options on the 90nm chip, such as low leakage devices (LLD) and analog IO devices (ANA) and implemented different reset circuits and different reset schemes to reduce leakage and suppress temporal noise (Figure 6). Compared with LLD, analog IO devices show several advantages, esp. lower channel leakage and basically no gate leakage. LDD transistors are smaller in size, but operate at

1.2V supply voltage, which reduces the available signal swing and dynamic range. Since leakage is generally increasing with technology shrink, the sensor in 65nm technology is implemented using IO devices only.

Further, we are using different configurations of junction diodes as photo element, focusing on well diodes, since the junction leakage of diffusion diodes is in general orders of magnitude higher because of their doping concentration. In general, well diodes are not very common in pixel design due to their large interspace requirements. Our solution is to partially compensate this by applying moat layers, which prevent the doping implantation of the surrounding p-well. The resulting p-i-n diode structure shows reduced junction leakage and an enhanced depletion region as well as smaller capacitance and thus improved sensitivity. However, due to the implantation depth, a well diode shows higher sensitivity especially in the infrared region compared to shallow diffusion diodes.

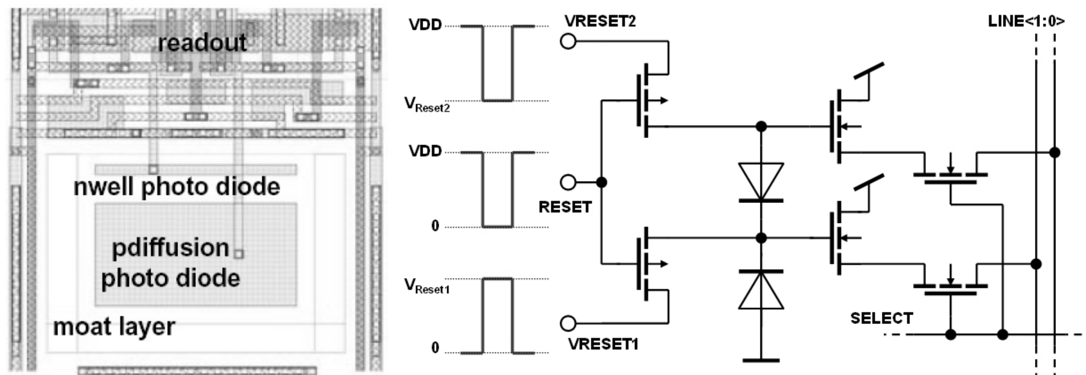


Figure 1: 6T dual channel pixel

In addition, different pn-junctions (n-well, diffusion, triple-well) were arranged to form vertically stacked photo diodes with distinguishable spectral characteristics [2] (Figure 1). These pixel structures require separate reset and readout for the different diodes, but provide multiple output signals. These outputs are sampled on identical spatial and temporal coordinates. These multi-channel sensors avoid/simplify the color filter array necessary for color reproduction in visual range. Furthermore multi sensor channels allow in particular to control the infrared response by using a novel approach to suppress or emphasize infrared light for special applications [3].

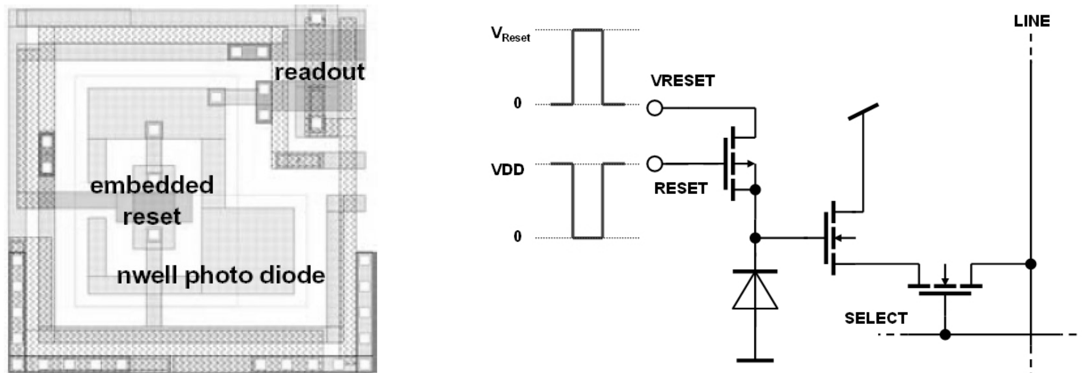


Figure 2: 3T pixel cell with embedded PMOS reset

Using single channel pixels, the fill factor of a well diode pixel can be further improved by embedding a PMOS reset transistor directly into the diode n-well (Figure 2). Compared to standard NMOS reset this special technique gives the advantage of threshold voltage dependent fixed pattern noise cancellation and an increased signal swing at the expense of higher transistor leakage.

Measurement results prove that important imager parameters like sensitivity, dark current, and resolution

in a standard deep-submicron CMOS technology are comparable with state of the art CMOS-imagers using special photo process options (Figure 3). The FEOL part of photosensitive elements, i.e. the dopant profiles, is usable for visible range and infrared.

Feature	Unit	90nm, nwell with moat	90nm, nwell/pdiff with moat	90nm, nwell w/o moat	90nm, nwell/pdiff w/o moat	65nm, nwell with moat	65nm, nwell w/o moat	180nm Reference [5]
pixel size	μm^2	6x6	6x6	6x6	6x6	6x6	3x3	3.5x3.5
integrating capacitor	C / fF	8.2	13.2	12	16.2	11	4.3	4.5
dark current sensitivity	Rdark/ mV/s	23	37	210	71	50	7700	6.29
saturation	Nsat / e-	61199	98876	89888	120974	82397	48315	22472
reset noise (kT/C) [1)]	Nrn / e-	36	46	44	51	42	26	20
dark current noise	Ndn / e-	23	61	315	143	69	2067	4
noise floor	Nn / e-	43	76	320	152	81	2067	21
SNR [2)]	dB	61.2	59.3	48.0	55.9	60.2	27.4	61

1) reset noise is assumed to be 1*sqrt(kT/C), not yet measured, (Reference [5]: 0.75*sqrt(kT/C))
2) based on measurements of dark current and reset-noise estimation

Figure 3: Comparison of different diode configurations

Figure 4 (left side) shows the spectral sensitivity of different diode configurations of the 90nm design. Within the right side of this figure sensitivities of the double channel pixel and the smaller single channel pixel on 65nm chip are compared. As seen in Figures 4, sections of spectral range are suppressed. This is caused by the copper wire metal stack with many dielectric layers and strong varying reflective index, which leads to distinct interference effects, since the layer thickness is within the range of λ/2. The main minima of the resulting light transmission characteristic are determined by layer structure, thickness and dielectric coefficient of the isolating materials of the backend process, but the transmission characteristic also shows high variability due to the strong dependence on fabrication parameters.

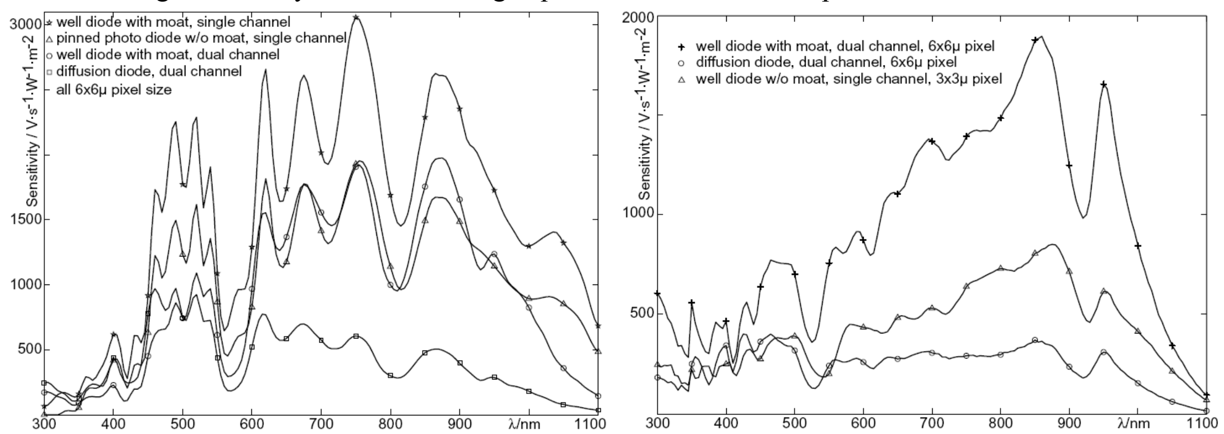


Figure 4: Spectral sensitivity of 90nm (left) and 65nm (right) photo diodes (30nm spectral gap width)

Simulated transmission characteristics show a good match with measured characteristics and can thus be used for technology optimization in respect to photo sensors [5]. Figure 5 shows sample images taken from contiguous pixel areas of the test chips.

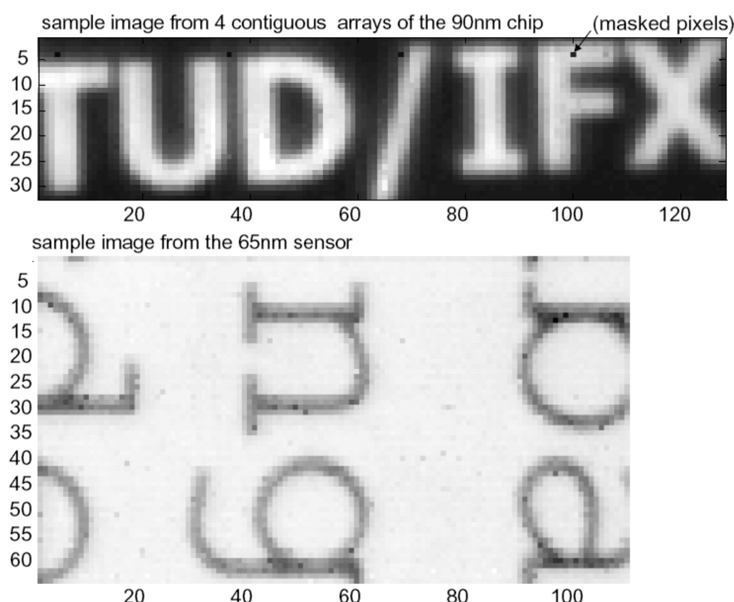


Figure 5: Images samples taken with pixel evaluation chip (top) and sensor evaluation chip (bottom)

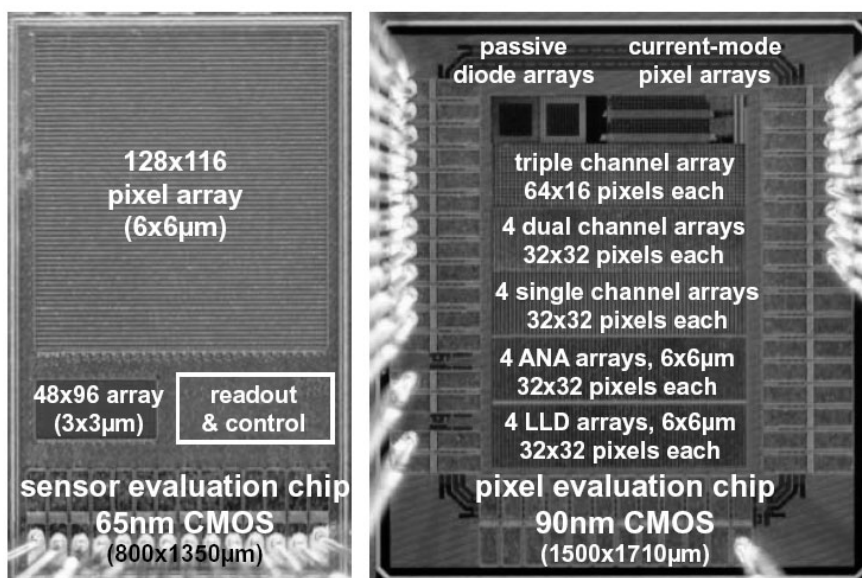


Figure 6: Die Photographs

References

[1] U. Ramacher, I. Koren, H. Geib, C. Heer, T. Kodytek, J. Werner, J. Dohndorf, J.-U. Schlüßler, J. Poidevin, S. Kirmser, “Single-Chip Video Camera with Multiple Integrated Functions,” *International Solid-State Circuits Conference ISSCC'99*, pages 306-307, 1999.

[2] A. E. Gamal, “Trends in CMOS image sensor technology and design,” *Digest of IEEE International Electron Devices Meeting*, pp. 805-808, December 2002.

[3] S. Henker, J.-U. Schlüßler, R. Schüffny, “Concept of Color Correction on Multi-Channel CMOS Sensors,” *Digital Image Computing: Techniques and Applications, Proc. of the 7th Biennial Australian Pattern Recognition Society Conference - DICTA 2003*, vol. 2, pp. 771-780, Dec. 2003.

[4] J. Yang, K. G. Fife, L. Brooks, C. G. Sodini, A. Betts, P. Mudunuru, H.-S. Lee, “A 3MPixel Low-Noise Flexible Architecture CMOS Image Sensor,” *ISSCC Digest of Technical Papers*, pp. 496-497, Feb. 2006.

[5] *IBIS4-6600 High resolution 6.6 M Pixel Rolling shutter CMOS Image sensor Datasheet*, Cypress Semiconductor Corporation, San Jose, CA, 2005.

Auto-Focus Technology

R.C. Gutierrez, E.R. Fossum, T.K. Tang

Siimpel Corporation, 1055 E. Colorado Blvd., Suite 410, Pasadena, CA 91106

ABSTRACT

Several technologies that are being developed for auto-focus (AF) in miniature cell phone cameras are discussed. These include lens-motion-type AF, lens-modification-type AF, and extended depth of field AF. Len-motion-type AF includes stepper motor, voice coil, piezoelectric, electropolymer and micro-electro-mechanical-system (MEMS) technologies. In all these, precise alignment and motion control of the lens relative to the imager is important for image quality. Lens-modification-type AF includes liquid lens and solid-state electro-optical devices. Lens shape and/or refractive index changes are the key to implementing these types of AF. Extended depth of field AF use annular apodizers or wavefront coding to increase the depth of field by increasing the F# or using image processing techniques. Achieving good SNR in the presence of noise and image surrealism are the challenges in extended depth of field AF.

1. INTRODUCTION

The increased performance expectation for digital cameras in cell phones is driving the image sensor industry to develop smaller pixels that will enable the miniaturization of 2-8 Mpixel cameras to fit these mobile platforms. At the same time, optics companies are developing smaller and more precise lens barrels. Module integrators are developing more capable optical systems to take advantage of these new image sensors and lenses as they become available. These efforts need to be carefully coordinated in order to fulfill the promise of stand-alone digital still camera (DSC) quality in a cell phone.

Auto focus (AF) is commonplace for DSCs where volume and power dissipation are less critical. AF is only recently being introduced into cell phone cameras where size is very critical, and power dissipation is also of concern. Stepper motors, commonly used in DSCs, do not scale well to the requirements of the cell phone camera and different technologies have emerged. Active AF systems that use structured light or ultrasonics to determine focus are also not well suited for the size and power constraints inherent in cell phone cameras. This paper will describe the various technologies being pursued for AF and some of their advantages and disadvantages.

All technologies need to be evaluated in terms of characteristics required for cell phone cameras. These include small size (e.g. 10 x 10 x 6 mm), low cost (typically less than $2), reliability (millions of cycles), wide environmental operating range (from car dashboard in the sun to subzero freezing temps), and high shock survivability of up to 8,000-10,000Gs.

2. AUTO-FOCUS SYSTEM OVERVIEW

The AF system is composed of the image sensor, image processing, AF algorithm, driver circuit, AF actuator, and an imaging lens, as shown in Figure 2. The image sensor, image processing, and AF algorithm blocks are often integrated onto a single chip called the imager system on a chip (SOC). The lens and the image sensor must be designed to match each other for optimum performance. For example, the chief-ray angle (CRA) as a function of distance from the center of the image must be matched for the lens and image sensor. Mismatch in CRA can lead to pixel crosstalk and color artifacts. The optical resolution and imager resolution must be matched to maximize picture sharpness and avoid image artifacts caused by under-sampling.

There are various technologies available for the AF actuator. The AF actuator is responsible for modifying either the position of the imaging lens with respect to the imager or the optical properties of the imaging lens. To pick the best AF actuator for a cell phone camera, it is important to consider its effects on image quality, size, reliability, and power consumption.

Several technologies being developed for AF in miniature cell phone cameras include lens-motion-type AF, lens-modification-type AF, and computational-type AF. Lens-motion-type AF includes stepper motor, voice coil, piezoelectric, electropolymer and micro-electro-mechanical-system (MEMS) technologies. In all these, precise alignment and motion control of the lens relative to the imager is important for image quality. Lens-modification-type AF includes liquid lens and solid-state electro-optical devices. Lens shape and/or refractive index changes are the key to implementing these types of AF. Computational-type AF use wavefront coding to cause predetermined "blurring" of the image that can be removed using image processing techniques. Achieving good SNR in the presence of noise and numerical rounding, and image surrealism are the challenges in computational-type AF.

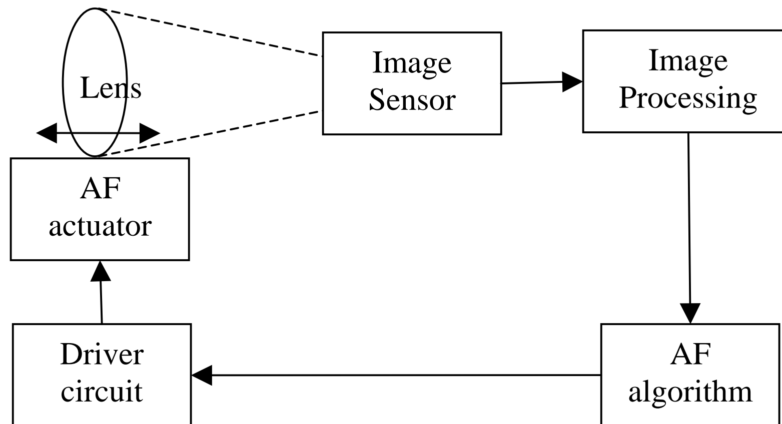


Figure 1. Block diagram illustrating the system level operation of an AF system.

For lens-motion-type and lens-modification-type AF, the control loop requires the capture of an image, processing of the image to evaluate focus, moving or modifying the lens to a next value, capturing another image, calculating a new focus score, etc., until some optimum focus position has been passed through. The lens is then set to the condition of best focus. The lens position or shape, etc., must return to the same value it had when the best focus score was achieved. The presence of hysteresis (not returning to the same position) can result in an out of focus image, or a need to redo the loop leading to latency, or a need for position sensing. The latter adds cost, size and additional complexity to the design and should be avoided. Computational focus is either deterministic and does not require a focus-score feedback, or the feedback takes place completely in the computational domain.

The AF process must take place in the shortest possible amount of time. This is to avoid user frustration over "missed photo opportunities" associated with latency. Continuous focus is a possible solution but it requires more power.

3. AF USING MOTION OF AN OPTICAL ELEMENT

When moving an entire lens barrel, it is important that the lens barrel is properly positioned with respect to the imager in all but one degree of freedom. The position of the lens barrel along the optical axis (z-axis) affects focus, so it is important to have the ability to place the lens barrel with better than 10 micrometer precision. Position in the x and y axes affects the chief-ray-angle (CRA) matching of the optics and imager, as well as the relative illumination and distortion, so it is important to place the lens barrel optical axis with the imager active area center with better than 50 micron accuracy. The position of the lens barrel in pitch and yaw affects the optical resolution as shown in Figure 2. The vertical axis is the modulus of the optical transfer function (from 0 to 1) and the horizontal axis is the spatial resolution on the horizontal axis (from 0 to 125 cycles/mm). The graph on the left is for a lens barrel that is properly aligned, while the graph on the right is for a lens barrel that is misaligned in pitch by 2 degrees. Whereas a properly aligned lens barrel has > 30% MTF at 125 cycles/mm, a misaligned lens barrel has some portions of the image with < 30% MTF at about 30 cycles/mm. As a result, it is important to place the lens barrel with a pitch and yaw accuracy of < 0.3 degrees.

Lens-motion-type AF then has two key requirements. First, the motion must be controlled with optical precision. Second, the actuator must use low power and occupy small space. Thus, stepper motors that use a rotary electromagnetic actuator and gears to convert the rotary motion into linear motion are not suitable due to their relatively

large size, larger cost, and low shock survivability. Although stepper motors were used in DSCs in the first autofocus cameras, they are largely not being applied to the cell phone camera market.

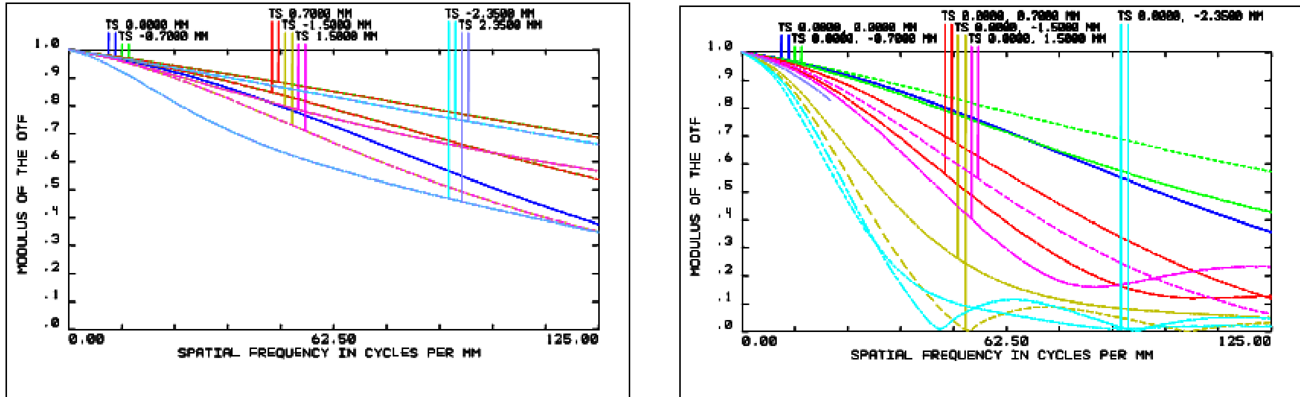


Figure 2. Plots showing the MTF as a function of the spatial frequency for a properly aligned lens barrel (left) and a lens barrel with a misalignment of 2 degrees in pitch (right). The various curves are for different positions on the imager.

MEMS technology, which uses photolithography and etching of silicon wafers to enable moving mechanical structures with less than 1 micron tolerance, ensure that the lens is optimally positioned with respect to the imager for AF [1]. This, in turn, ensures a high quality picture. A photograph of a MEMS AF digital camera and the MEMS components that make this type of camera possible are shown in Figure 3.

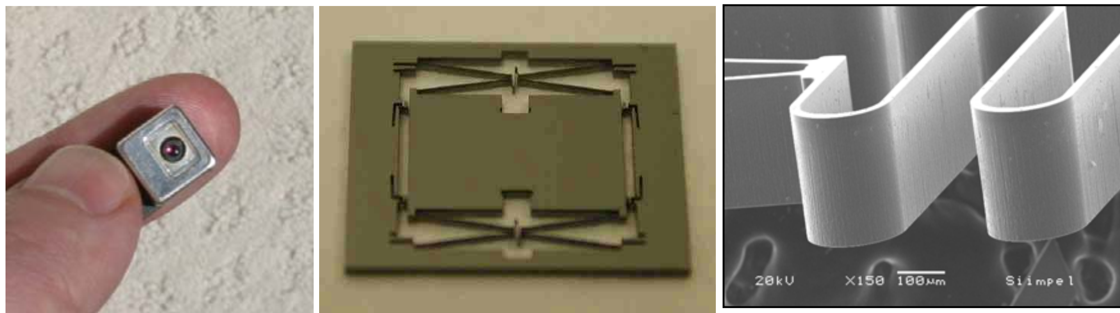


Figure 3. Photograph of a MEMS digital camera for use in cell phone (left), photograph of the MEMS stage used for AF (center), and scanning electron microscope photograph of a portion of the MEMS stage (right).

The voice-coil motor (VCM) and the MEMS actuator both use linear electromagnetic actuation, which use interaction between a permanent magnet and the magnetic field generated by the current flowing through a coil. However, the motion control for each of these two technologies has widely different tolerances and only the MEMS actuator ensures the proper lens positioning previously specified. For example, Figure 4 shows measurements of the position accuracy for a MEMS and VCM actuator. This data was taken using a laser metrology system of the lens position (y-axis from 0 to 350 microns) vs. the code given to a 10 bit current mode digital to analog converter (x-axis from 0 to 1024 corresponding to 0 to 100 mA). The plot on the left shows the data for the MEMS actuator, whereas the plot on the right shows the data for a VCM from a cell phone. The VCM has considerable hysteresis. As a result of the improved positioning accuracy, MEMS provides improved imaging quality. In addition, MEMS has advantages in size and environmental robustness, as a result of the machining precision of silicon micromachining and the strength of silicon.

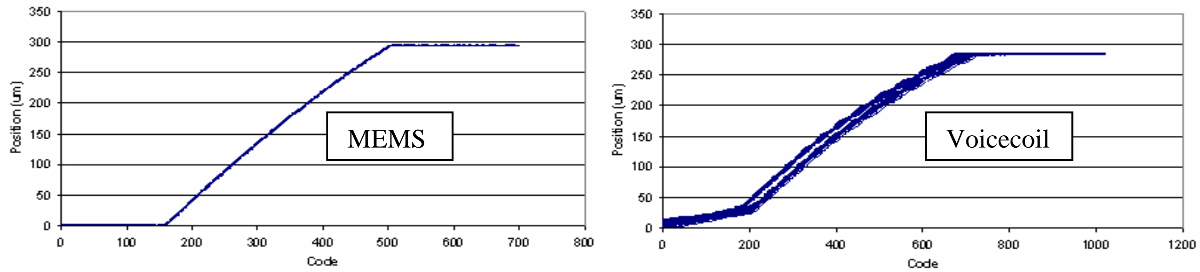


Figure 4. Plot comparing positioning accuracy along optical axis for MEMS (left) and voicecoil (right) AF actuators.

Many solutions have been implemented using piezoelectric actuation. For example piezoelectric actuators from Limited 1 and New Scale Technologies are shown in Figure 5. The Limited 1 actuator is unique in that it achieves mechanical motion amplification by making a coil of piezoelectric material. The Squiggle motor from New Scale Technologies uses piezo actuators to turn a screw and achieve large motion through thousands of small steps. The main disadvantage of piezoelectric actuators is that they require position sensing due to their large hysteresis and poor positioning repeatability. The position sensor requirement combined with the limited strength of piezo materials translate into disadvantages in size and environmental robustness.

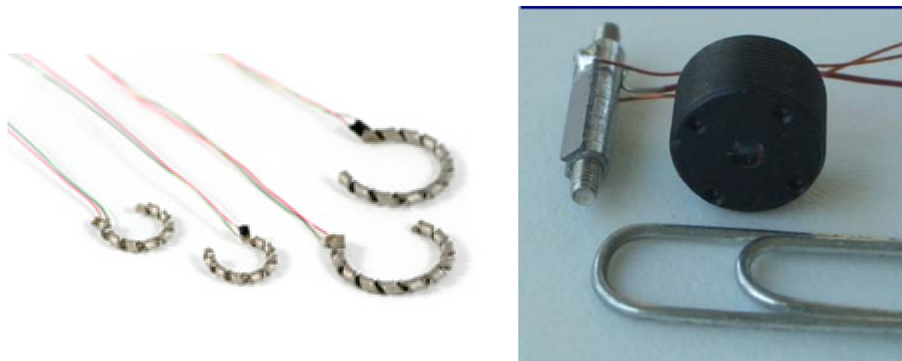


Figure 5. Piezoelectric AF actuators from Limited 1 (left) and New Scale Technologies (right).

Artificial Muscle uses electropolymers for AF actuation. Although electropolymers have the advantage of large actuation energy density, their dependence on water in the polymer raises significant problems in environmental robustness. In addition, the electropolymers would have the same limitations as piezoelectric materials in terms of hysteresis, poor motion control, and environmental robustness.

4. AF USING MODIFICATION OF AN OPTICAL ELEMENT

When modifying the optical properties of an optical element to adjust focus, it is important that the optical element does not introduce additional aberrations and does not absorb any light. The optical aberrations are carefully controlled in the design of an imaging lens system by using aspheric surfaces and selecting materials with specific values of index and Abbe numbers (optical dispersion). Liquid lens from Varioptic is the most published approach [3] that uses the modification of the optical properties of a lens to achieve focus control. A liquid lens varies the radius of curvature of the surface joining two liquids with different index of refraction to change optical properties. Because the optical surface created by these two liquids is spherical (as opposed to aspheric), this technology has significant limitations in terms of optical performance. Figure 6 shows a photograph of the liquid lens from Varioptic and a camera using the liquid lens for AF.

Figure 6. Photograph of a camera (left) using liquid lens from Varioptic (right).

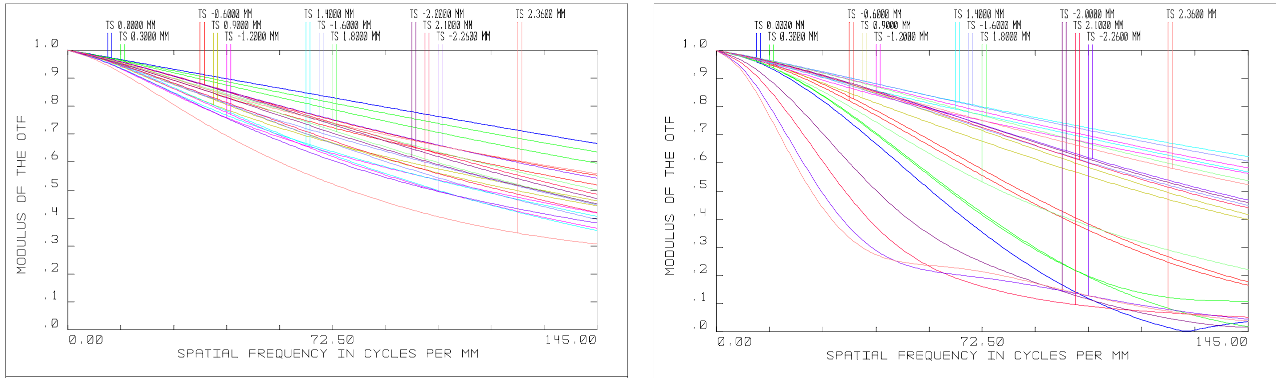


Figure 7. Optical performance comparison between an AF based on moving a lens barrel (left) and liquid lens (right) for F# 2.5. The horizontal axis is the spatial frequency on the imager surface, and the vertical axis is the modulus of the optical transfer function (MTF). Plots show modeling results at 10 cm focus.

In order to quantify the effect that liquid lens has on the image quality, we modeled the MTF of an imaging system with F# 2.5 when focusing on an object at 10 cm both using a liquid lens and moving the lens barrel. This is shown in Figure 7. In the plots, the vertical axis is the modulus of the optical transfer function (from 0 to 1) and the horizontal axis is the spatial resolution on the horizontal axis (from 0 to 145 cycles/mm). The graph on the left is for moving a lens barrel, while the graph on the right is for liquid lens. Whereas a properly aligned lens barrel has > 30% MTF at 145 cycles/mm, a liquid lens has some portions of the image with < 30% MTF at about 30 cycles/mm. This modeling was done assuming a perfect alignment of the liquid lens, so additional issues are possible if the optical axis of the liquid lens and/or barrel is not aligned with the rest of the imaging system. In addition to the reduced resolution, additional disadvantages of the liquid lens are increased thickness of the camera, and reliability that depends on proper sealing, separation, and stability of two fluids.

5. EXTENDED DEPTH OF FIELD

Finally, there is also a separate group of technologies being applied to achieve extended depth of field in order to eliminate the need for AF in cell phone cameras. Although these approaches may eliminate the need for AF, they do so at the expense of image realism, as the human brain is not used to seeing objects at different distances all in focus.

The standard approach to increase the depth of field is to reduce the entrance pupil diameter by placing a spatial filter that only allows light in the center of the lens to pass through the optical system. This increases the F# of the lens and, as a result, increases the depth of focus. A camera using this approach is often referred to as a “pinhole” camera. The advantages of this approach are that the lens becomes very simple to design and manufacture, and that objects from 10 cm to infinity can be at the same focus position of the lens. The disadvantages are lower resolution and bad low light performance.

A new approach to increase the depth of field is to reduce the effective entrance pupil diameter by placing a spatial filter that only allows light in the center of the lens to pass through the optical system without phase disruption. Since light

from the entire aperture falls on the imager, image processing is used to reconstruct the image using knowledge of the phase disruption at the entrance pupil plane. This approach is also known as computational AF. Although this approach does not directly increase the F# of the lens, it effectively increases the F# of the imaging system (after image reconstruction) and, as a result, increases the depth of focus. The advantages of this approach are that the lens becomes very simple to design and manufacture, and that objects from 10 cm to infinity can be at the same focus position of the lens. Compared to the "pinhole" camera, this approach has the advantage that the amount of light falling on the imager is increased, and this can be used for the low frequency components of the image. The disadvantages are lower resolution, bad low light performance, increased image processing requirements, additional optical element, and higher power consumption.

6. ACKNOWLEDGMENTS

The authors gratefully acknowledge the many contributions of fellow Siimpel employees in the analysis of competing AF actuator technologies.

7. REFERENCES

[1] Roman C. Gutierrez, Tony K. Tang, Robert Calvet, Eric Fossum, "A MEMS Digital Camera", SPIE Electronic Imaging – Digital Photography III Proc. SPIE vol. 6502 paper 36, January 28-29, 2007

[2] David A. Henderson, "Piezo ceramic motors improve Phone Camera Autofocus and Zoom," article in www.squiggle.com, May 16, 2005

[3] B. Berge, J. Peseux, "Variable focal lens controlled by an external voltage: an application of electrowetting", Eur.Phys. J. E. 3, pp159-163, 2000.

[4] M. Mino and Y. Okano, ``Improvement in the OTF of a Defocused Optical System Through the Use of Shaded Apertures," Applied Optics 10, 2219-2225 (1971)

[5] J. Ojeda-Castañeda, P. Andres, and A. Diaz, ``Annular Apodizers for Low Sensitivity to Defocus and to Spherical Aberration," Optics Letters 11, 487-489 (1986).

[6] Edward R. Dowski, Jr. and W. Thomas Cathey , "Extended Depth of Field by Wavefront Coding", (1995)

A Wide Dynamic Range CMOS Image Sensor with Resistance to High Temperatures

Koichi Mizobuchi[1], Satoru Adachi[1], Tomokazu Yamashita[1], Seiichiro Okamura[1], Hiromichi Oshikubo[1], Nana Akahane[2] and Shigetoshi Sugawa[2]

[1]DISP Development, Texas Instruments Japan, 2350 Kihara, Miho, Inashiki , Ibaraki 300-0496, Japan
Tel: +81-29-880-4066, Fax: +81-29-880-3242

[2]Gradute School of Engineering, Tohoku University, 6-6-11 Aramaki, Aza-Aoba, Aoba-ku, Sendai, 980-8579, Japan
Tel: +81-22-795-4833, Fax:+81-22-795-4834

E-mail: {mizo, chiro, cdty, iapo, hiromichi-oshikubo}@ti.com, {nana, sugawa}@fff.niche.tohoku.ac.jp

Abstract

A 1/4 inch VGA 5.6 μm pixel pitch wide dynamic range (WDR) CMOS image sensor with resistance to high temperatures has been developed using a very-low-dark-current front-end of line (VLDC FEOL), a metal hermetic seal package and/or the inorganic cap layer to suppress the degradation of the spectra response of the on-chip micro lens and color filter (OCML/OCCF). The dark current is reduced to 175 e^-/sec-pixel at 85˚C (25 e^-/sec-pixel at 60˚C) by the use of VLDC FEOL. Sensor chips with no cap and an inorganic cap onto the OCML were assembled into a metal seal package and a conventional package respectively. They were exposed to a 150˚C/ 500 hours thermal-stress test in the air. No degradation of the spectra response in any of R/G/B pixels for both samples is observed after the thermal stress test. The sample images captured by the WDR CMOS image sensor with and without the thermal stress show no significant degradation in image quality up to 85˚C. The image sensing performance results in a low noise and huge effective saturation voltage. The dynamic range is extended to 93 dB.

Introduction

A wide-dynamic-range (WDR) CMOS image sensor using a lateral overflow integration capacitor in each pixel demonstrated over-100 dB dynamic range (DR) in single exposure and over-200 dB DR in multiple exposures plus the current readout operation, keeping a high sensitivity and a high S/N ratio [1-4]. Automotive applications, for which this sensor best suits, require an operation temperature typically ranging from -40 to 85 ˚C or much higher. Security and medical applications also desire the extension of operation temperatures. In these hard conditions, especially at very high temperatures, the increase of dark current shot noise requires careful attention. Thermal decomposition of organic materials in the sensor chip and/or the package is also an issue. Several papers have reported dark current reduction approaches [5,6]. However a temperature-resistant image sensing solution has not been clearly reported as the discussion has just started [7]. This paper describes a WDR CMOS image sensor with resistance to high temperatures using a very-low-dark-current front-end of line (VLDC FEOL) and an inorganic cap on the on-chip micro lens (OCML) as well as a metal hermetic seal package to suppress thermal decomposition of both the OCML and the on-chip color filter (OCCF).

Dynamic Range Enhancement

Fig. 1 shows a pixel schematic circuit diagram adopted for the wide dynamic range solution. The pixel circuit consists of a fully depleted photodiode (PD), a floating diffusion to convert the charge to the voltage (FD), a charge transfer switch (M1), an overflow photoelectron integration capacitor (CS), a switch between the floating diffusion FD and the overflow capacitor CS (M3), a reset switch (M2), a source follower amplifier (M4) and a pixel select switch (M5). The basic concept in this pixel circuit is to use the switch M1 for a suitable overflow path of saturated photoelectrons and integrate overflowed photoelectrons in FD and CS during a charge integration period. The non-saturated photoelectrons are transferred from PD to FD and converted to the voltage as a high sensitivity low light signal (S1) as well as the conventional 4 transistors type CMOS image sensor. The dynamic range is extended by fully utilizing the photoelectrons integrated at and overflowed from PD for a bright light signal (S2).

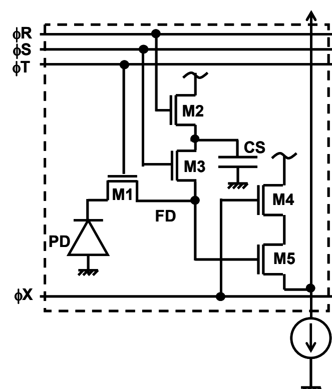


Fig.1 Pixel schematic of wide dynamic range (WDR) CMOS image sensor.

One of the advantages in this CMOS image sensor is high tolerance to reset noise and dark current in the signal S2 [4]. Since the signal S2 is a mixture of the non-saturated and the saturated overflow photoelectrons, the minimum number of photoelectrons in S2 is close to the number of the saturated photoelectrons in S1 for the case of S2 selected. Precisely speaking, the only N2 in the next frame (defined as N2') can be stored in the same horizontal blanking period, however the fixed pattern noise is removed by the subtraction of (S2+N2)-N2' in the same horizontal blanking period and a high S/N ratio can be realized in the region of S1/S2 switch. This noise reduction method offers the simple operation without the necessity of the off-chip frame memory.

In order to prove the shrink-ability of the WDR pixel concept, the pixel pitch is reduced from 7.5 μm (in the previous work) to 5.6 μm in this work. Fig.2 shows the chip micrograph of the 1/4 inch VGA 5.6μm-pixel-pitch WDR-CMOS image sensor fabricated through a 0.18μm 2P3M process.

Operation Temperature Range Extension

Very Low Dark Current Front End of Line

Very-low-dark-current (VLDC) approaches are implemented to the front-end of line (FEOL) of the 0.18μm 2P3M process. These include: the reduced plasma etching damage at the transfer gate formation, the modified channel doping profile under the transfer gate, the pinned photodiode with smaller electrical field and furnace temperature process for re-crystallization. Fig.3 compares the dark current of the VLDC FEOL and the conventional flow. Dark current is reduced to 175 e^-/sec-pixel at 85˚C (25 e^-/sec-pixel at 60˚C) by the use of the VLDC FEOL. The activation energy of the dark current for VLDC FEOL is about 0.62eV and should be the generation dominated.

Thermal Resistant On-chip Micro Lens & Color Filter

The chemical aspects of the thermal decomposition of the OCML/OCCF material (phenol resin) have been analyzed with a Fourier transform infrared spectrophotometer (FTIR) as shown in Fig.4. Fig.5 shows the CO_2 (2362 cm^{-1}) absorbance as the result of thermal decomposition in the varied O_2 concentration from 0% to 1% in O_2/N_2 mixed gases. It is also found that CO_2 over 100 ppb is detected at 222˚C for 1 % O_2/N_2, 237˚C for 1000 ppm O_2/N_2 and 282˚C for 100 ppm. No CO_2 over 100 ppb is found under 300˚C for the case of <10 ppm O_2/N_2. By preventing the OCML/OCCF from oxidation, the thermal decomposition is suppressed. In order to prevent the oxidative decomposition of the OCML/OCCF, two approaches, an inorganic (SiO_2 /SiN) cap onto the OCML and a metal hermetic seal package with low residual oxygen concentration in N_2 gas ambient are adopted. Fig.6 shows the schematic of the inorganic cap

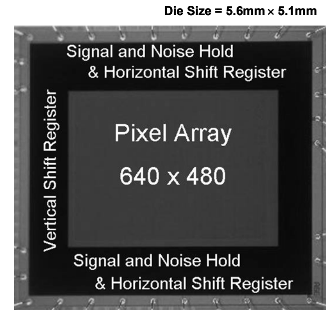


Fig.2 Chip micrograph of the 1/4 inch VGA WDR CMOS image sensor with 5.6 μm pixel pitch.

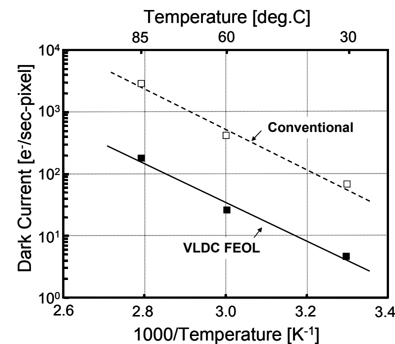


Fig.3 Dark current comparison between the VLDC FEOL and the conventional flows.

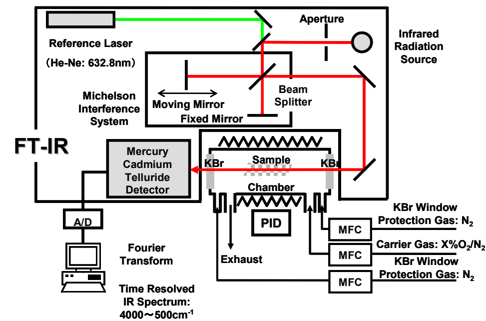


Fig.4 Schematic drawing of Fourier transform infrared spectrophotometer (FTIR).

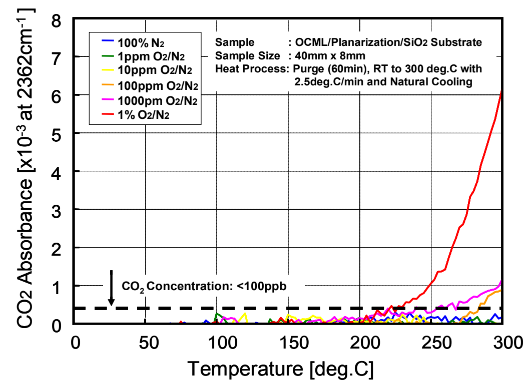


Fig.5 CO_2 absorbance measured by Fourier transform infrared spectrophotometer as the result of the thermal decomposition of the micro lens in O_2 (=0 to 1%)/N_2 ambient.

onto the OCML. In addition to the passivation effect, optical performance is taken into account to select the inorganic cap. The optical simulation results in improved quantum efficiency for the SiO_2 /SiN cap on the OCML, as shown in Fig.7. Sensor chips with and without the inorganic cap onto the OCML were assembled into a conventional package or the metal hermetic seal package, as shown in Fig.8. They were exposed to a 150˚C/ 500 hours thermal stress test in the air. Fig.9 shows the sensitivities of R/G/B pixels under a certain illumination, tested every 100 hours. The sensor chip under the thermal stress with the conventional package shows a drastic drop of sensitivity, especially in B/G pixels. However, the other two samples (the inorganic cap onto the OCML and the metal hermetic-sealed package) show no significant degradation of the spectral response in any of R/G/B pixels. The surface of the OCML is found to be protected from oxidative decomposition in both cases.

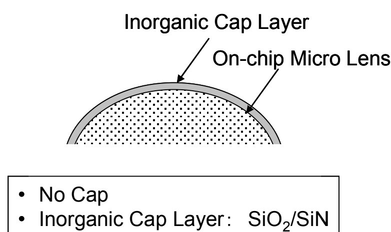


Fig.6 Inorganic cap layer onto on-chip micro lens.

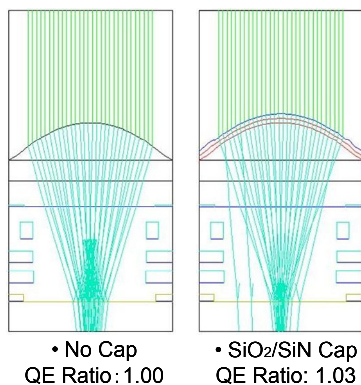


Fig.7 Optical performance of the inorganic cap layer to on-chip micro lens.

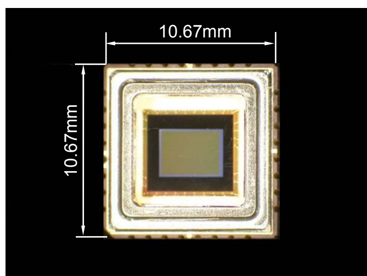


Fig.8 The WDR CMOS image sensor with the metal hermetic seal package.

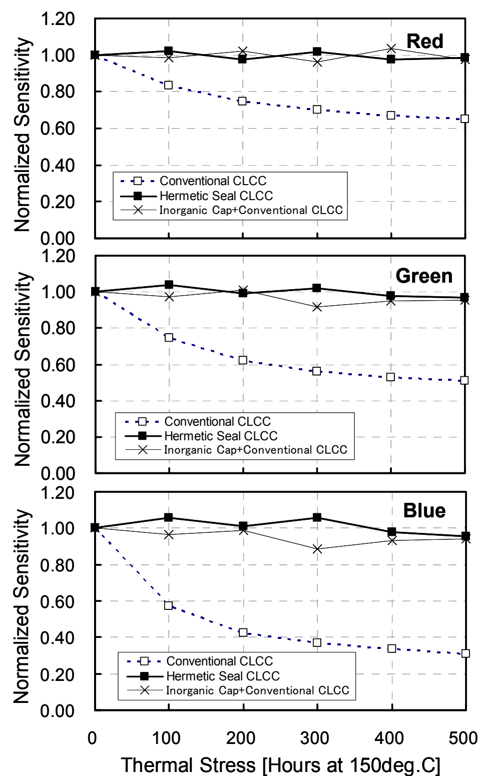


Fig.9 R, G and B sensitivities of the WDR CMOS image sensors with the hermetic seal package and the conventional package after the thermal stress test.

Image Sensing Performance

Fig.10 shows image samples captured by the temperature-resistant WDR CMOS image sensor with the metal hermetic seal package at 30, 60 and 85˚C before and after the thermal stress (150˚C / 500 hours). The WDR signal selecting either the non-saturated signal (S1) or the saturated overflow signal (S2) by pixel is reproduced and displayed as 8 bit resolution by applying the gamma correction ($\gamma \cong 0.15$) to 16 bit resolution data. The random noise is found to slightly increase as the temperature goes up, however no significant degradation of the image quality is observed even at 85˚C. Table 1 summarizes the image sensing performance of the temperature-resistant WDR CMOS image sensor with the metal hermetic seal package after 150˚C /500hours thermal stress test. The noise is 0.19 mV-rms, the effective saturation voltage of S2 is 8.8 V and the dynamic range is extended to 93 dB. The use of the metal hermetic package prevents the oxidative decomposition of the OCML/OCCF and leads to being thermally stable even after the thermal stress test.

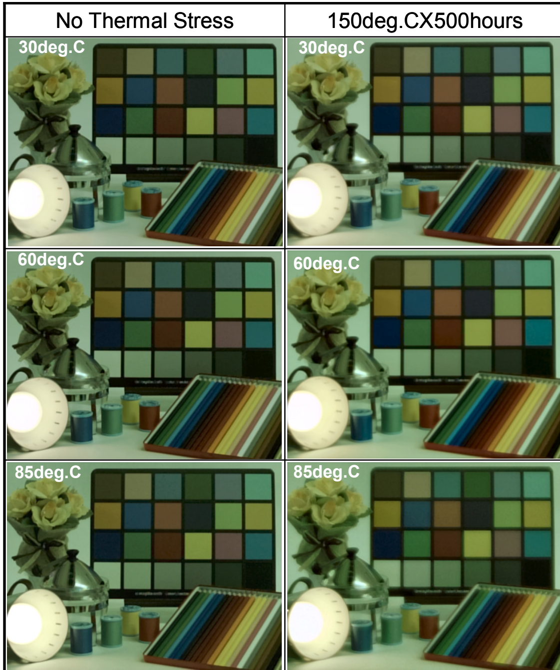


Fig.10 Image samples captured by no thermal stressed and 150˚C /500hours thermal stressed WDR CMOS image sensors with metal hermetic seal packages, at 30, 60 and 85˚C.

Table 1 Image sensing performance of the temperature-resistant WDR CMOS image sensor with the metal hermetic seal package (: after 150˚C /500hours).

Process technology	0.18μm 2P3M CMOS
Optical format	1/4 inch
Pixel size	5.6 x 5.6 μm^2
Number of effective pixels	640 x 480
Supply voltage	5 V
Frame rate	30 fps
Random Noise	0.19 mV_{rms}
Saturation of S1	700 mV
Saturation of S2	1100 mV
Effective saturation of S2 (saturation of S2 x 8)	8.8 V
Dynamic range	93 dB

Conclusion

The 1/4 inch VGA (5.6 μm pixel pitch) wide dynamic range (WDR) CMOS image sensor with resistance to high temperatures has been developed. The use of the very low dark current front-end of line (VLDC FEOL), the inorganic cap to the on-chip micro lens & color filter (OCML/OCCF) and the metal hermetic seal package enables the operation temperatures up to 85˚C. The VLDC approaches which include: reduced plasma etching damage at the transfer gate formation, modified channel doping profile under the transfer gate, pinned photodiode with smaller electrical field and furnace temperature process for re-crystallization achieves 175 e^-/sec-pixel of dark current at 85˚C (25 e^-/sec-pixel at 60˚C). The oxidative decomposition of the OCML/OCCF is completely suppressed, thus no significant degradation of the spectra response in any of R/G/B pixels is observed after the thermal stress test. The sample images captured by the WDR CMOS image sensor with and without the thermal stress test show no significant change in the image quality and keep a good noise performance up to 85 ˚C. The dynamic range is extended to 93 dB even after the thermal stress test.

References

[1] S. Sugawa, N. Akahane, S. Adachi, K. Mori, T. Ishiuchi and K. Mizobuchi, “A 100 dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor,” 2005 ISSCC Dig. Tech. Papers, 352-353 (2005).

[2] N. Akahane, S. Sugawa, S. Adachi, K. Mori, T. Ishiuchi and K. Mizobuchi, “A Sensitivity and Linearity Improvement of a 100-dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor,” IEEE J. Solid-State Circuits, 41(4), 851-858 (2006).

[3] N. Akahane, R. Ryuzaki, S. Adachi, K. Mizobuchi and S. Sugawa, “A 200dB Dynamic Range Iris-less CMOS Image Sensor with Lateral Overflow Integration Capacitor using Hybrid Voltage and Current Readout Operation,” 2006 ISSCC Dig. Tech. Papers, 300-301 (2006).

[4] S. Adachi, S. Sugawa, N. Akahane, K. Mori, T. Ishiuchi and K. Mizobuchi, “The Tolerance for FD Dark Current and PD Overflow Current Characteristics of Wide Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor,” Proc. 2005 IEEE Workshop on CCDs and AISs, 153-156 (2005).

[5] H. Takahashi, M. Kinoshita, K. Morita, T. Shirai, T. Sato, T. Kimura, H. Yuzurihara and S. Inoue, “A 3.9-um Pixel Pitch VGA Format 10-b Digital Output CMOS Image Sensor with 1.5 Transistor/Pixel,” IEEE Journal of Solid-State Circuits, 39(12), 2417-2425 (2004).

[6] B. Pain, T. Cunningham, B. Hancok, C. Wrigley and C. Sun, “Excess Noise and Dark Current Mechanisms in CMOS Imagers,” Proc. 2005 IEEE Workshop on CCDs and AISs, 145-148 (2005).

[7] K. Mizobuchi, S. Adachi, T. Yamashita, S. Okamura, H. Oshikubo, N. Akahane, S. Sugawa. “A Temperature Resistant Wide Dynamic Range CMOS Image Sensor,” Proc. 2007 Electronic Imaging Science and Technology, Paper No.2501-24, to be published.

A 121.8dB Dynamic Range CMOS Image Sensor using Pixel-Variation-Free Midpoint Potential Drive and Overlapping Multiple Exposures

Yusuke Oike, Atsushi Toda, Tadayuki Taura, Akihiko Kato,
Hiroki Sato, Masanori Kasai and Tadakuni Narabu

Sony Corporation
4–14–1 Asahi-cho, Atsugi, Kanagawa, 243-0014 Japan
Phone: +81–46–202–7953, Fax: +81–46–230–6170
E-mail: Yusuke.Oike@jp.sony.com

Abstract

This paper presents a wide dynamic range CMOS image sensor using a pixel-variation-free midpoint potential drive with a double midpoint shutter. No degradation of the sensitivity is seen due to continuing charge integration. The double midpoint shutter suppresses the fixed pattern noise of short-exposure images and realizes high linearity throughout the full scale. We have developed a 2M pixel prototype using a 0.18 μm CMOS process with three 90 nm Cu layers. Wide dynamic range operation up to 121.8 dB has been successfully demonstrated.

Introduction

Dynamic range is a key performance specification of an image sensor and there have been various approaches to extending it [1]–[8]. However, these are not preferable for color images due to nonlinearity [1]–[3] or not applicable for small pixel structures because of their complex pixel circuits [3]–[5]. Multi-sampling is a well-known approach to linear dynamic range extension. In recent years, high-speed CMOS image sensors have been developed [6, 9] which can realize a multi-sampling wide dynamic range with high pixel resolutions. On the other hand, the conventional technique of multiple exposures decreases the sensitivity because of the split and divided exposure terms. That is, the minimum required illumination increases in exchange for dynamic range.

This paper presents a wide dynamic range CMOS image sensor using a pixel-variation-free midpoint potential drive with a double midpoint shutter. It provides multiple images of several short exposures in addition to an image at full exposure by continuing charge integration. There is no degradation of the sensitivity in the wide dynamic range operation unlike the well-known multiple-exposure technique such as [6]. This technique concurrently suppresses the fixed pattern noise in short-exposure images resulting from inter-pixel variations of device characteristics. Furthermore the double midpoint shutter achieves high linearity throughout the full range, which is its major advantage over the conventional techniques using midpoint drives [7, 8].

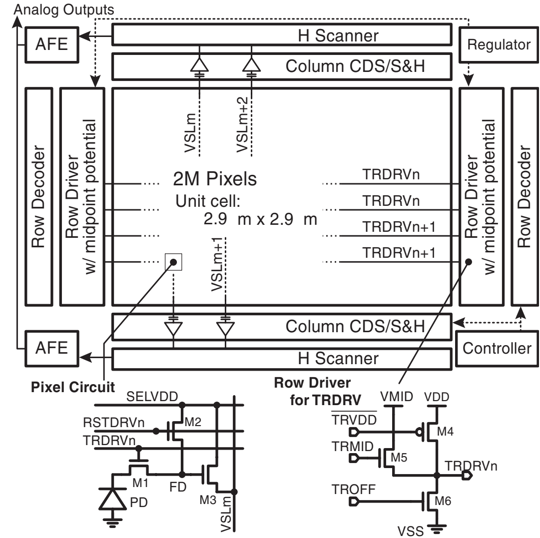


Fig. 1 Block diagram and simplified schematics.

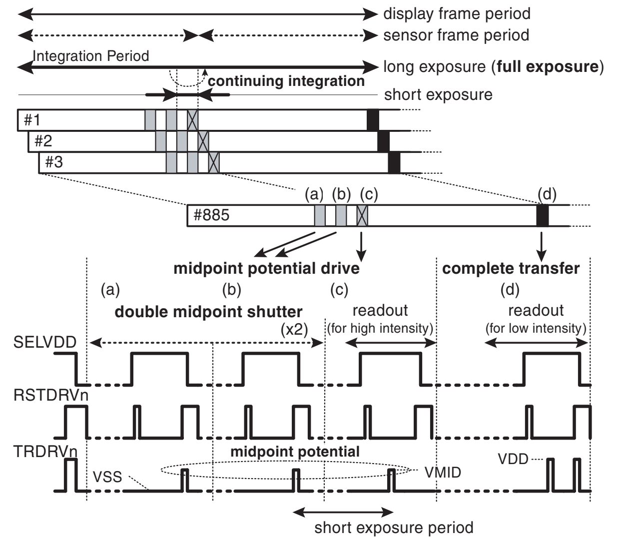


Fig. 2 Timing diagram.

Wide Dynamic Range Operation

Figure 1 shows a block diagram and simplified schematics illustrating our wide dynamic range CMOS image sensor using a pixel-variation-free midpoint potential drive. It consists of a pixel array, row decoders and drivers with a midpoint potential driver, column CDS circuits with a sample and hold (S&H) function, and horizontal scanners. As peripherals, the sensor has a controller, a regulator to generate the midpoint voltage, and analog front ends (AFE). The pixel circuit has three transistors as described in [10]. The cost of the additional circuit, for the wide dynamic range operation, is only that of a row driver extension and a regulator for the midpoint voltage supply. Note that the present technique is also applicable to a small pixel structure such as [11].

Figure 2 illustrates the timing diagram of the overlapping multiple exposures using the midpoint potential drive. Multiple sensor frames are assigned to a display frame period, then the midpoint voltage of $VMID$ is repeatedly supplied to the charge transfer gate of $TRDRV_n$ during the full charge integration of the display frame period. The first two midpoint drives are used

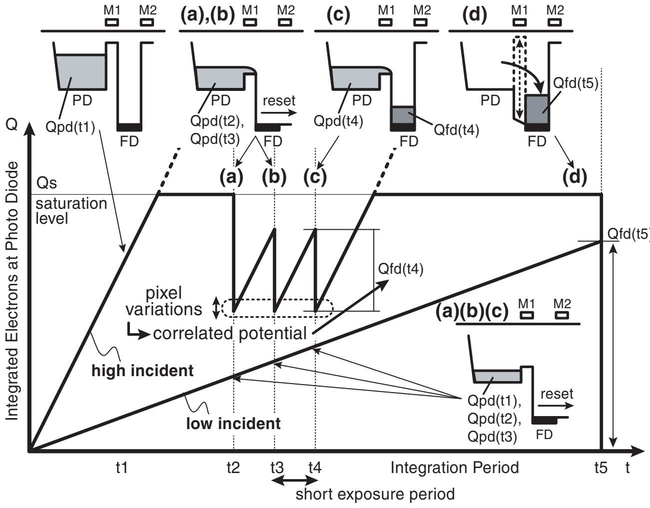


Fig. 3 Potential diagram of overlapping multiple exposures.

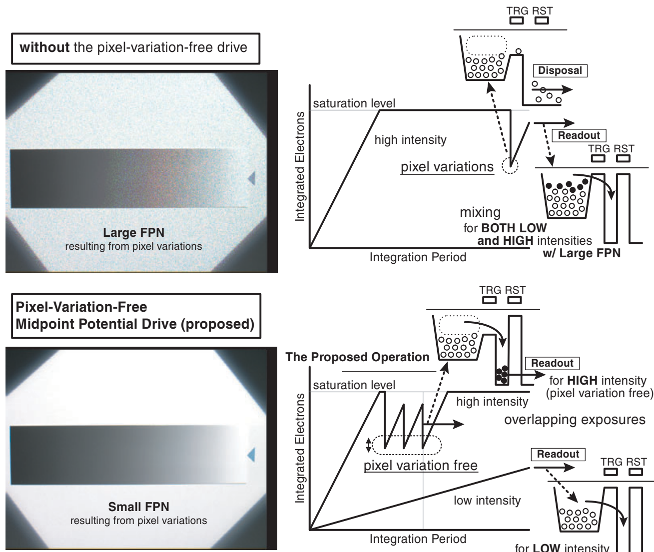


Fig. 4 Impact of pixel variations.

to make a double midpoint shutter, which sets the short exposure time and suppresses the FPN resulting from variations in device characteristics and supply voltages. The double midpoint shutter is provided from the relative timings (a) and (b) in Fig. 2. The last midpoint drive provides the image from the short exposure at the timing of (c). Finally, the complete charge transfer provides the image from the full exposure at the timing of (d) since the midpoint potential drives then allow continuation with charge integration for the low-intensity incident light.

Figure 3 is the potential diagram of overlapping multiple exposures. At a pixel with low-intensity incident light, the charge integration continues without a charge transfer by the midpoint potential drives. On the other hand, a partial charge transfer comes via the midpoint potential drives when the pixel receives high-intensity incident light which finally saturates it within the full integration time. The double midpoint shutter guarantees correlation in the potential between $Q_{pd}(t3)$ and $Q_{pd}(t4)$. Therefore the transferred charge of $Q_{fd}(t4)$ is free from pixel variations such as those caused by the threshold voltage of the transfer gates, the uneven distribution of impurities, the supplied midpoint voltage level, and the pulse settling time of $TRDRV_n$ as shown in Fig. 4.

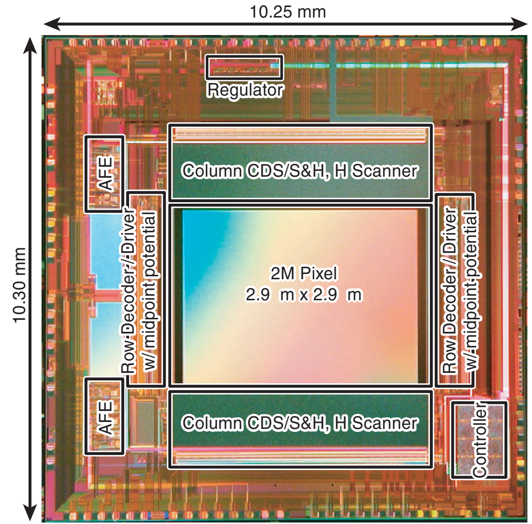


Fig. 5 Chip microphotograph.

Table 1 Chip Characteristics.

Process	0.18 μm CMOS + 90 nm 3 Cu layers
Die size	10,250 μm (H) $\times$ 10,300 μm (V)
Supply voltage	3.3 V / 1.5 V
Num. effective pixels	2 M pixels
Pixel size	2.9 μm $\times$ 2.9 μm
Max. frame rate	60 frames/s
RMS random noise	6.5 e-$_{rms}$ at 60 frames/s at dark level
RMS fixed pattern noise	2.0 e-$_{rms}$ at 60 frames/s at dark level
Conversion gain	88 μV/e-
Dynamic range	62.8 dB (normal operation)
Max. dynamic range	121.8 dB at 15 fps display rate

At the timing of (a) and (b) in Fig. 3, the transferred charges are reset without a readout operation. Then, the transferred charge of $Q_{fd}(t4)$ is read out as an image of the short exposure at the timing of (c). The integration period between (b) and (c) defines the short exposure time. The initial potential at (b), which is a condition just before the partial charge transfer at the starting point of the short exposure, needs to be correlated with the initial potential at (c) in order to get the exact charge integrated during the short exposure time. Therefore the first shutter is provided at the timing of (a) which is previous to the starting point of short exposure, and the time interval between (a) and (b) is the same period of the short exposure time. The double midpoint shutter makes the initial potential at (b) correlated to the initial potential at (c) as shown in Fig. 3. It achieves two advantages over conventional techniques using a midpoint drive [7, 8]. One is higher linearity throughout the full range. The linearity is not affected by variations of the midpoint voltage, since the offset is canceled due to the potential correlation. The other is a wider dynamic range because our technique is capable of cascading dynamic range extensions owing to the higher linearity and the offset canceling. Finally, the transferred charge of $Q_{fd}(t5)$ is read out as an image of the full exposure at the timing of (d).

Multiple sequences of the midpoint drives are iteratively applicable with arbitrary exposure times during the full exposure period. The overlapping multiple exposures can provide several images with different sensitivities in addition to that of the maximum sensitivity.

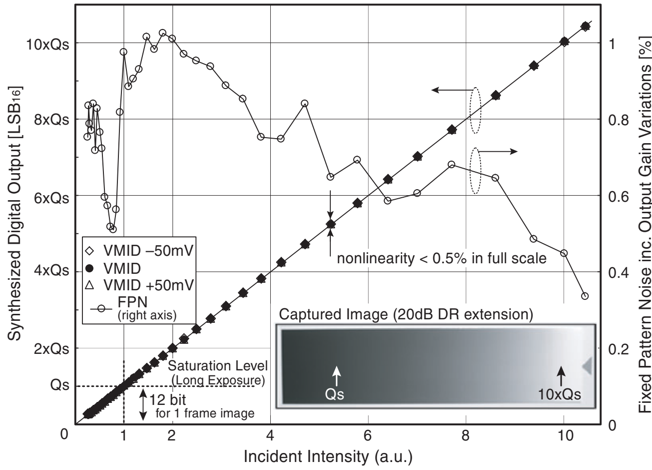


Fig. 6 Linearity and fixed pattern noise.

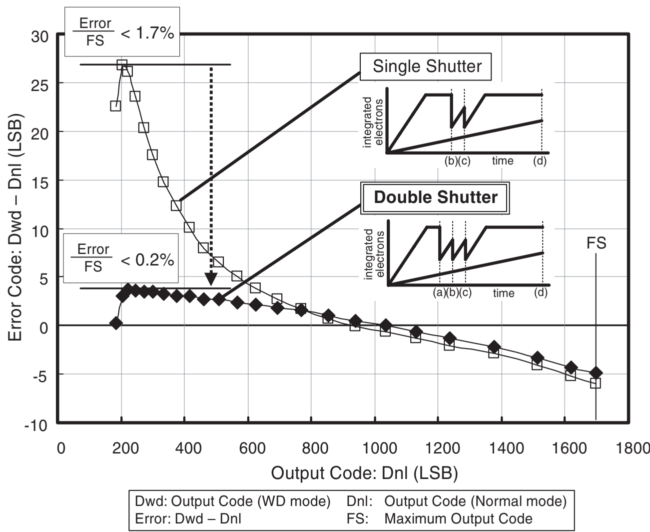


Fig. 7 Error suppression by the double midpoint shutter.

Chip Implementation

We designed and fabricated a 2M pixel CMOS image sensor, shown in Fig. 5, using a 0.18 μm CMOS process with three 90 nm Cu layers. The die size was $10{,}250 \times 10{,}300\,\mu\text{m}^2$. The supply voltages were 3.3 V for analog parts and 1.5 V for digital parts. The pixel size was 2.9 μm × 2.9 μm. The random noise (RN) was 6.5 e-$_{rms}$ and the FPN was 2.0 e-$_{rms}$ at the dark level. The innate dynamic range was 62.8 dB. The chip characteristics are summarized in Table 1.

Measurement Results

Figure 6 shows the measured results for the linearity and the fixed pattern noise in a 20 dB dynamic range extension by 2 frames. The midpoint voltages were set to $VIMD$, $VMID - 50$ mV, and $VMID + 50$ mV, respectively, to verify the robustness of device with the pixel-variation-free midpoint potential drive. Here, the error is defined as $|D_{wd} - D_{nl}|/FS$, where D_{wd} is the output data of the wide dynamic range operation, D_{nl} is that of a normal short-exposure operation, and FS is the full code. An error of less than 0.5 % of the full scale was found and this value was not affected by the variations of the midpoint voltage; as expected as the connecting point is provided by the sum of the long- and short-exposure output codes and any offset in the short-exposure output will be reduced due to the potential correlation.

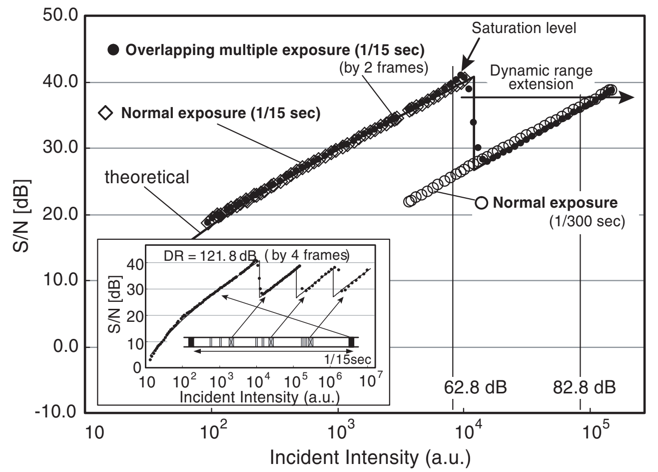


Fig. 8 Signal-to-noise ratio.

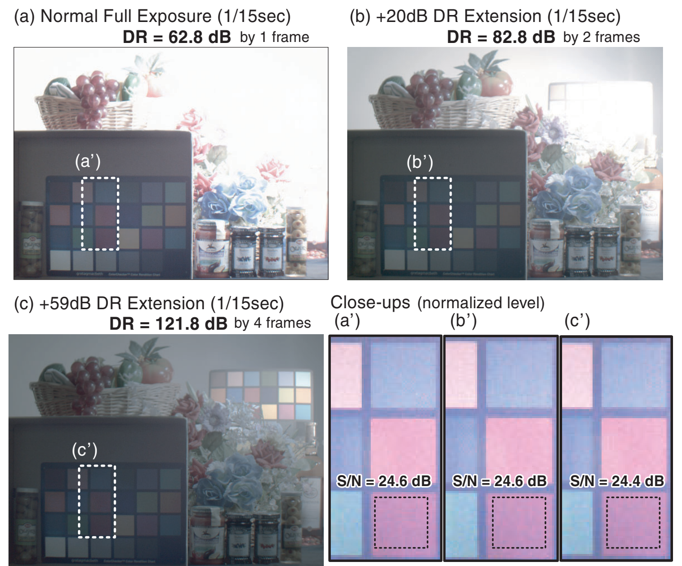


Fig. 9 Reproduced images.

The FPN at the dark level was 2.0 e-$_{rms}$, just as it was in the innate specification. The FPN including output gain variations was less than 1.1 % due to the double midpoint shutter. The random noise at the dark level was 6.5 e-$_{rms}$ as the same as the innate device. A captured image with 20 dB extension is inserted into Fig. 6. There is no obvious solarization or posterization.

The double midpoint shutter effectively suppresses the offset error as shown in Fig. 7. Here the error code of $|D_{wd} - D_{nl}|$ is plotted for the case of 18 dB dynamic range extension. In a single midpoint shutter operation, where the first midpoint shutter is excluded, the offset error was found to be 1.7 % at the boundary of dynamic range extension. This offset error at the boundary leads to a color shift after the white balance processing. The double midpoint shutter reduces this offset error to 0.2 %. The high linearity provides a good gradation sequence without any color shift.

The measured signal-to-noise ratio is plotted in Fig. 8. The S/N of overlapping multiple exposures is in excellent agreement with a normal exposure using the full integration time in the innate dynamic range of 62.8 dB. The S/N follows that of a normal short exposure in the extended dynamic range. In this case, the interval of midpoint potential drives was 1/300 sec, and the S/N was at the level of a 1/300-sec normal short expo-

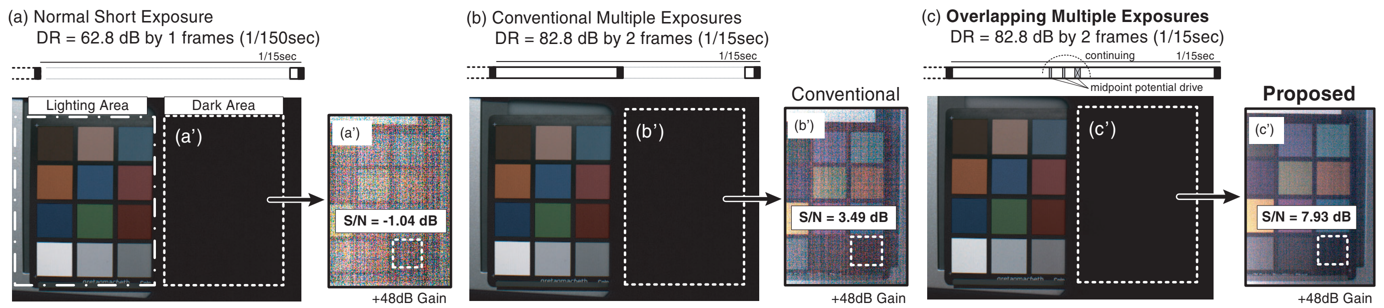


Fig. 10 Comparison with the conventional multiple exposures.

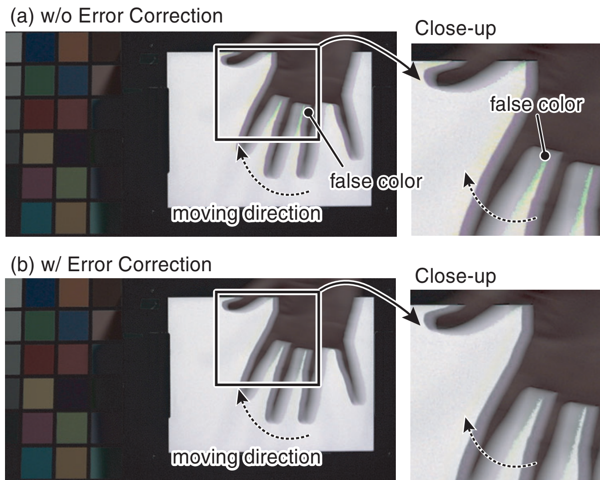


Fig. 11 A sample image of a moving target object.

sure. The present technique is capable of cascading dynamic range extensions according to the ratio of the sensor frame rate to the display frame rate. The prototype image sensor achieved a 121.8 dB dynamic range by 4 frames at a 15 fps display rate as shown by the inserted plot in Fig. 8.

Figure 9 shows reproduced color images. A normal exposure of 1/15 sec provided the maximum sensitivity at a display rate of 15 fps. Figure 9 (a) is, however, saturated because the dynamic range of 62.8 dB was not enough for the high contrast scene. Figure 9 (a') is a close-up. Figure 9 (b) and (c) are reproduced images of 82.8 dB by 2 frames and 121.8 dB by 4 frames, respectively, using overlapping multiple exposures. The S/N in the dark region agrees with (a') as presented in the close-ups of (b') and (c'). Figure 10 shows a comparison with the conventional multiple exposure technique. The present technique achieved a 121.8 dB linear dynamic range without either sensitivity loss in a dark region or visible FPN in a bright region. Thus, we can say that this highly linear and wide dynamic range operation is more suitable for color and high-pixel-resolution image sensing than conventional techniques.

We have also developed a signal processing algorithm to reduce false color for a moving target object. In the wide dynamic range technique, a reproduced image is a composite image using several integration periods. Therefore, several moving target objects against a static background would be captured over different integration periods for a high contrast scene. Figure 11 is a sample image of such a moving target object. Some false colors were seen to at the boundaries of the moving object. Our false color reduction algorithm successfully detects the error region and effectively suppresses the false color as shown in Fig. 11.

Conclusions

We have presented a 121.8 dB dynamic range CMOS image sensor using pixel-variation-free midpoint potential drives and overlapping multiple exposures. The pixel-variation-free midpoint potential drive provides multiple images of several short exposures, in addition to an image of the full exposure by continuing charge integration. There is no sensitivity loss, even in wide dynamic range operation, since this technique makes efficient use of the full exposure time. Furthermore, the double midpoint shutter concurrently suppresses the fixed pattern noise, resulting from inter-pixel variations of device characteristics, of short-exposure images. Small pixel configurations are no barrier for the wide dynamic range operation and we believe that the present technique is applicable to various fields of image sensing.

References

[1] G. G. Storm *et al.*, "Combined Liner-Logarithmic CMOS Image Sensor," *IEEE ISSCC Dig. Tech. Papers*, pp.112–113, Feb. 2004.

[2] K. Hara *et al.*, "A Linear-Logarithmic CMOS Sensor with Offset Calibration Using an Injected Charge Signal," *IEEE ISSCC Dig. Tech. Papers*, pp.354–355, Feb. 2005.

[3] N. Akahane *et al.*, "A 200dB Dynamic Range Iris-less CMOS Image Sensor with Lateral Overflow Integration Capacitor using Hybrid Voltage and Current Readout Operation," *IEEE ISSCC Dig. Tech. Papers*, pp.300–301, Feb. 2006.

[4] D. Yang *et al.*, "A 640 × 512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating-Point Pixel-Level ADC," *IEEE ISSCC Dig. Tech. Papers*, pp.308–309, Feb. 1999.

[5] S. Sugawa *et al.*, "A 100dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor," *IEEE ISSCC Dig. Tech. Papers*, pp.352–352, Feb. 2005.

[6] M. Mase *et al.*, "A 19.5b Dynamic Range CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters," *IEEE ISSCC Dig. Tech. Papers*, pp.352–352, Feb. 2005.

[7] S. Decker *et al.*, "A 256×256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output," *IEEE J. Solid-State Circuits*, vol.33, no.12, pp.2081–2091, Dec. 1998.

[8] Y. Egawa *et al.*, "A 1/2.5 inch 5.2Mpixel, 96dB Dynamic Range CMOS Image Sensor with Fixed Pattern Noise Free, Double Exposure Time Read-Out Operation," *in Proc. IEEE Asian Solid-State Circuits Conf.*, pp.135–138, Nov. 2006.

[9] Y. Nitta *et al.*, "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor," *IEEE ISSCC Dig. Tech. Papers*, pp.500–501, Feb. 2006.

[10] K. Mabuchi *et al.*, "CMOS Image Sensor Using a Floating Diffusion Driving Buried Photodiode," *IEEE ISSCC Dig. Tech. Papers*, pp.112–113, Feb. 2004.

[11] M. Mori *et al.*, "A 1/4in 2M Pixel CMOS Image Sensor with 1.75 Transistor/Pixel," *IEEE ISSCC Dig. Tech. Papers*, pp.110–111, Feb. 2004.

A High Dynamic Range digital LinLog CMOS image sensor architecture based on Event Readout of pixels and suitable for low voltage operation

Alexandre Guilvard[1,2], Pierre Magnan[1],Josep Segura[2], Philippe Martin-Gonthier[1]
[1]Supaero, Toulouse, France;
[2]STMicroelectronics, Crolles, France

[1]A. Guilvard, P. Magnan, P. Martin-Gonthier: E-mail : {guilvard, magnan, martingo}@supaero.fr Tel : +33.5.62.17.80.79
[2]J. Segura : E-mail : josep.segura@st.com Tel : +33.4.76.92.56.94

Several approaches have been developed to extend the dynamic range of image sensor [1] in order to keep all the information content of natural scenes covering a very broad range of illumination. Digital CMOS image sensor are especially well suited to wide dynamic range imaging by implementing dual sampling [2], multiple exposure methods using either column [3] or in pixel ADC [4][5][6], or Address Event Representation [7].

A new architecture of digital high dynamic range CMOS image sensor, suitable for low voltage operation, has been developed that implements a built-in dynamic compression function targeted to LinLog behavior, by combining an event based readout of pixels, the use of multiple integrations per frame (fig.1) and the coding of pixel values using the mantissa-exponent principle [4] [8], to achieve the dynamic range extension.

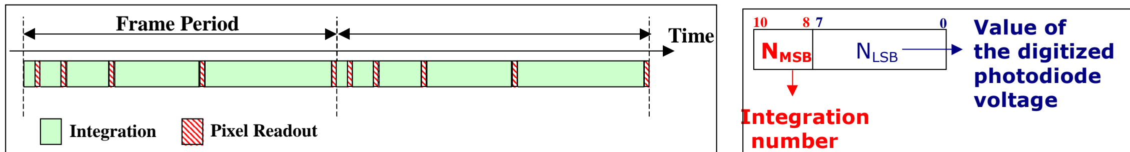


Fig. 1: Multiple integrations per Frame and output data coding

This architecture is depicted in Fig 2: each pixel implements an ADC based on an autozero comparator and a global voltage ramp (Vramp) generated by a unique 10 bits DAC with a roughly 1,2 mV resolution. In order to have a constant photodiode voltage during digitizing, a snapshot feature has been added to the pixel with a light shielded memory node Csn storing the photodiode voltage that is compared to the ramp value.

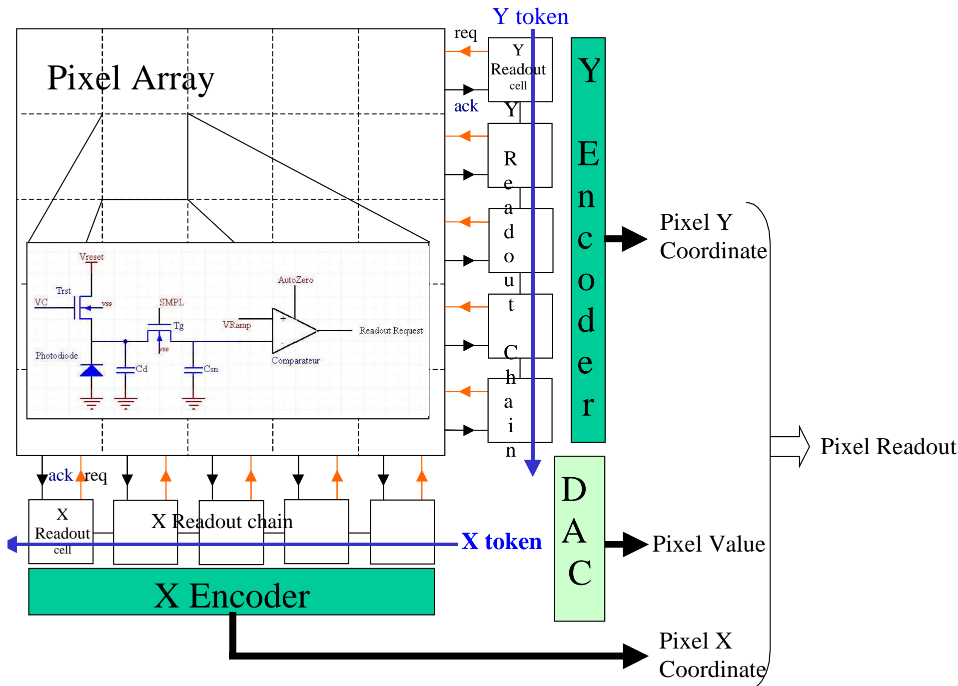


Fig. 2: Pixel and sensor architecture.

The sensor makes use of an innovative and fast event based readout chain to avoid the readout of the entire pixel array after each integration, and so allows a direct capture of the final image from the different exposure times without the need of external reconstruction. After each integration, the ADC ramp rises and for each pixel, when its voltage value is larger than the Csn voltage, the comparator flips, and a readout request is sent by the pixel (reqY). Once detected and processed by the readout chains, the read pixel is attributed the digital input value of the DAC together with its address coordinates. In order to read the array with no pixel loss nor possible conflicts, the readout requests have been splitted into row (Y) and column (X) requests. Two readout chains, one per axis, have been created to allow the circulation of an asynchronous token at very high speed (typically 3 GHz in advanced process, based on the gate propagation delay) as depicted in fig. 3 for the Y axis. For each step of the voltage ramp (Vramp), a scan of all the rows is performed by sending a token on the Y axis. Upon a pixel request, the Y flag is stopped at this line, an acknowledge signal is sent on the row (ackY) by the corresponding readout cell and at the receipt of the acknowledge signal, an in-pixel logic block emits the readout request on the column (reqX). As a requesting line has been detected, the X flag is started to scan the column. The X flag is stopped on the requesting column and an acknowledge signal is send (ackX). At the receipt of the two acknowledge signals, the pixel is attributed the DAC digital input value and is placed in placed in standby mode, the comparator output being disconnected from readout chain (this requires logic blocs in the pixel) until the capture of the next frame. Therefore, each pixel is read only once during a given frame. and their data is externally memorized. Thanks to the request-acknowledge readout principle, no conflicts or loss can occur.

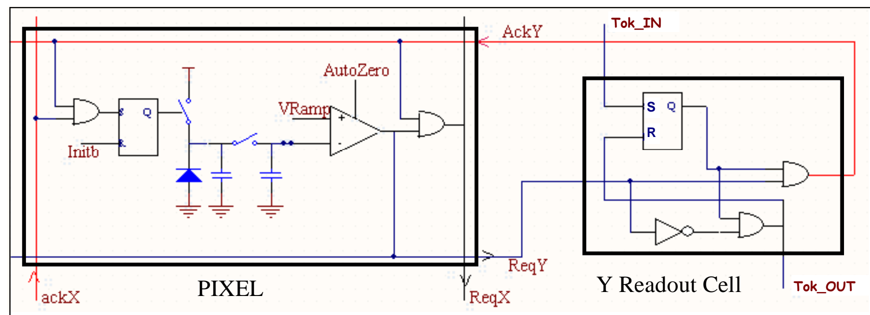


Fig. 3 Pixel and readout cell interaction (simplified view)

Doing so, each possible illuminance level of the scene is processed in a unique integration. The integrations are performed from the shortest to the longest, and only a part of the photodiode voltage swing is be explored by the DAC at each integration [Vrefmin, Vrefmax](Fig 4).

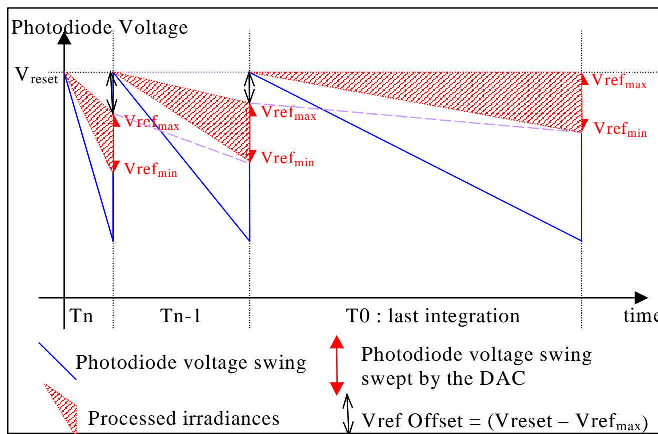


Fig. 4 Distribution of the scene dynamic range to the different integrations

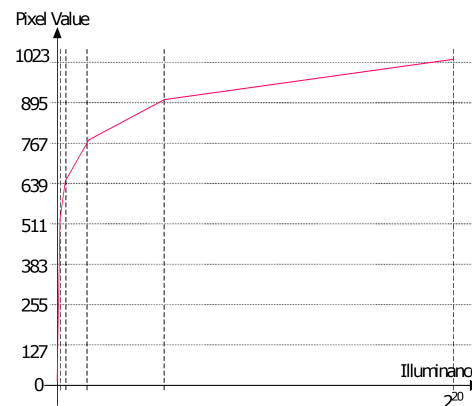
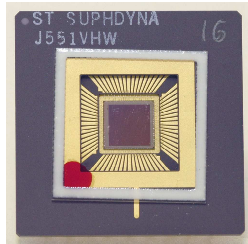


Fig. 5: Segment approximation of LinLog dynamic compession curve obtained with 8 integrations per frame with Tint Ratio = 4

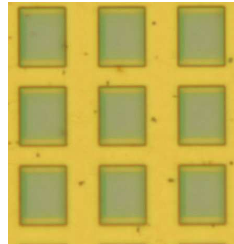
The compression function is build from segments whose slope ratios are defined by the integration times ratios. As an exemple, in fig. 5, 8 integrations with a constant ratio equal to 4 are used to produce a Lin-Log compression characteristics. Ratios between the slope of the segments building the compression function are defined

by the ratios between the integration times This architecture is entirely digital and so well suited for the low voltage supply of advanced processes.

The previous principles have been implemented in a validation prototype (fig.6) - 511x511 pixels array- realized in the STMicroelectronics 0.13µm CMOS standard (non imaging) technology with simple oxide 1.2 V transistors; table 1 provides the key features. This sensor operates at video rate and the pixel containing 42 transistors and an Nwell photodiode.



the sensor



view of the pixels

Fig. 6: 511x511 pixel array prototype implemented in STMicroelectronics 0.13µm digital CMOS technology.

Sensor Prototype target specifications	
Resolution	511 x 511
Pixel size	10 µm x 10 µm
Number of transistor per pixel	42
Fill Factor	25 %
Output resolution	10 bits
DAC step	1.17mV
Clock Frequency	50 MHz
Conversion gain @pixel level	40 µV/e
Power supply	1,2 V
Supported dynamic range	>100dB

Table 1: Sensor Prototype target specifications

The event-driven readout principle is completely functional and no error in the readout process occur but due to unexpected leakage in the non optimized technology used, still in investigation at the time of paper writing, the linear voltage swing of the pixel is limited to 300mV as shown in fig.7.

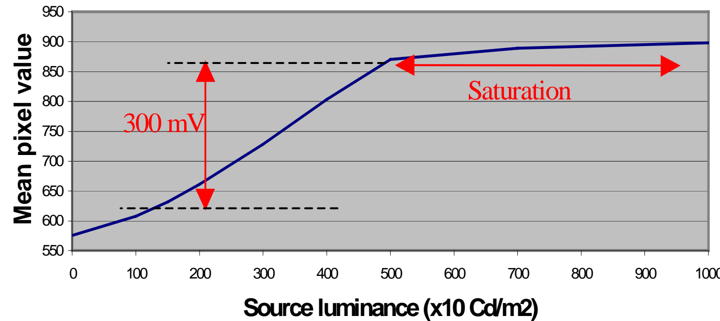


Fig.7: Transfer characteristic in linear mode (@Tint=5ms) demonstrating a limited linear voltage swing of 300mV

Despite this limitation in the swing, the DR extension principle still works but with less versatility in the integration time ratio and so in the produced characteristics. Fig. 8 shows the Transfer Characteristic achieved with a Tint Ratio setting of 3 and demonstrates a significant DR extension (more than 30 dB).

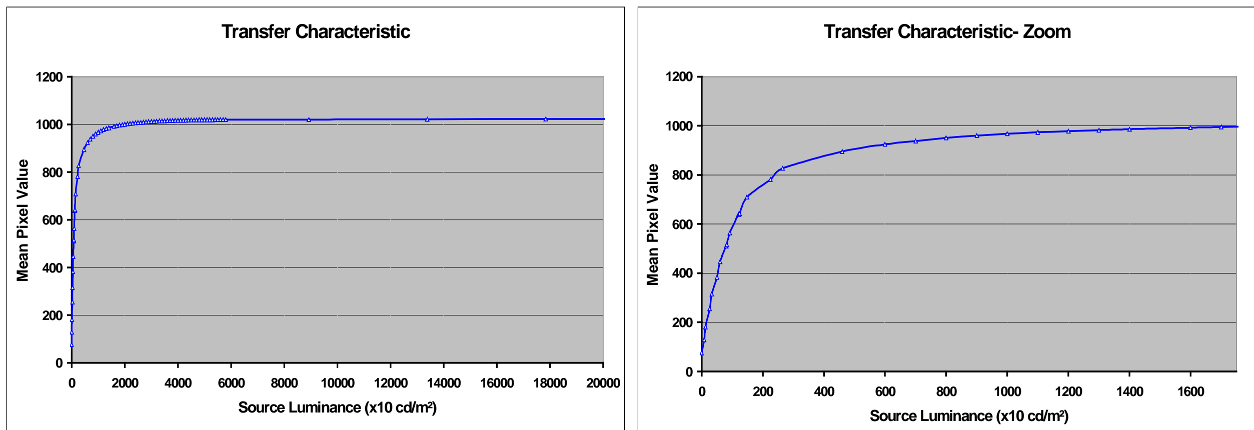


Fig. 8: Measured Transfer characteristic for Tint Ratio setting= 3 (from 3 µs to 6.5 ms).The source-sensor distance is more than 3 times shortest than for the linear characteristic measurement

Images of HDR scenes have been captured with this sensor (Fig. 9) and the 4 images (splitted 256 gray scale level) demonstrate that all the information of the HDR image is available. This HDR image is rebuilt in memory with no need of post processing.

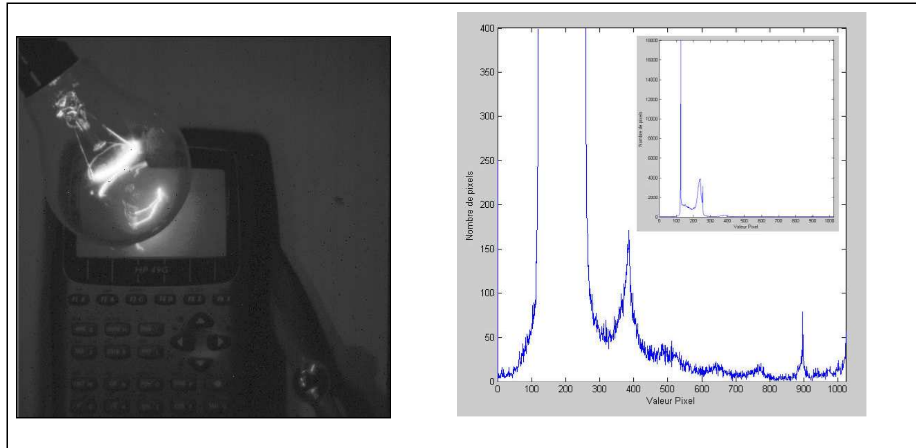
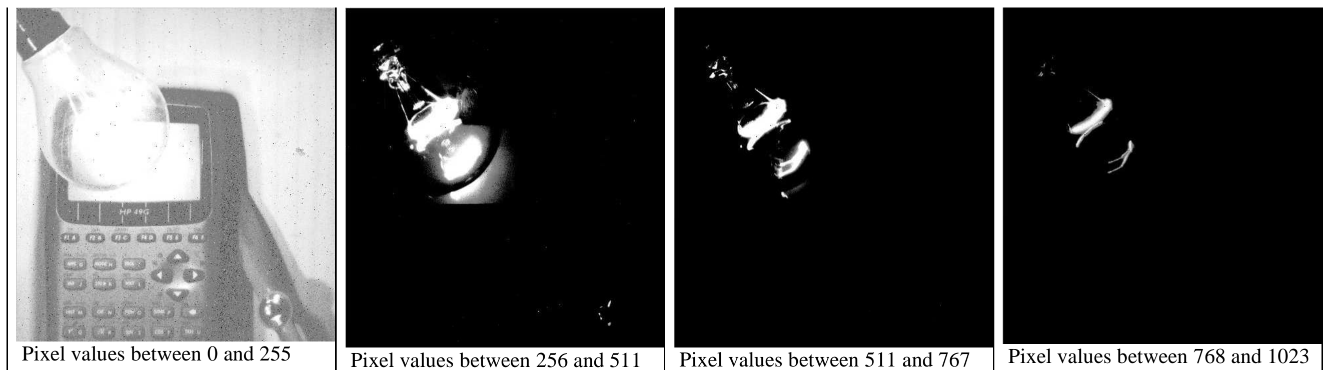


Fig. 9: Image of an HDR scene and the corresponding histogram



The temporal noise have been measured as 7 mV with a significant contribution of KTC noise and comparator noise, the FPN as 6mV and the power consumption as 60mW at video rate.

Efforts are still on-going to improve the behavior of the device. The use of an imaging process would help significantly on this way but the key principles have been demonstrated especially the event based readout principle that allow a unique readout of each pixel along the multiple integrations and the dynamic range extension scheme.

References :

[1] O. Yadid-Pecht, “Wide dynamic range sensors,” Opt. Eng., vol. 38, no.10, pp. 1650–1660, Oct. 1999.
[2] O. Yadid-Pecht and E. Fossum, “ Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling ”, IEEE Trans. Electron Devices, vol. 44, pp. 1721–1724, Oct. 1997.
[3] M. Mase S. Kawahito, M. Sasaki,Y. Wakamori, "A 19.5b Dynamic Range CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters", ISSCC Dig Tech Papers 2005, pp. 350-351.
[4] D. X. D. Yang, A. El Gamal, B. Fowler, H. Tian, “A 640_512 CMOS image sensor with ultra wide dynamic range floating-point pixel level ADC,” IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 1999, pp. 308–309.
[5] L. G. McIlrath, “A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion,” IEEE J. Solid-State Circuits, vol. 36, pp. 846–853, May 2001
[6] A. V. Harton and al, , "A High Dynamic Range CMOS Image Sensor with Pixel levl ADC and in-situ image enhancement", Proc SPIE-IST Electronic Imaging 2005, Vol 5677, pp 67-77
[7] E. Culurciello, R. Etienne-Cummings, and K. Boahen, “Arbitrated address event representation digital image sensor,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2001, pp. 92–93.
[8] O. Yadid-Pecht and A. Belenky, “Autoscaling CMOS APS with customized increase of dynamic range“, ISSCC Dig. Tech. Papers, Feb. 2001, pp. 100–101

Performance of solid-state image sensors in medical X-ray applications

Inge M. Peters

DALSA Professional Imaging, High Tech Campus 12a, 5656 AE Eindhoven, The Netherlands
Inge.Peters@DALSA.com - phone +31-40 274 39 57 – fax +31-40 – 274 40 90

Abstract

During the last decade the conventional film screen in medical X-ray equipment is being replaced by digital detectors. These digital detectors consist of an energy converter, x-ray to photons or x-ray to electric charge, a gain element and a read-out device, e.g. CCD or CMOS detector.
In this tutorial the focus will be on indirect X-ray detection using a phosphorous applied on a fiber optic plate coupled to a CCD or CMOS detector. The influence of each separate element on the final image quality will be discussed.

In medical X-ray imaging the detective quantum efficiency (DQE) is an important parameter for defining the image quality and system performance. It is a measure of how well a detector is able to extract information from a beam of radiation. For high doses – in the quantum-noise limited regime – the DQE is independent of dose, but at low doses the DQE starts to decrease and hence it is a good indicator of the system performance at low radiation levels. The method to measure DQE will be explained. The effect of the performance of a solid-state image sensor on the DQE will be presented. The main items to discuss are the noise, quantum efficiency, charge capacity, pixel size and the binning feature. The presentation will end with a summary of the strengths and weaknesses of solid-state image sensors for medical X-ray applications.

Highlight Scene FPN on Shared Pixels and a Reduction Technique

Takashi Watanabe, Katsuji Kimura, Masamitsu Taki, Kohji Horikawa, Mitsuru Homma,
Shoko Daikoku, Tetsuya Fujimoto, and Kiyotoshi Misawa
Imaging and Sensing Module Division, LSI Group, Sharp Corporation, Japan
Phone: +81-743-65-0860, Fax: +81-743-65-4847, E-mail:watanabe.takashi@sharp.co.jp

Abstract

Shared pixel technology is most common in recent small pixel CMOS image sensors. In the case of vertically shared pixels, it has been observed horizontal line FPN with the period of shared pixels when highlight scene is imaged and integration period is reduced to very short time by electronic shuttering. We present here the reason of the phenomena and the technique for reducing it. As the results, the FPN reduced to below background level.

Ⅰ. Introduction

Pixel sharing becomes most common technology as pixel size of CMOS image sensors is highly scaled down [1]. Recently, 4-pixel sharing such as 4x1 [2,3,4] and 2x2 [5,6,7] are widely used. In particularly 4x1 sharing, it has been observed horizontal line FPN with the period of shared pixels when highlight scene is imaged and integration period is reduced to very short time by electronic shuttering. Figure 1 shows an example of captured image.

We have analyzed the phenomena and attributed it to overflow mechanism from other pixels within shared pixels. To suppress this overflow mechanism, we introduced additional shutter operations before original shutter and after readout. Experimental results based on the suppressing method show that the overflow model is proved and the horizontal line FPN is clearly removed.

Ⅱ. Analysis

In 4x1 pixel sharing, pixel circuit is shown in Figure 2 and readout timing is shown in Figure 3. We consider the case that highlight scene is imaged and integration period is reduced to very short time around one horizontal line period (1H) by electronic shuttering. When first line of shared pixels is readout, only first readout photodiode (PD-1) is below saturation and others (PD-2,PD-3 and PD-4) are over saturation. Therefore, overflow current from three photodiodes are continuously injected to detection node (FD). In Figure 3, the overflow current accumulated in CDS period (Tcds) causes additional signal (Vfpn) on CDS output, which is the difference between reset output at Tr and signal output at Ts. Next, when second line of shared pixels is readout, first and second readout photodiodes (PD-1 and PD-2) are below saturation and others (PD-3 and PD-4) are over saturation, because PD-1 is just after the readout. Therefore, additional signal (Vfpn) of second line is smaller than that of first line. In the same way, additional signals of third and forth lines are smaller than that of first and second lines. As the results, horizontal line FPN with the period of shared pixels will appear. Figure 4 shows those phenomena schematically, where (A) is the case that shutter period is 1H and (B) is the case that the shutter period is 2H. When incident light is strong enough to saturate the photodiode below 3H period, overflow occurs soon after readout, which is shown as Δ2 in Figure 4. Figure 5 is a measured signal output along horizontal line numbers. Pixel size in this

case is 2.2um square. FPN indicated in Figure 4 is clearly observed.

The FPN value is proportional to light intensity Vs, time ratio Tcds/Th and shutter period, where Vs is the signal at 1H integration period and Th is a horizontal line period. At 1H-shutter operation, $Vfpn=2(Tcds/Th)(Vs)=2\Delta 1$. At 2H-shutter operation, $Vfpn=(Tcds/Th)(Vs)=\Delta 1$. To reduce the FPN, it is effective to reduce the CDS period (Tcds). But reduction of CDS period brings increase of readout band width, which causes increase of readout noise [8]. A certain CDS period should be maintained.

Ⅲ. FPN reduction method

To suppress this overflow mechanism, we introduced additional shutter operations before original shutter and after readout. Figure 6 shows timing diagram of the operation and expected effect. Before normal shutter operations (S), additional shutter operations (S') are added in all related lines. As the same manner, after normal readout operations (R), additional shutter operations (S') are added in all related lines. By introducing additional shutter operations, signal charges in photodiodes before shutter and after readout operations are removed and overflow is ceased. As the results, the FPN disappears.

Ⅳ. Results and discussions

Figure 7 shows captured image and Figure 8 shows measured signal pattern when the reduction method is applied. The FPN clearly disappears from captured image and signal waveforms. This also proves the overflow model.

The improvement method shown in Figure 6 is easily realized in progressive readout mode, but in interlace or random access readout modes, it needs special care for constructing readout logic.

In 2x2 pixel sharing architecture, similar overflow effect may occur (See Figure 9). As FPN is 2x2 mode, it may cause coloring effect in Bayer color filter array. The correcting method shown above is also applicable to this case.

Ⅴ. Conclusions

It was found that horizontal line FPN was observed in vertically shared pixels. The FPN was reduced to below background level by introducing additional shutter operation.

References

[1] R.D.McGrath, et al., "Shared pixels for CMOS image sensor arrays", Proceeding of 2005 IEEE Workshop on CCD and AIS, R3,2005.

[2] H.Takahashi et al., "A 3.9um pixel pitch VGA format 10b digital image sensor with 1.5-transistor/pixel", ISSCC Dig. Tech. Papers, 6.1, 2004.

[3] S.Yoshihara, et al., "A 1/1.8-inch 6.4 M pixel 60 frame/s CMOS image sensor with seamless mode change", ISSCC Dig. Tech. Papers, 27.1, 2006

[4] J.Kim, et al., "1/2.5" 8 mega-pixel CMOS image sensor with enhanced image quality for DSC application", IEDM Proc., S5P3, 2006

[5] M.Mori, et al., "A 1/4in 2M pixel CMOS image sensor with 1.75 transistor/pixel", ISSCC Dig. Tech. Papers, 6.2, 2004.

[6] M.Cohen, et al., "Fully optimized Cu based process with dedicated cavity etch for 1.75um and 1.45um pixel pitch CMOS image sensors", IEDM Proc., S5P3, 2006

[7] K-B.Cho, et al., "A 1/2.5 inch 8.1M pixel CMOS image sensor for digital cameras", ISSCC Dig. Tech. Papers, 28.5, 2007

[8] L.J.Kozlowski, et al., "Performance limits in visible and infrared image sensors", IEDM Proc., S36P1, 1999

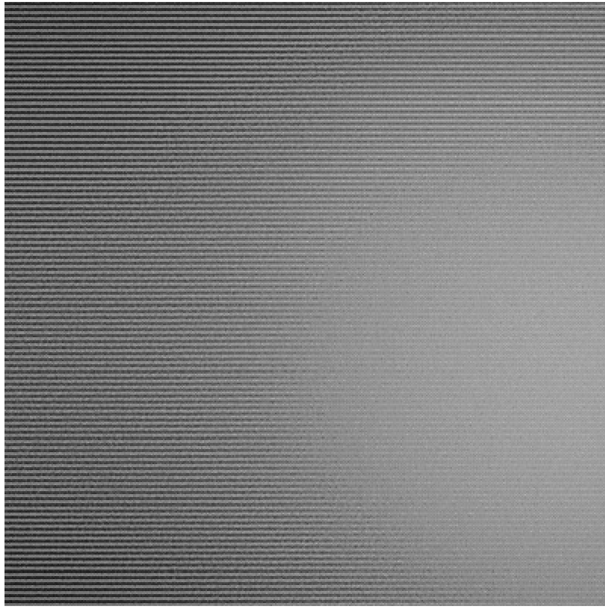


Figure 1. FPN image at high light scene

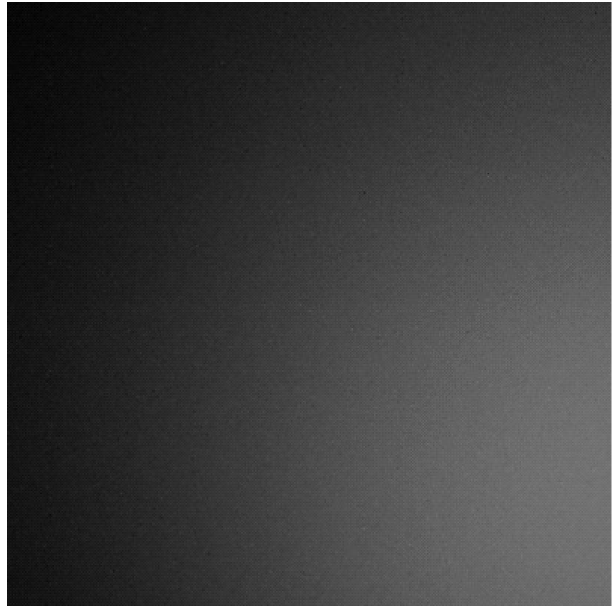


Figure 7. Image with FPN reduction operation

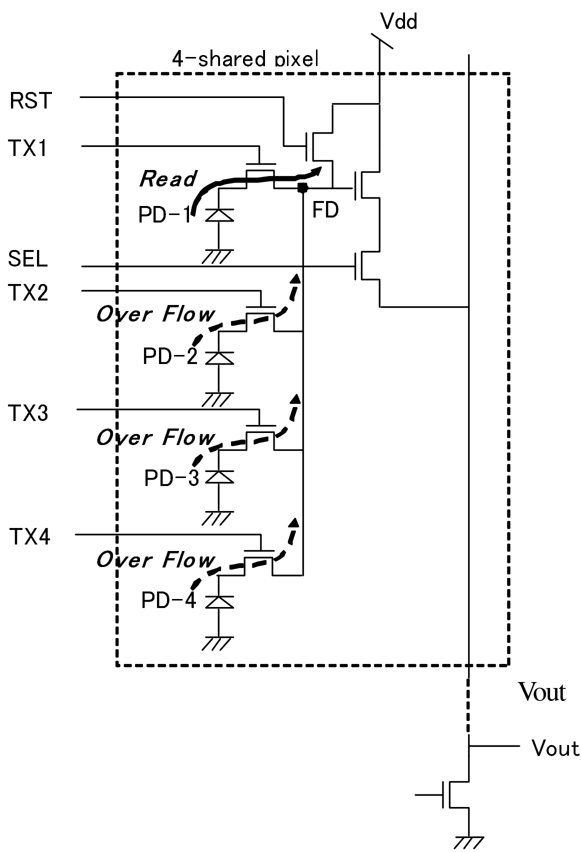


Figure 2. Pixel layout for 4x1 pixel sharing

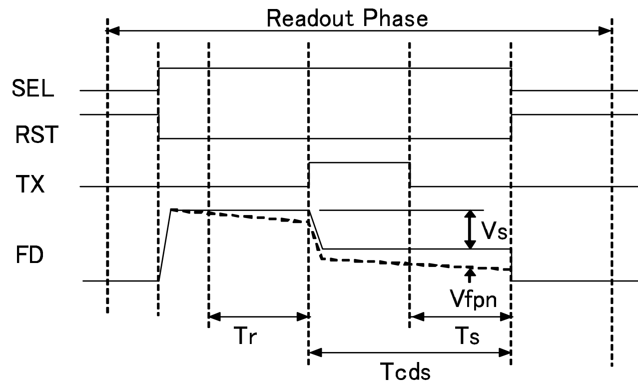


Figure 3. Timing diagram at readout phase

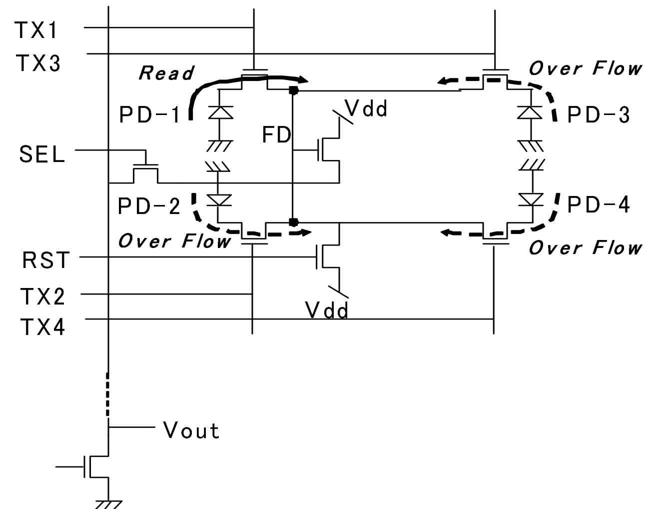


Figure 9. Pixel layout for 2x2 pixel sharing

1H-Shutter — Overflow Line

(A)

Position		Read Timing				
		0H	1H	2H	3H	4H
Position	Line 1	S	R			
	Line 2		S	R		
	Line 3			S	R	
	Line 4				S	R
Overflow			2Δ1	Δ1	0	0〜Δ2

2H-Shutter

(B)

Position		Read Timing					
		0H	1H	2H	3H	4H	5H
Position	Line 1	S		R			
	Line 2		S		R		
	Line 3			S		R	
	Line 4				S		R
Overflow				Δ1	0	0	0〜Δ2

Figure 4. FPN caused by overflow current. (A):1H-shutter, (B):2H-shutter.

1H-Shutter — S': Additional Shutter Line

(A)

Position		Read Timing				
		0H	1H	2H	3H	4H
Position	Line 1	S	R	S'	S'	S'
	Line 2	S'	S	R	S'	S'
	Line 3	S'	S'	S	R	S'
	Line 4	S'	S'	S'	S	R
Overflow			0	0	0	0

2H-Shutter

(B)

Position		Read Timing					
		0H	1H	2H	3H	4H	5H
Position	Line 1	S		R	S'	S'	S'
	Line 2	S'	S		R	S'	S'
	Line 3	S'	S'	S		R	S'
	Line 4	S'	S'	S'	S		R
Overflow				0	0	0	0

Figure 6. FPN reduction timing. (A):1H-shutter, (B):2H-shutter.

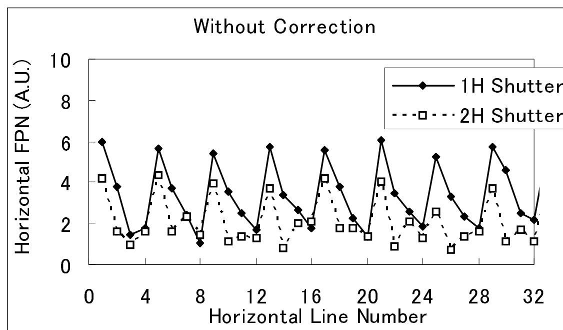


Figure 5. Waveform without FPN reduction

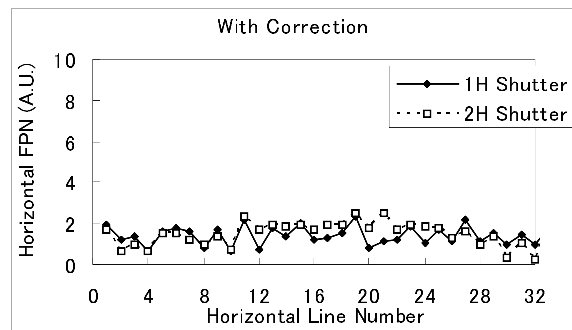


Figure 8. Waveform with FPN reduction

1/4 inch 2Mega CMOS Image Sensor Fabrication

Se Jung Oh*, Keun Hyuk Lim**, Jae Young Rim*, Chan Ki Kim*, An Sik Choi*, Do Young Lee*
*: SiliconFile Technologies Inc.
10F, Yewon Bldg., 75-1, Yangjae-Dong, Seocho-Ku, Seoul 137-130, Korea
TEL : +82-2-578-9037 (ext.219)
FAX : +82-2-578-9337
e-mail : woody@siliconfile.com
**: Dong Bu Electronics.

Abstract

We fabricate a 1/4inch 2mega CMOS image sensor with the non-shared type 2.25um pixel with 4 transistors. To implement this pixel, we use borderless contact to connect driver transistor (Dx) and floating diffusion (FD). The borderless contact replaces one metal connection line and one metal1 contact so that we can ensure the optical fill factor for incident light. Also, this borderless contact helps to get similar fill factor with that of shared type pixels for the implementing 2.25um pixel. This paper presents another approach of pixel design and its competitive performance like 34% fill factor, 550mv saturation level and 10mV/sec dark current level.

1. Introduction

The progress of CMOS fabrication technology has reduced the pixel size in CMOS image sensors significantly, down to 2.2 x 2.2 um^2 [1]. However, most of companies face the similar problems like small fill factor and small light incident windows when they design small size pixels which have non-shared type pixels [2]. These problems are more critical if they want to realize the small size pixel with 4 transistor type or pinned photo diode type pixel [3]. So, most of companies use shared type pixels like 2 shared type or 4 shared type to implement 2.25um pixel or under 2.25um pixel [4].

However, shared type pixels have some issues which are not severe in the case of non shared type pixels. Shared type pixels are weak to the crosstalk because of its different space between photo diodes of shared pixel structure. This structure causes a pixel variation and results in maze noise. Especially, this maze noise is more critical at corner area of pixel array because of large incident angle.

If the spaces between photo diodes are equal, optical crosstalk and electrical crosstalk will happen the same amount in each pixel so there are small maze noises. So, companies need to consider design and process symmetries carefully [5].

In this paper, 2.25um non-shared type pixel structure is presented as an approach to reduce crosstalk and the characteristics of 2 Mega CMOS image sensor, which has the same pixel, is discussed.

2. Pixel architecture and borderless contact

1) Pixel architecture

Fig. 1 shows the pixel design architecture of this work, the most critical issue is to guarantee the optical fill factor for incident light by reducing inter-connection lines which comprises an pixel array, i.e. Tx, Rx, Sx, Vdd, Vout and Dx to FD in pixel array interconnection line. Except Dx to FD interconnection line, other lines cross the whole pixel area to connect the each pixel. However, Dx to FD inter-connection line is just to transfer the potential of FD to the gate of Dx and there is a little need for low resistivity but stable connection.

We use the borderless contact for the interconnection line, which is a standard process for normal logic or SRAM to maximize inter-connection routing efficiency [6]. For the borderless contact, the gate of Dx is extended to the floating diffusion so the interconnection line is replaced by the Dx gate poly. Also, there are no needs to make Dx gate contact. Eventually, the borderless contact is able to reduce 1 metal line and 1 metal1 contact. In Table 1, we compare the numbers of composition units for various pixel types.

Fig. 1 illustrates the circuit diagram of this work. To get the design advantage, the Dx Tr. gate of left side pixel is drawn to the FD junction of right side pixel and the gate poly and FD junction is connected by borderless contact. So, the pixel of this work uses the source follower of the left side pixel.

component	Type A	Type B	Type C	Type D
Transistor	4	4	2.5	1.75
Metal line	6	5	3	2
Metal1 CT	7	6	4	2.5

Table. 1. Comparison table of components of unit pixel

for each different pixel. Type A: Normal 4T pixel, Type B: Normal 4T pixel with borderless contact, Type C: 2Shared 4T pixel, Type D: 4Shared 4T pixel.

The other conditions except using the borderless contact and the source follower of the left side pixel are the same as normal 4T pixel. By developing a 2 mega pixel image sensor with the explained pixel structure using a 0.13um CMOS process, we can get 40% optical fill factor and 34% fill factor.

2) Borderless contact

Fig. 2 shows the top view design of borderless contact and its cross section SEM view. The size of borderless contact is 2times larger than normal contact size in Y direction to realize the stable connection between Dx and FD node.

The test structure of borderless contact is that the poly connected the each active over the field oxide with 0.1um active overlap and the borderless contact connected the poly and active.

The total borderless contacts in this test pattern are 5,000ea. The resistance of each borderless contact is 710ohm/ea. When the Dx gate and FD region are connected with metal line, the FD contact resistance is 50ohm and Dx gate contact resistance is 360ohm/ea because salicide process is not applied to the whole pixel area. It means that borderless contact resistance is 300ohm/ea larger than normal separated FD and Dx gate contact resistance. To verify the contact resistance of borderless contact itself, it is measured in Kelvin pattern. In that case, the contact resistance is 150ohm/ea for borderless contact. So, non-silicide poly and active sheet resistance contribute to the larger borderless contact Rc.

From these results, we reach the conclusion that borderless contact does not make high contact resistance. Also, the borderless contact transfers the potential from FD to Dx gate perfectly even in high poly sheet resistance because there are no current paths to the silicon substrate. Fig. 3 shows the comparison results of unit contact resistance which are used in this work.

3. Process integration and microlens shift

This work is processed in Dong Bu Electronics, which is a foundry company in Korea, with 0.13um technology. Basic process scheme and design rule are the same as normal logic 0.13um technology except the process for making photo diode. STI process is applied to separate active region. STI process can cause the dark current in photo diode because of its rough interface state between silicon and oxide. Appropriate thermal budget is controlled to minimize the dark current caused at interface state. Also, Co-salicide process is blocked for whole pixel area due to two reasons. First is to minimize dark current caused by metallic contaminations even which is not on photo diode. Second is to remove the salicide layer in photo diode area which blocks the incident light into photo diode. USG oxide was applied for IMD and IMO material.

The total height from silicon surface to the bottom of color filter is 3.0um. In the case of color filter, the height was 0.8um for Green filter. So, the total stack height from silicon surface to the bottom of Microlens was 3.8um. According to the simulation and experiment results, the appropriate microlens height is decided to focus the incident light into the photo diode.

In the case of 2Mega product, the incident angle of module lens reaches to 27 deg at 0.8 image field. So, it is very difficult to shrink the microlens with linear method. We applied a non-linear microlens shift for this work. According to the data, Gr/Gb ratio is in max 2% difference in all image area. Fig. 4. shows the captured white image and its Gr/Gb ratio in 64 divided area. There are no maze noises in all image area. Proper microlens shift and non-shared type pixel design minimize crosstalk which can make maze noise.

4. Sensor characteristics

By using the borderless contact to get proper optical fill factor and fill factor, we can make 2Mega CMOS image sensor with 2.25um pixel which is 4T non-shared pinned photo diode type.

According to the pixel design, optical fill factor and fill factor are 40% and 34% each. Measured performance of this work is given by Table 2. Fig. 5. shows the sample image of this work.

Parameters	Value	Remark
Pixel size	2.25 x 2.25 um^2	
Max. SNR	36 dB	
Dynamic Range	60.2dB	
Dark current	10mV/sec	
Sensitivity	750mV/lux sec	@Green
Saturation	> 550mV	

Table 2. Measured image sensor performances

5. Conclusion

2 Mega CMOS image sensor with non-shared pinned photo diode type is fabricated with 0.13um technology. Through this work, we can reach the below conclusions.
1) We can get 40% optical fill factor and 34% fill factor by using borderless contact at 2.25um 4T pinned photo diode structure.
2) According to the evaluation results of electrical characteristics of the borderless contact, it has process reliability to do mass production.
3) Non shared type pixel design and proper non-linear microlens shift reduce optical crosstalk. The Gr/Gb differences are less than 2% in all image area.
4) Saturation level is 550mV and dark level is 10mV/sec.

References

1.Shou-Gwo Wuu et al., International Electron Devices Meeting, IEDM Technical Digest, PP.24.3.1-24.3.4,2001

2.Hideshi Abe, Workshop on Micro and Electron Device, PP.04 2004

3. E.R.Fossum, Proc. SPIE, Vol.1900, PP.2-14, 1993

4.H.Rhodes, et al., IEEE Workshop on Micro-electronics and Electron Device, PP.7-18, 04 2004

5.R.D. McGrath et al, Workshop on Charged-Coupled Devices and Advanced Image Sensor, PP.9-12, 2005

6.T.Lin, et al., Semiconductor Manufacturing Technology Workshop, PP.57-60 06 1998

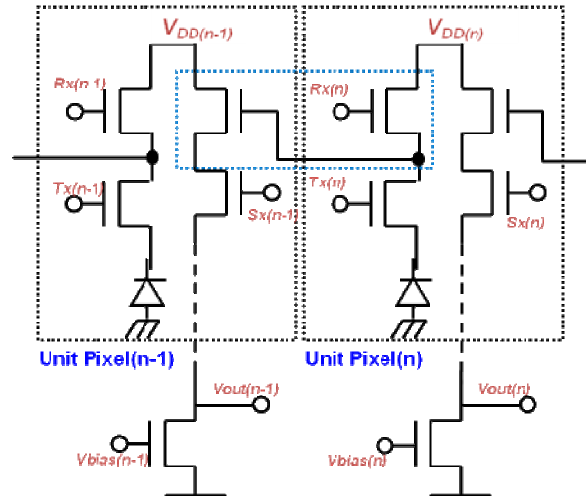
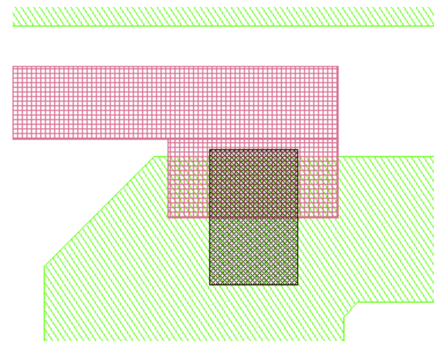
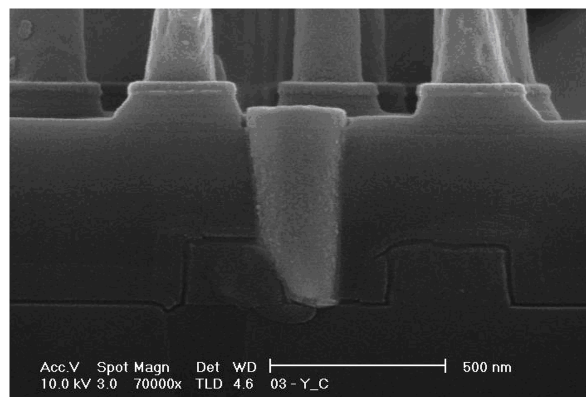


Fig. 1. Pixel architecture of this work. Pixel uses the source follower of left side pixel for the design advantage.



(a) Top view design of borderless contact



(b) Cross-Section SEM view of borderless contact

Fig. 2. Feature of borderless contact of this work.

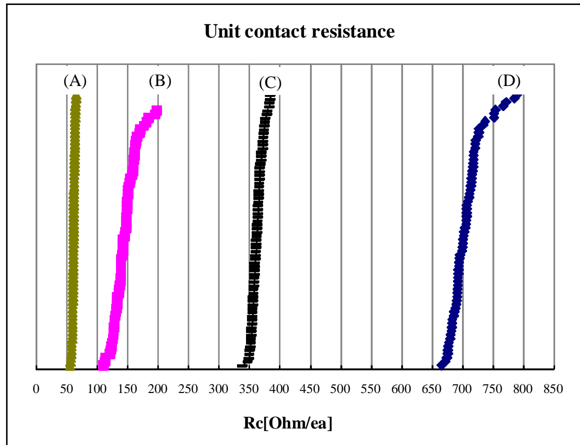
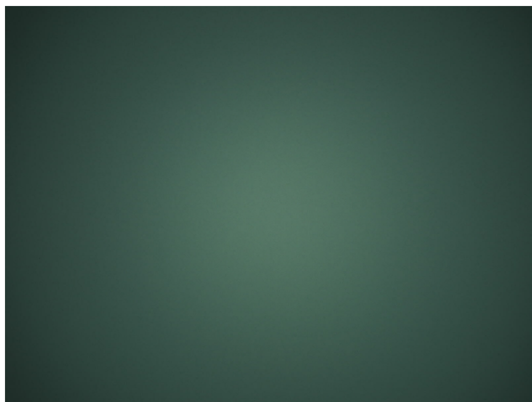


Fig. 3. Comparison graph of metal 1 contact resistance
(a) N+ active contact resistance
(b) Borderless contact resistance in Kelvin pattern
(c) N+ poly contact resistance
(d) Borderless contact resistance



a) White image without ISP @ 5100 Kelvin deg.

0.65	0.03	0.21	0.23	0.42	0.83	0.89	0.55
0.62	0.22	0.11	0.27	0.11	0.61	0.58	0.48
0.55	0.20	0.18	0.19	0.10	0.75	1.01	0.57
0.43	0.01	0.46	0.37	0.45	1.15	1.19	0.89
0.66	0.25	0.32	0.08	0.30	0.99	1.04	0.71
1.03	0.52	0.33	0.47	0.39	0.32	0.57	0.42
1.31	0.92	0.77	0.76	0.74	0.26	0.10	0.08
1.40	1.16	0.83	0.92	0.84	0.40	0.34	0.41

b) Gr/Gb difference at divided image (unit : %)

Fig. 4. Gr/Gb ratio of whole image which was captured by the 2Mega product of this work.

Fig. 5. Captured sample image of this work.

Implementing a CMOS Image Sensor Noise Performance Model

Keith Findlater[1], Ryan Gow[2], David Renshaw[3], Lindsay Grant[4], John Hart[4], Stuart McLeod[4], Robert Nicol[4]
[1]Gigle Semiconductor, Edinburgh, UK. Email: keith.findlater@gigle.biz
[2]University of Oxford, Oxford, UK [3]University of Edinburgh, Edinburgh, UK
[4]STMicroelectronics Imaging Division, Edinburgh, UK

An accurate model of CMOS image sensor noise performance is useful in optimising sensor design and setting targets, ultimately leading to improvements in image quality. Many attempts at modelling CMOS image sensor noise are based on over-simplistic assumptions and may not incorporate a sufficient variety of noise sources to yield a realistic simulator [1]–[3]. These issues inspire the creation of a unified and accurate sensor noise model capable of displaying noisy end-images. In [4], we describe a noise model that incorporates plausible distributions to create realistic images. This paper presents further details of the implementation of such a tool.

Our model has been implemented in MATLAB. The use of this high level programming tool has aided the speed of model development, as many routines are already available for image manipulation and statistical analysis. Figure 1 shows the well known CMOS image sensor noise chain that has been modelled [5]. Optical effects other than diffusion crosstalk in the silicon have not been considered. Realistic modelling of non-Gaussian effects is required to model shot noise, dark current noise, pixel 1/f and RTS noise, and other readout related noises.

Generation of such distributions for megapixel images and for video sequences can be computationally expensive and acceleration methods are needed for acceptable performance and usability from the simulator. For example, the generation of Poisson statistics to model photon and dark current shot noise involves the generation of a Poisson random variable for each pixel with the variance equal to the mean arrival rate. It was found that repeatedly generating such variables was very slow. Fig 2 shows the method used to reduce the computation time, in which pixels of the same value are grouped together and the same Poisson variable used for those pixels. In typical images, the number of unique values is much less than the total number of pixels, so this results in a considerable reduction in computation time. This technique can equally be applied to photon shot and dark current shot noise.

Fixed pattern noise (FPN) such as photo-response non-uniformity (PRNU) also impacts image quality. Our method of modelling this is shown in Fig 3. In this case, a normal distribution is used to model the PRNU. A single frame of PRNU gain values is generated, and this is used over multiple frames to simulate video sequences, resulting in a fixed pattern noise. This method of generating a single frame of noise values is used to model all the fixed pattern effects. Of course the distribution used must be adjusted depending on the type of FPN [6].

Fixed pattern dark current noise is a key example of this. It is important to account for the non-Gaussian nature of this noise, especially the extreme outliers that appear as white pixels [7]. The exponential temperature dependence of this noise is also very important. Figure 4 shows how the dark current is simulated in our model. Using measured characterisation data, three different distributions have been fitted, one for each temperature. These distributions are then scaled by the gain and exposure time values to produce an FPN frame. Following this the shot noise of the dark current is added. As can be seen in Fig 5, realistic dark current effects are produced using this method.

Furthermore, we have accounted for non-Gaussian random noise, such as in the pixel source follower [8] and other readout electronics. As with the dark current modelling, we did not succeed in finding a single distribution which could account for the majority of the population while also reflecting the extreme outliers. Therefore we combined the Fischer-Tippet-Gumbel [9] distribution with a uniform distribution as is shown in Fig 6. Fig 7 shows in detail how we have modelled the RTS and 1/f noise of the pixel source follower using the combination of these two distributions.

Many noise sources in our model required the use of non-Gaussian distributions. However we were able to model the thermal noise of the readout chain, the vertical fixed pattern noise, and the time varying line noise, using Gaussian random variables with appropriate variance. Figure 8 shows the method of modelling time varying line noise while Figure 9 shows an example of measured values versus the model; they are in good agreement.

Figure 10 shows the complete noise model chain, and a simulated image with all noise sources enabled is given in Figure 11. Exaggerated noise parameters have been used for illustration purposes.

The model has proved useful for evaluating trade-offs between various noise parameters. An example of this is given in Figure 12. For two different values of vertical FPN, the simulated light level is swept. It can be seen that at low light, even a low value of vertical FPN (in this case 5 electrons input referred) is still visible. Many other similar investigations are possible using this model and the results provide a means of setting and justifying design and process targets for image sensors development.

[1] J. Farrell *et al.,* "A simulation tool for evaluating digital camera image quality", *Proc. of SPIE*, v. 5294, pp. 124–131, 2004.
[2] H. Wach and E. Dowski, "Noise modeling for design and simulation of computational imaging systems", in *Proceedings of the Color Imaging Conference: Color Science, Systems, and Application,* pp. 211–216, 2004.
[3] R. Costantini and S. Süsstrunk, "Virtual Sensor Design", *Proceedings of SPIE*, v. 5301, pp. 408–419, 2004.
[4] R. Gow *et al.*, "A Comprehensive Tool for Modeling CMOS Image Sensor Noise Performance", submitted to IEEE Transactions on Electron Devices, accepted for publication 2007
[5] A. Theuwissen, "The Effect of Shrinking Pixels in Existing CMOS Technologies", Fraunhofer IMS Workshop CMOS Imaging, 2002.
[6] L. Grant, "Characterisation of noise sources in CMOS image sensors", presented at *IEEE Solid-State Circuits Conference Image Sensor Design Forum*, Feb. 2005.
[7] J. Janesick, *Scientific Charge-Coupled Devices*, SPIE Press, 2001.
[8] K. Findlater *et al.*, "Source follower noise limitations in CMOS active pixel sensors", Proc. of SPIE, v5251, pp 187-195, Feb 2004
[9] J. Beirlant, *et al*, *Statistics of Extremes: Theory and Applications*, Hoboken, NJ: Wiley, 2004.

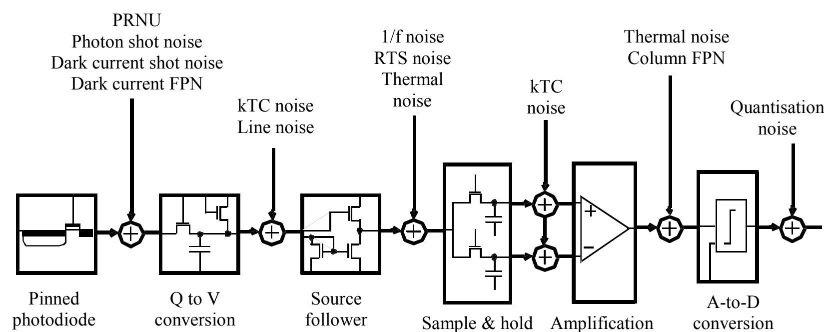


Fig. 1. Main noise sources in the CMOS imager pipeline (adapted from [5]).

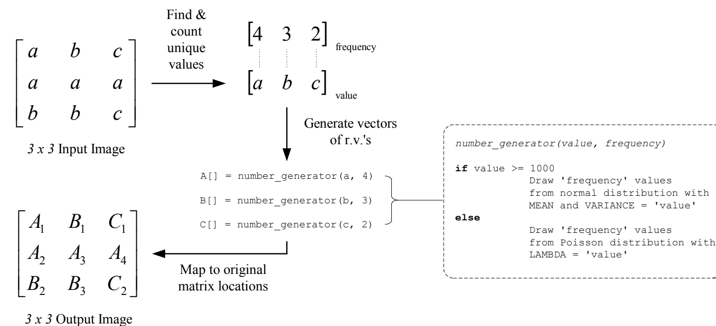


Fig. 2. Simple example of how to exploit recurring pixel values.

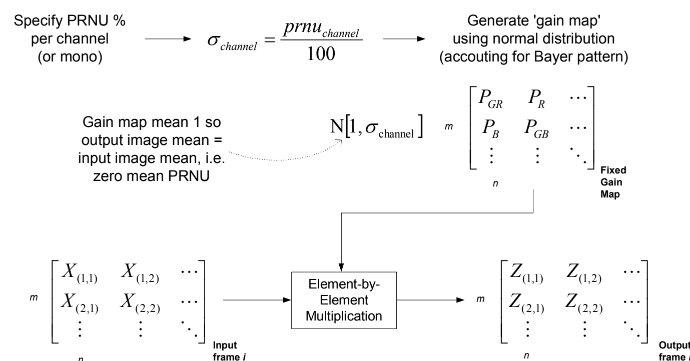


Fig. 3. Technique of modeling PRNU.

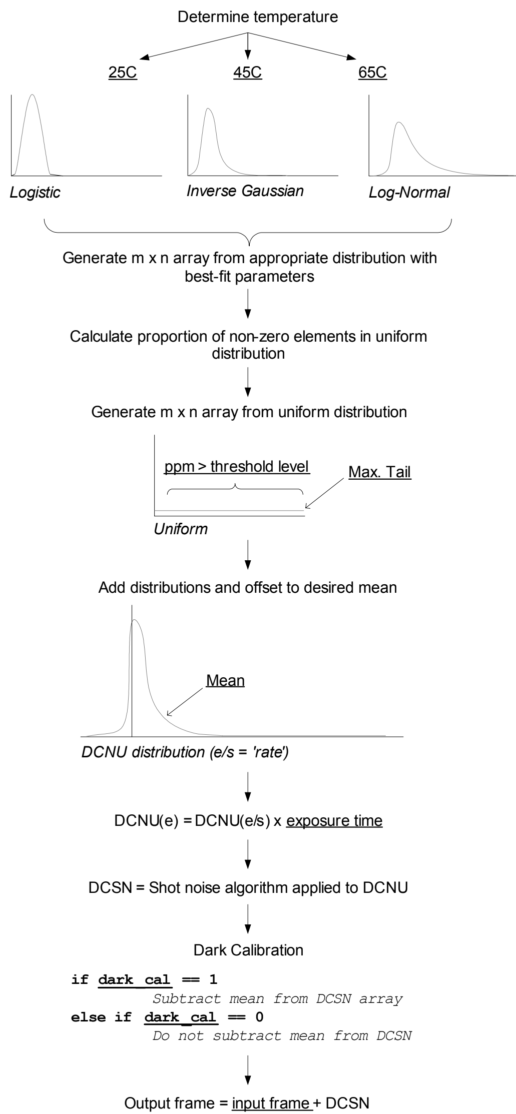


Fig. 4. Process of modeling dark current. Underlined text indicates input parameters specified by the user.

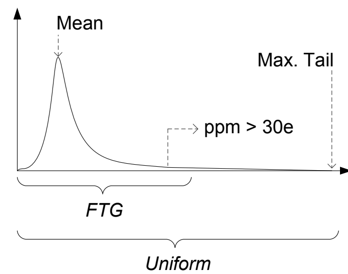


Fig. 6. Sketch of a synthetic flicker noise distribution, indicating the two underlying pdf's used and which parameters are controllable by the user.

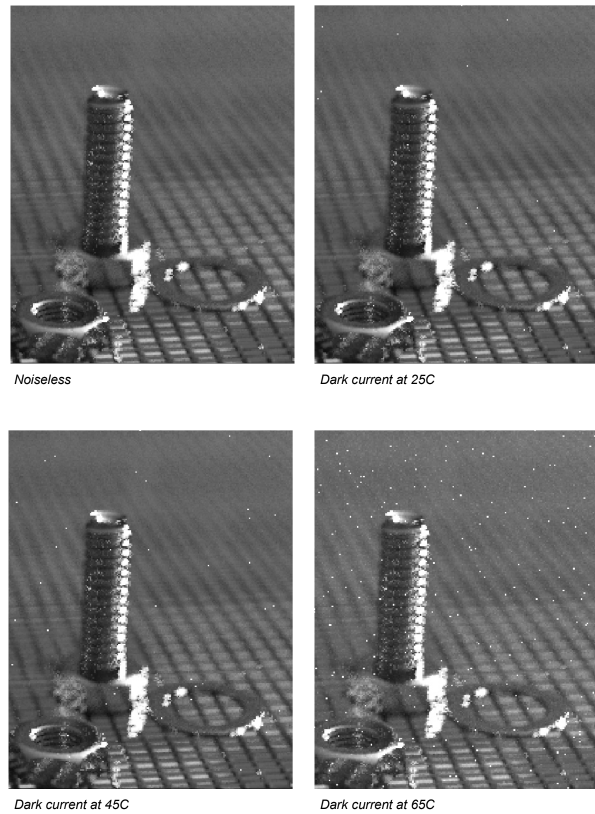


Fig. 5. Impact of dark current at 25˚C, 45˚C and 65˚C on a noiseless image at 0.25s exposure, using exaggerated dark current parameters for illustration.

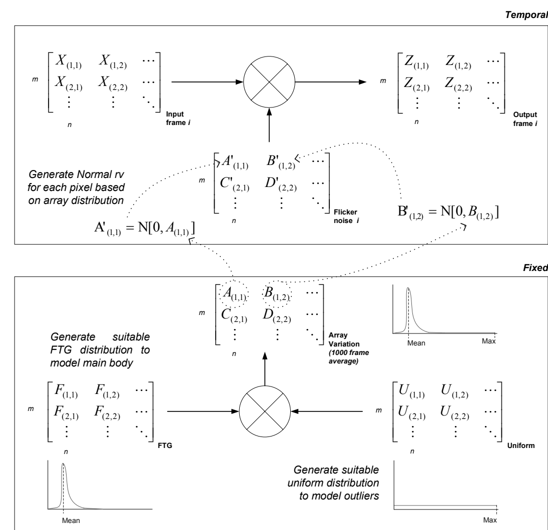


Fig. 7. Overview of the technique used to model flicker/RTS noise.

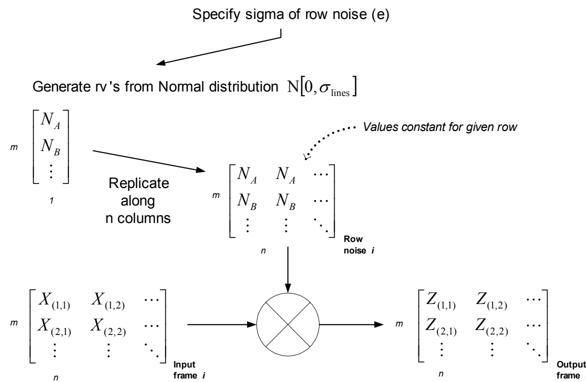


Fig. 8. Technique used to model temporal row noise.

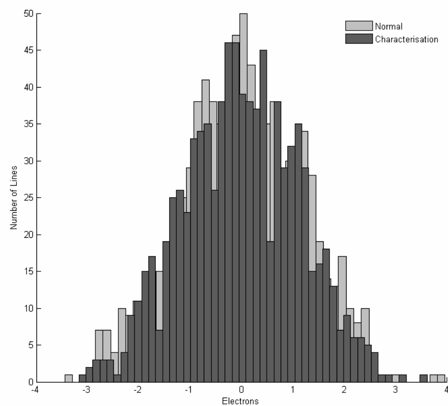


Fig. 9. Comparison of an actual temporal row noise histogram and a normal distribution with the same mean and standard deviation.

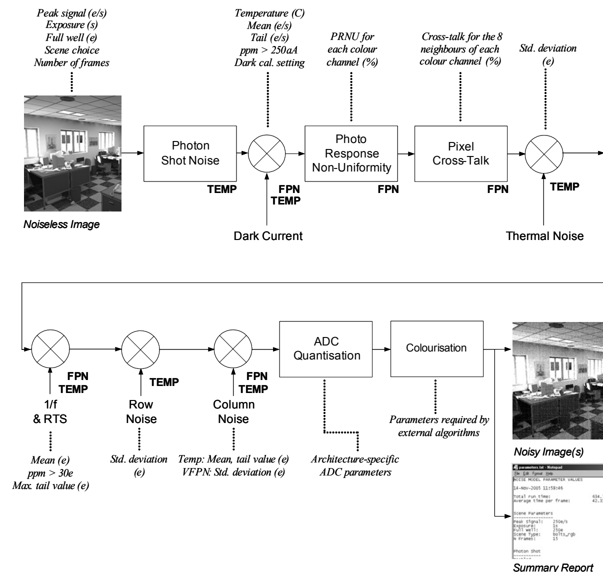


Fig. 10. Block diagram of the overall sensor noise model.

Fig. 11. Simulation of the entire sensor noise chain, based on exaggerated noise values for illustration purposes.

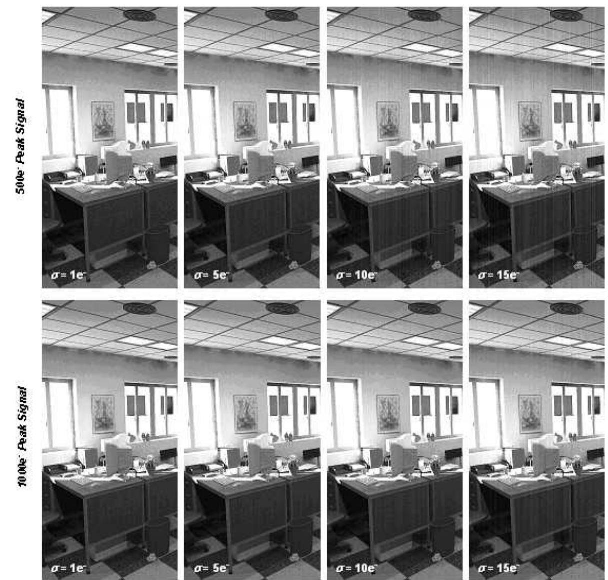


Fig. 12. Images showing the impact of various VFPN levels at low and medium light.

Charge Transfer Noise in Image Sensors

Boyd Fowler and Xinqiao (Chiao) Liu
Fairchild Imaging, 1801 McCarthy Blvd. Milpitas, CA 95035 USA

***Abstract*— Charge transfer noise often limits the performance of image sensors when read noise is reduced to below 2e- RMS. Therefore, understanding the source or sources of charge transfer noise and how they can be reduced is essential for the design of ultra low noise image sensors. In this paper we analyze charge transfer noise in a 4T CMOS image sensor using a simple 1-D model.**

We investigate incomplete charge transfer noise and determine that it is not a significant source of transfer noise in 4T CMOS image sensor. Therefore, we conclude that the most probable source of transfer noise in 4T CMOS image sensors is charge trapping and detrapping at the Si–SiO2 interface during the charge transfer process. We propose a model for analyzing this noise based on a random sum of random telegraph signals. Finally we analyze this model and discuss how it can be verified.

I. Introduction

READ noise sets the fundamental detection limit for image sensors. Process improvements in modern image sensors have reduced reset noise and source follower noise to levels where other sources are starting to dominate. Specifically, charge transfer noise often limits the performance of image sensors when read noise is reduced to below 2e- RMS. Therefore, understanding the source of charge transfer noise and how it can be reduced is essential for the design of ultra low noise image sensors.

Charge transfer noise was first rigorously investigated in surface channel CCDs in the early 1980s by Omura and Owanda [1]. They derive the charge noise generated by surface trapping and detrapping while signal charge is moved from the photogate pixel to the output amplifier. Their model matches measured results for sensors with a large number of charge transfer stages and a large number of traps. Unfortunately, their results break down for cases when the number of charge transfers and or traps is small. Incomplete charge transfer noise has been reported in CMOS photogate sensors [2], CMOS pinned photodiode sensors [3] and hybrid CCD/CMOS image sensors [4].

In this paper we analyze charge transfer noise in a 4T APS using a 1-D model. This same model can be used for analyzing charge transfer noise in the final stage of a CCD or a hybrid CCD/CMOS image sensor. The remainder of this paper is organized as follows: Section II presents a 1-D model for analyzing charge transfer noise. The following section presents a detailed analysis of the 1-D model, and derives a closed form solution for the charge transfer noise power and its spectrum. The final section provides summary conclusions.

II. Transfer Noise Model

In this section we develop a simple model for charge transfer noise in 4T CMOS image sensors. A typical 4T CMOS image sensor pixel is shown in Figure 1. There are at least two possible causes for transfer noise, the first is incomplete charge transfer between the pinned photodiode and the floating diffusion node, and the second is charge trapping and detrapping at the Si–SiO2 interface [1]. Incomplete charge transfer results in variations in thermionic emission and or quantum mechanical tunneling from either a potential barrier or a potential pocket between the pinned photodiode and the floating diffusion node. Charge trapping also causes variation in the charge collected on the floating diffusion node.

In order to determine if incomplete charge transfer is a source of noise in 4T CMOS image sensors, we will estimate the average time required to empty charge from a small potential barrier or a small potential pocket within the pinned photodiode (see Figure 2). We will assume that thermionic emission is the dominant source of electron transport from the potential pocket to the floating diffusion node. In addition, we will assume that at $t = 0$ the potential pocket is filled with

[1] It is also possible that charge trapping occurs in the bulk, but typically the density of bulk traps is very low in modern CMOS processes.

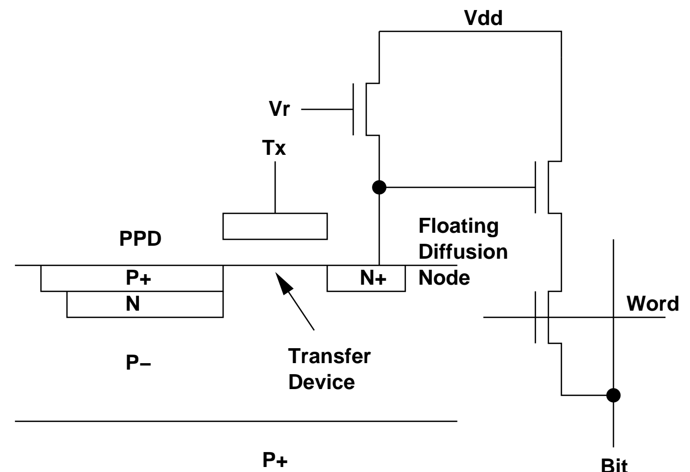


Fig. 1. 4T APS Pixel

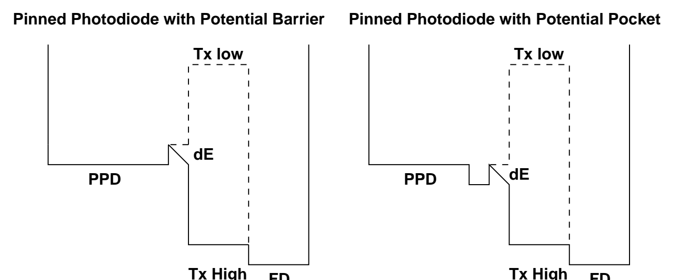


Fig. 2. Pinned Photodiode Energy Diagram

electrons. The probability of an electron being emitted from the potential pocket during a small time interval dt is equal to the probability that a given electron has enough energy to jump over the barrier times the probability that the same electron is close enough to the barrier to jump over, times the number of electrons inside the potential well, i.e.

$$P_r(N+1,t+dt|N,t) = \frac{1}{1+e^{-\frac{q^2N^2}{k\theta c_{pd}}}} \frac{(N_0-N)v_{th}dt}{2l_{pd}}, \quad (1)$$

where N is the number of electrons emitted from the potential pocket at time t, N_0 is the number of electrons in the potential pocket at $t = 0$, v_{th} is the thermal velocity of electrons in the potential pocket at thermal equilibrium, l_{pd} is the length of the photodiode, q is the charge of an electron, k is Boltzmann's constant, θ is absolute temperature, and c_{pd} is the pinned photodiode capacitance. Note that dt can be made small enough such that the probability of emitting more than one electron during dt is vanishingly small. Equation 1 assumes that the location of each electron is uniformly distributed within the potential well, and that each electron is traveling to either the left or right with velocity v_{th}. When an electron hits the potential barrier it either bounces off the barrier or jumps over it. The probability of an electron bouncing off the barrier or jumping over it is determined by the Fermi-Dirac distribution, where the difference between the Fermi level and the barrier is assumed to be

$$\Delta E = \frac{q^2N^2}{k\theta c_{pd}}. \quad (2)$$

If we assume that electrons are independently emitted from the potential well with an exponential waiting time then using Equation 1 it can be shown that the probability density function of the emission time of the Nth electron, T_N, is

$$f(t_N|N) = \frac{1}{\tau_N} e^{-\frac{t_N}{\tau_N}}, \quad (3)$$

where t_N is the time between the emission of the Nth and $N+1$th electron, and

$$\tau_N = \frac{1}{1+e^{-\frac{q^2N^2}{k\theta c_{pd}}}} \frac{(N_0-N)v_{th}}{2l_{pd}}. \quad (4)$$

The time to emit all N_0 electrons from the potential pocket is

$$T_{emission} = \sum_{i=1}^{N_0} T_i. \quad (5)$$

Therefore the average emission time is

$$\begin{aligned} E[T_{emission}] &= \textstyle\sum_{i=1}^{N_0} E[T_i] \\ &= \textstyle\sum_{i=1}^{N_0} \tau_i, \end{aligned} \quad (6)$$

and the variance of the emission time is

$$\begin{aligned} \sigma^2_{T_{emission}} &= \textstyle\sum_{i=1}^{N_0} (E[T_i^2] - E[T_i]^2) \\ &= \textstyle\sum_{i=1}^{N_0} \tau_i^2. \end{aligned} \quad (7)$$

Assuming that $N_0 = 100e-$, $v_{th} = 1.33 \times 10^5$m/s, $l_{pd} = 10\mu$m, $\theta = 300$K, and $c_{pd} = 4$fF, then $E[T_{emission}] = 0.821$ns and $\sigma_{T_{emission}} = 0.193$ns. Clearly the emission time of this process is much faster than the typical charge transfer time in a 4T CMOS image sensor, i.e. approximately 1μs. Therefore, even if our example is off by one or two orders of magnitude, due to the 1-D approximation, incomplete charge transfer is not a significant source of charge transfer noise. If lag in the pinned photodiode is very large this analysis should be reconsidered. Additional information on thermionic-emission from potential wells is discussed by Kawai [5] and Janesick [6].

Charge trapping and detrapping at the Si–SiO2 interface is likely the dominate source of charge transfer noise in 4T CMOS image sensors. Specifically, as charge is transferred from the pinned photodiode to the floating diffusion node it comes in contact with the Si–SiO2 interface near the floating diffusion node. In addition, while the transfer gate voltage is held high electrons from the floating diffusion can interact with surface traps in the transfer channel. Both of these mechanisms enable charge trapping and or detrapping during charge transfer. We propose the following random telegraph based model to analyze charge fluctuations at the floating diffusion node while the transfer gate is high. The number of electrons added or subtracted to the floating diffusion node at time $t \geq 0$ is

$$Y(t) = \sum_{i=1}^{N} Z_i(t), \quad (8)$$

where i is the trap index, and N is the number of traps in the transfer channel. Each trap is either full or empty at time t and its initial state is unknown. The number of electrons added or subtracted to the floating diffusion node at time $t \geq 0$ by trap i is

$$Z_i(t) = X_i(t) + B_i, \quad (9)$$

where $X_i(t)$ is a random telegraph signal (RTS) with unit amplitude, and B_i is a random variable with $P_r(B = 1/2) = 1/2$ and $P_r(B = -1/2) = 1/2$. B_is are determined at $t = 0$ and stay constant for $t > 0$. B_is are assumed to be uncorrelated. Therefore $Z_i(t)$ toggles between 0 and 1 or 0 and -1 depending on the value of B_i. Moreover, if $B_i = 1/2$ then $Z_i(t)$ toggles between 0 and 1 representing a trap that contained an electron at $t = 0$. If $B_i = -1/2$ then $Z_i(t)$ toggles between 0 and -1 representing a trap that was empty at $t = 0$. By definition, we assume that each trap can only hold one electron[2]. The number of traps in the channel N is a random variable with mean μ_N and variance σ_N^2. Each RTS $X_i(t)$ has a Poisson distributed transition probability, i.e. the probability of m transitions in t seconds is

$$P_r(m,t) = \frac{(\nu t)^m e^{-\nu t}}{m!} \quad t \geq 0 \quad m \geq 0, \quad (10)$$

where ν is the characteristic transition frequency. We also assume that RTSs are uncorrelated, and that the average emission and capture times are equal for each RTS[3]. Figure 3 shows a typical waveform for $X_i(t)$. The characteristic transition frequency ν is a random variable with the following

[2]This may not always be a good approximation but it simplifies the mathematics in this paper.

[3]The average emission and capture times for each trap are not stationary, they are a function of the channel potential, but we will neglect this in our analysis.

distribution

$$f_\nu(\nu) = \frac{1}{\nu \ln(\frac{\nu_2}{\nu_1})} \quad \nu_1 \leq \nu \leq \nu_2 \tag{11}$$

where ν_1 is the lowest transition frequency of any trap and ν_2 is the highest transition frequency of any trap. $f_\nu(\nu)$ is derived assuming that traps are uniformly distributed as a function of depth into the SiO2 [7]. Note that this assumption it typically used to explain 1/f noise in surface channel MOSFETs. We

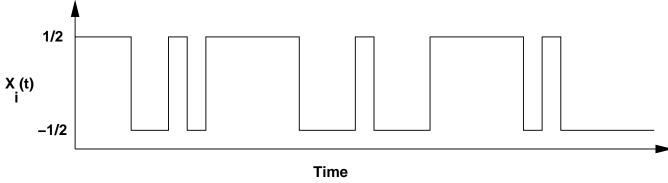


Fig. 3. RTS Waveform

assume that N and ν are independent random variables.

III. Transfer Noise Analysis

In this section we analyze the model developed in Section II. In order to derive the autocorrelation function of $Y(t)$ we need to determine the statistics of its components. By definition a symmetric RTS, with Poisson distributed transition times and a fixed transition frequency ν, has a mean value of zero, i.e.

$$E[X_i(t)|\nu] = 0, \tag{12}$$

and an autocorrelation function

$$E[X_i(t)X_i(t+\tau)|\nu] = \frac{1}{4}e^{-2\nu|\tau|}. \tag{13}$$

Note that this shows that $X_i(t)$ is wide sense stationary and therefore $Y(t)$ will also be wide sense stationary. Since RTSs are assumed to be uncorrelated

$$E[X_i(t_1)X_j(t_2)|\nu] = 0 \quad i \neq j. \tag{14}$$

It can then be shown that

$$E[Z_i(t)|\nu] = 0, \tag{15}$$

$$E[Z_i(t)Z_i(t+\tau)|\nu] = \frac{1}{4}e^{-2\nu|\tau|}, \tag{16}$$

and

$$E[Z_i(t_1)Z_j(t_2)|\nu] = 0 \quad i \neq j. \tag{17}$$

Now we are ready to determine the average value of $Y(t)$ given ν, i.e.

$$E[E[Y(t)|N,\nu]] = 0. \tag{18}$$

The autocorrelation function of $Y(t)$ given N and ν, i.e. the autocorrelation function of $Y(t)$ with a known number of traps with a fixed trapping frequency ν, is

$$\begin{aligned} E[Y(t)Y(t+\tau)|N,\nu] &= E[(\textstyle\sum_{i=1}^N Z_i(t))\times \\ &\quad (\textstyle\sum_{j=1}^N Z_j(t+\tau))|N,\nu] \\ &= NE[Z_i(t)Z_i(t+\tau)|\nu]+ \\ &\quad N(N-1)E[Z_i(t)Z_j(t+\tau)|\nu]. \end{aligned} \tag{19}$$

Taking the expectation of $E[Y(t)Y(t+\tau)|N,\nu]$ with respect to N we find

$$\begin{aligned} R_{YY|\nu}(\tau) &= E[Y(t)Y(t+\tau)|\nu] \\ &= \tfrac{1}{4}\mu_N e^{-2\nu|\tau|}. \end{aligned} \tag{20}$$

Since $Y(t)$ is wide sense stationary the two sided power spectral density is defined as the Fourier transform of the autocorrelation function $R_{YY|\nu}(\tau)$, i.e.

$$\begin{aligned} S_{YY|\nu}(f) &= \textstyle\int_{-\infty}^{\infty} R_{YY|\nu}(\tau)e^{-2\pi jf\tau}d\tau \\ &= \frac{\mu_N}{4}\frac{\frac{1}{\nu}}{1+(\frac{\pi f}{\nu})^2} \quad -\infty \leq f \leq \infty. \end{aligned} \tag{21}$$

This shows that $Y(t)$ given ν has a Lorentzian spectrum as expected for this model. Taking the expectation of $S_{YY|\nu}(f)$ over ν we find

$$\begin{aligned} E[S_{YY|\nu}(f)] &= \frac{\mu_N}{4}\int_{\nu_1}^{\nu_2}\frac{\nu}{\nu^2+(\pi f)^2}f_\nu(\nu)d\nu \\ &= \frac{\mu_N}{4\ln(\frac{\nu_2}{\nu_1})}\int_{\nu_1}^{\nu_2}\frac{1}{\nu^2+(\pi f)^2}d\nu \\ &= \frac{\mu_N}{4\ln(\frac{\nu_2}{\nu_1})}\frac{tan^{-1}(\frac{\nu_2}{\pi f})-tan^{-1}(\frac{\nu_1}{\pi f})}{\pi f}. \end{aligned} \tag{22}$$

This shows that the noise power spectrum of $Y(t)$ has an inverse frequency dependence between ν_1 and ν_2. Again this is expected based on our trap frequency distribution $f_\nu(\nu)$. This model can be verified by first measuring the power spectrum of a single pixel while the transfer gate is high, and then measuring the spectrum of the same pixel with the transfer gate low. The difference of the two power spectrums is the power spectrum of the charge transfer noise. If the transfer device has a large number of traps then equation 22 should predict the measured transfer noise power spectral density, but if the number of traps is close to one then equation 21 should predict the measured transfer noise power spectral density. If neither equation matches the measured transfer noise power spectral density, then this model is not valid for predicting charge transfer noise! Figures 4 and 5 show the power spectral densities predicted by equations 21 and 22 respectively. Figure 4 assumes $\mu_N = 1$ and $\nu = 10000$ transition/sec, and Figure 5 assumes $\mu_N = 10$, $\nu_1 = 10$ transitions/sec and $\nu_2 = 10^7$ transitions/sec.

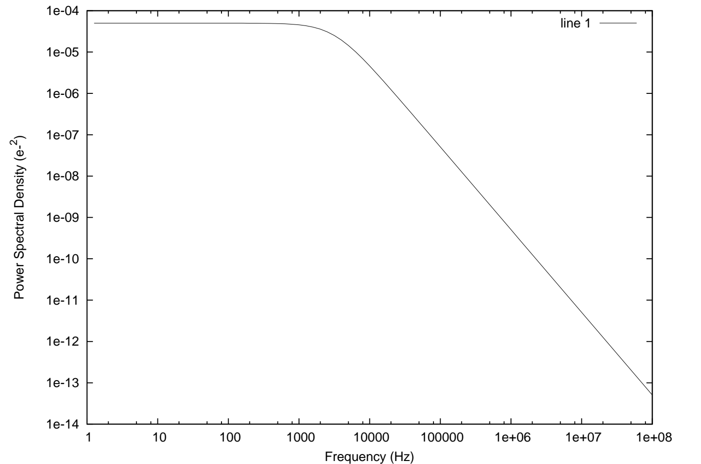


Fig. 4. Lorentzian Noise Spectrum Predicted by Equation 21

In most applications 4T CMOS image sensors with pinned photodiodes use correlated double sampling (CDS) to measure the charge transferred from the pinned photodiode to the floating diffusion node. Therefore, we define

$$A(t) = Y(t) - Y(0) \quad t \geq 0 \tag{23}$$

to estimate the charge transfer noise power after CDS. A typical waveform of $A(t)$ is shown in Figure 6. It can be shown that

$$E[A(t)] = 0, \tag{24}$$

and

$$\begin{aligned} E[A(t)^2|\nu] &= E[(Y(t) - Y(0))^2] \\ &= 2E[Y(0)^2 - Y(0)Y(t)] \\ &= \tfrac{1}{2}\mu_N(1 - e^{-2\nu t}). \end{aligned} \tag{25}$$

Taking the expectation of $E[A(t)^2|\nu]$ with respect to ν we find

$$\begin{aligned} E[A(t)^2] &= \tfrac{\mu_N}{2}\int_{\nu_1}^{\nu_2}(1 - e^{-2\nu t})f_\nu(\nu)d\nu \\ &= \tfrac{\mu_N}{2\ln(\frac{\nu_2}{\nu_1})}\int_{\nu_1}^{\nu_2}(1 - e^{-2\nu t})\tfrac{1}{\nu}d\nu \\ &= -\tfrac{\mu_N}{2\ln(\frac{\nu_2}{\nu_1})}\sum_{i=1}^{\infty}\tfrac{(-2\nu_2 t)^i - (-2\nu_1 t)^i}{i(i!)}. \end{aligned} \tag{26}$$

Figure 7 shows the variance of $A(t)$, i.e. $E[A(t)^2]$, as a function of time assuming that $\mu_N = 10, \nu_1 = 10$ transitions/s, and $\nu_2 = 1e7$ transitions/s. For small values of t

$$E[A(t)^2] \approx \mu_N \frac{t(\nu_2 - \nu_1)}{\ln(\frac{\nu_2}{\nu_1})}. \tag{27}$$

This implies that charge should be transferred from the pinned photodiode to the floating diffusion node as quickly as possible, i.e. the transfer gate should be pulsed high for as short a period of time as necessary to transfer all of the charge in the pinned photodiode. Clearly there is a trade off between image lag, incomplete charge transfer, and transfer noise in a 4T APS.

IV. Conclusion

We have presented a theoretical framework for understanding and modeling charge transfer noise in CMOS, CCD and hybrid CCD/CMOS image sensors. Further work is still required to validate this model using both simulated and measured data.

References

[1] Y. Omura and K. Ohwada, “Charge–Transfer Noise Theory for Surface–Channel Charge–Coupled Devices,” *IEEE Transactions on Electron Devices*, vol. 27, no. 9, pp. 1816–1824, September 1980.

[2] A. J. Blanksby and M. J. Loinaz, “Performance Analysis of a Color CMOS Photogate Image Sensor,” *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 55–64, January 2000.

[3] X. Liu *et al.*, “High Performance CMOS Image Sensor for Low Light Imaging,” in *2007 Internation Image Sensor Workshop*, Ogunquit, Maine, USA, June 2007.

[4] B. Fowler *et al.*, “CCD / CMOS Hybrid FPA for Low Light Level Imaging,” in *Proceedings of SPIE*, vol. 5881, San Diego, August 2005.

[5] S. Kawai *et al.*, “Thermionic-Emission Based Barrier Height Analysis for Precise Estimation of Charge Handling Capacity in CCD Registers,” *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1588–1592, October 1997.

[6] J. Janesick, *Scientific Charge Coupled Devices*. New York: SPIE Press, 2001.

[7] A. Van der Ziel, *Noise in Solid State Devices*. New York: Wiley, 1986.

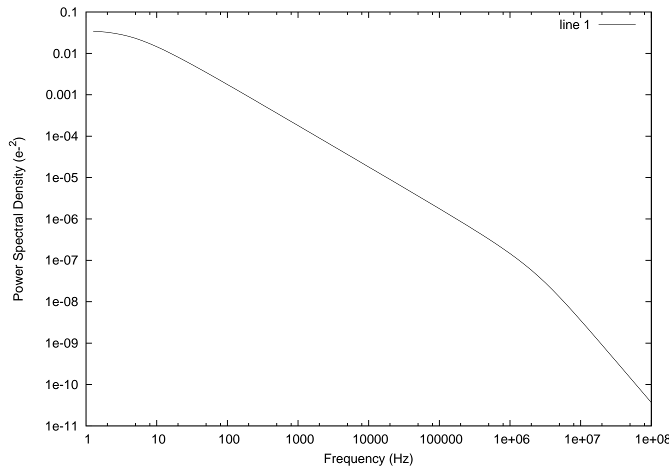


Fig. 5. 1/f Noise Spectrum Predicted by Equation 22

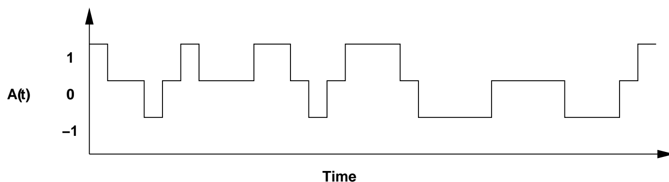


Fig. 6. Typical $A(t)$ Waveform

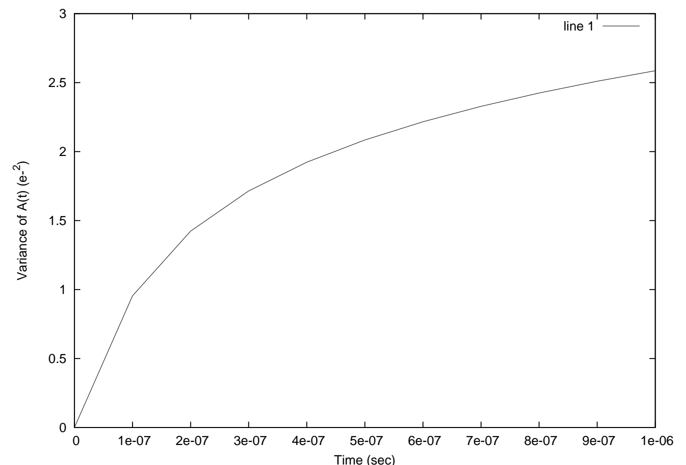


Fig. 7. Variance of $A(t)$ as a function of time

A 2.3e- Read Noise 1.3Mpixel CMOS Image Sensor with Per-Column Amplifier

Kwang-Bo Cho, Chiajen Lee, Siri Eikedal, Hai Yan, Taehee Cho, Tien-Min Miao,
Jason Song, Christopher Zeleznik, Alexander Mokhnatyuk, Sandor Barna

Micron Technology, Inc.
251 S. Lake Ave., 6-th Floor, Pasadena, California 91101.
Tel: 626-685-5169, Email: acho@micron.com.

Low-noise, low-power, area-efficient CMOS imager readout architecture is studied through four 1.3Mpixel test chips using the same pixel array and silicon area. By employing per-column amplifier in front of column sample-and-hold circuitry and utilizing the extended correlated-double-sampling[1,2] principle, a low 2.3e- read noise is achieved, as compared to 4.2e- with conventional serial analog multi-stage readout chain architecture. The gain stages and 10-bit pipelined analog-to-digital converter (ADC) featured the shared-amplifier with short-reset scheme [3] delivered a maximum of 64x analog gain with differential nonlinearity (DNL) +0.3/-0.6 least significant bit (LSB) and integral nonlinearity (INL) +1.2/-0.75 LSB with 50% lower power consumption.

Based on a 1/4-inch optical format 1.3Mpixel CMOS active-pixel digital image sensor with 1280x1024 resolution and 2.8um pixel size, this sensor requires 2.8V nominal pixel power supply, 1.8V nominal logic supply, and 1.7V to 3.6V I/O. The imager includes a low-noise signal readout chain, a 10-bit ADC, an internal phase-locked loop (PLL), and a 10-bit parallel interface to output pixel data at up to 27 megapixels per second (Mp/s). The imager uses a 2.5T cell 2.8μm × 2.8μm pixel configured in common element pixel architecture (CEPA) for high fill factor and light sensitivity. It also uses top and bottom multiple channels with analog signal readout at a rate of 13.5Mp/s, which result in 15 frames per second (fps) at full resolution and 30fps at VGA resolution in full field of view (FOV). Operating power consumption of the chip in full resolution at 15fps is less than 65mW. The chip dimensions are 6.25mm × 5.2mm.

Figure 1 shows the imager architecture. A conventional serial analog readout multi-stage chain is shown in Figure 2. Figure 3 shows low-noise analog readout chain with per-column amplifier. Figure 4 shows shared-opamp scheme for gain stages and 10-bit pipelined ADC. Figure 5 shows a comparison of capture images. Variation configurations and corresponding readout noises are summarized in Table 1.

References:

[1] Alex Krymski, Nail Khaliullin, Howard Rhodes, "A 2 e- noise 1.3Megapixel CMOS sensor", IEEE Workshop on CCDs and Advanced Image Sensors, 2003.
[2] Nobuhiro Kawai, Shoji Kawahito, " Noise analysis of high-gain, low-noise column readout circuits for CMOS image sensors," IEEE Trans. Electron Devices, vol. 51, no. 2, pp. 185-194, 2004.
[3] Taehee Cho, Sandor Barna, Andrew Lever, Kwang-Bo Cho, Chiajen Lee, "Sharing operational amplifier between two stages of pipelined adc and/or two channels of signal processing circuitry," United States Patent (US 7148833), Dec. 2006.

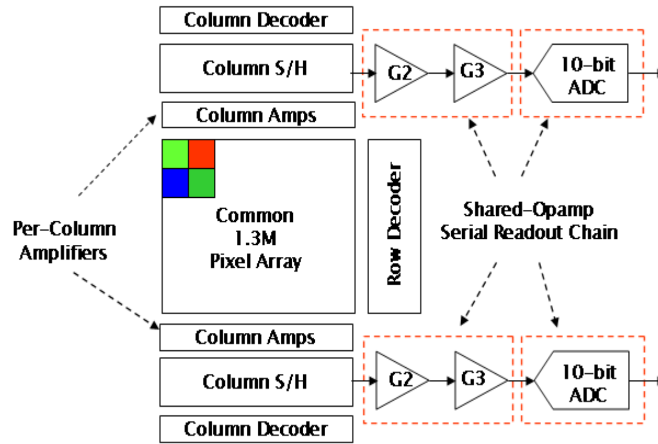


Fig. 1: Overall architecture.

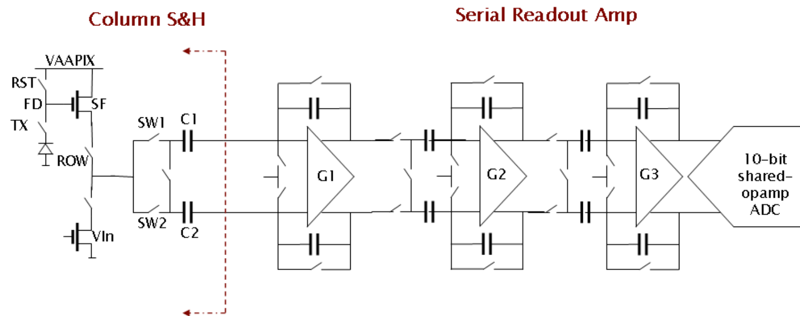


Fig. 2: Conventional serial analog multi-stage readout chain.

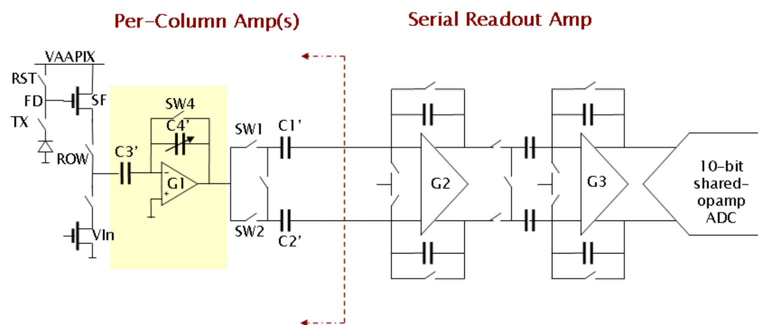


Fig. 3: Analog readout chain with per-column amplifier.

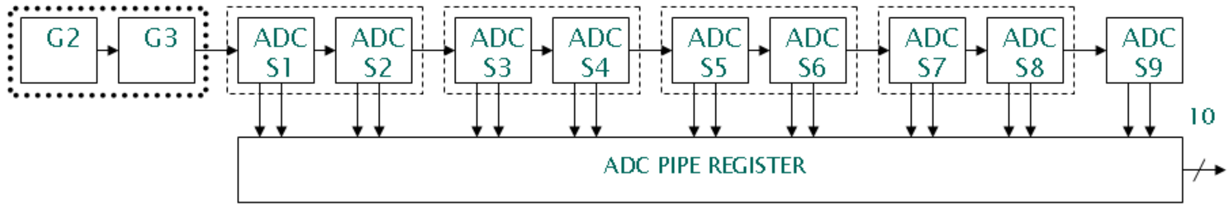


Fig. 4: Shared-opamp scheme for gain stages and 10-bit pipelined ADC.

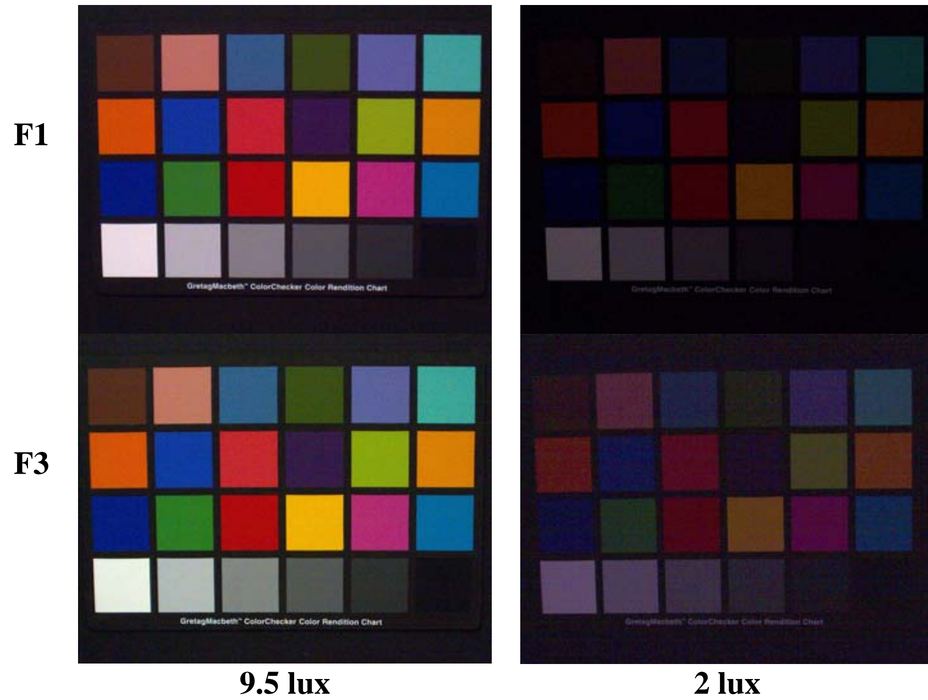


Fig. 5: Comparison of capture images.

Table 1: Variation configurations and corresponding readout noises.

F-CELL	ADC	Per-Column Amp	Spare Amp	G2/G3 shared-opamp	Total gain	Read noise* (e-)
F1	Common 10-bit shared-opmap ADC	Yes	No	Yes	16x	**2.82 e-**
F2		Yes	Yes	No	16x	**2.28 e-**
F3		No	Yes	Yes	16x	**4.21 e-**
F4		Yes	Yes	Yes	64x	**2.87 e-**

*** Measured at 16x total gain**

Continuous Time Column Parallel Readout for CMOS Image Sensor

G.G. Storm, M.D. Purcell, A. Laflaquiere, R.A. Elliott, L.A. Grant
T.Lule[1], F. Mutze[1], M.Sommer[1]

STMicroelectronics,Imaging Division,33 Pinkhill,Edinburgh, UK.Graeme.Storm@st.com +441313366233
(1) STMicroelectronics, Imaging Division, 12 rue Jules Horowitz, 28019 Grenoble, France

INTRODUCTION

As advances continue in process technology with features shrinking it is increasingly common for CMOS image sensors to contain pixels with dimensions below 2μm square. As the pixel size reduces, similarly the light sensitive area is reduced. Although this has been compensated for,to a degree, by an increase in the conversion gain, a reduction in the number of incident photons means the voltage swing for a given illumination has decreased. In a standard active pixel sensor architecture the pixel voltage is buffered via a source follower to the column bitline where it is sampled and converted to a digital word. Noise from the source follower, sampling and ADC all contribute to the total noise in the image.

Regardless of the process or design, a sampled system will be subject to kTC noise. If the signal swing from the pixel reduces for a given illuminatiion level, the sampling capacitor would need to increase by the square of the reduction to maintain the same SNR. A method of reducing the impact of kTC noise (and noise in subsequent stages) is to add an amplification stage into the column[1]. The design of such an amplification stage is obviously crucial so as not to introduce further noise but will unavoidably require extra silicon area.

This paper presents a column readout that operates without any sample and hold structure with an aim to reduce the readout noise whilst consuming a minimum of silicon area. The continuous time architecture has been fabricated as the readout for a 5Mpix CMOS image sensor and targetted towards a 12bit ADC resolution. The imaging array shares devices to give an effective 1.75 transistors per pixel[2] where the pixel size is 1.75μm in a 90nm minimum feature size technology.

Sensor and column architecture

The schematic of a single column with connected pixel is shown in Figure 1 where the capacitors are realised by metal-metal structures to achieve good linearity and matching. At the end of the set exposure period the RESET control signal to the pixel will fall to leave the ‘black’ or ‘reset’ level of the pixel on the floating diffusion node(FDN). This voltage is buffered by the pixel source follower to the column. During this time both amplifiers 1 and 2 in the column are held in their auto-zero state and the ramp is grounded. When the reset level of the pixel has settled in the column the AZ1 switch will first open causing charge injection onto the input node of the amplifier. By careful sizing of the AZ1 switch, input capacitors and amplifier gain, the output of the first amplifier can remain unsaturated allowing the input offset to be stored in capacitor C3.

After AZ2 has fallen the transfer gate in the pixel can be pulsed to transfer the light generated charge to the floating diffusion thus causing a similar drop in the column voltage and a reduced drop at the input of the first amplifier. When the column voltage has settled the DAC can be enabled to generate the RAMP which is applied to input capacitor CIN2. The capacitively coupled ramp will cause the input of the first amplifier to rise and at some point the output will flip. This flip will be cascaded through to the 2nd and third amplifiers and controls when the SRAM stores the count value. The READ signal to the addressed row will remain on for the duration of the ADC conversion[3] thus requiring the floating diffusion to maintain the light generated charge.

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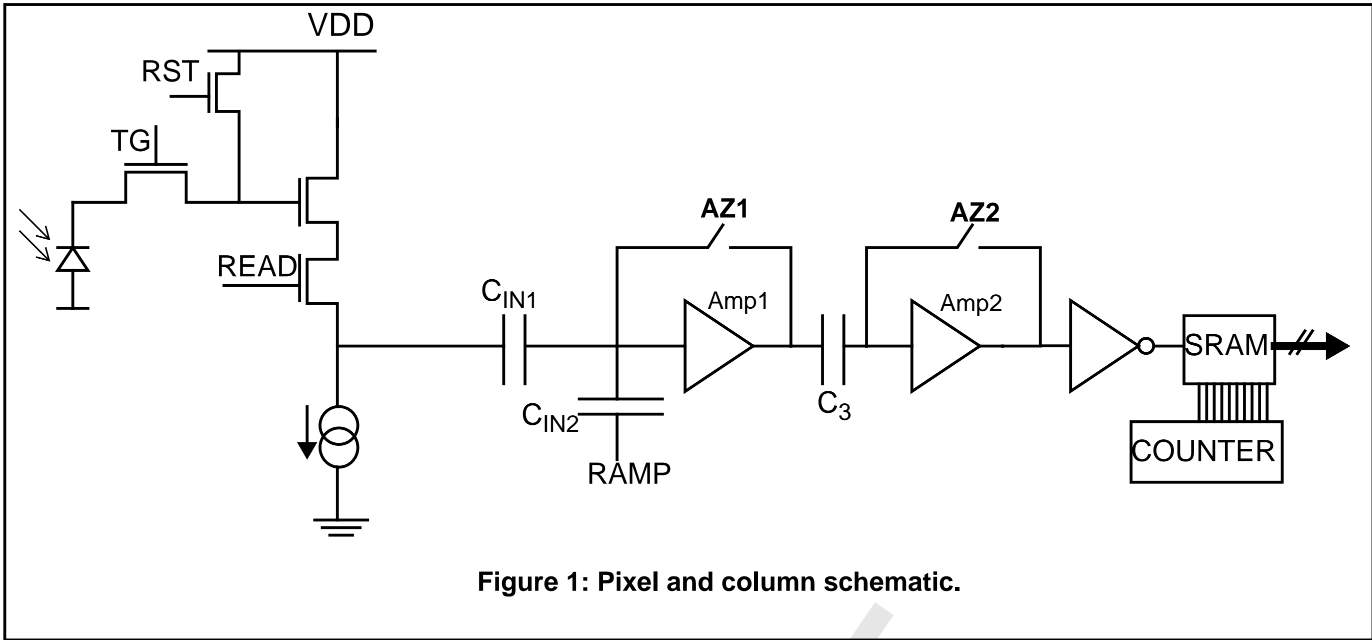


Figure 1: Pixel and column schematic.

The chip is composed of an array of 2640x1992 pixels arranged to share devices to give an effectice 1.75 transistors per pixel. Rows of pixels are addressed by a Y-decoder situated to the right of the imaging array and readout through top and bottom column parallel ADC's and SRAM. The SRAM output from the top and bottom are routed to the mid left of the chip and recombined before the parallel data is connected to pads. The power management circuitry including bandgap, charge pumps and DAC is situated to the right of the Y-Decoder. A ring oscillator is also included on chip to generate a high speed count which is sent to the SRAM and used to control the DAC. A chip plot is shown in Figure 5.

Readout of the imaging array is done with a rolling shutter type exposure. Opearting at a pixel clock of 80MHz allows 15fps and permits 33us to reset, read and convert addressed rows. At this data rate a DAC frequency of around 200MHz is required to achieve a true 12-bit conversion for the single slope ADC. Non-linear ramp schemes that exploit the characteristics of photon-shot noise to reduce the conversion time have been proposed[4][5]. However, a linear 12-bit conversion has been realised to maintain effective colour processing[6]. The ring oscillator was made programmable from 80MHz to just under 300MHz and the noise at different frequencies is shown in the measurements section.

Measurements

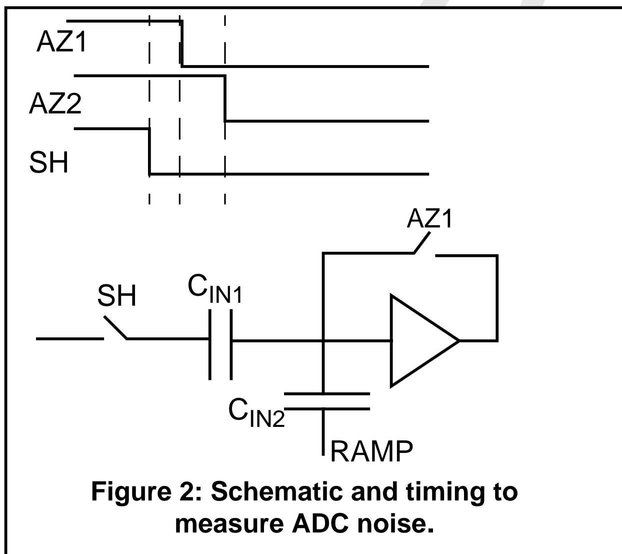


Figure 2: Schematic and timing to measure ADC noise.

The temporal noise contribution of different sections of circuitry in the readout chain was measured by applying different timing modes. To measure only the ADC noise it was necessary to add a sample and hold switch in series with C_{IN1} of the comparator. By sampling the 'reset' level of the pixel before AZ1 falls, the noise of the preceeding circuitry can be removed, leaving only ADC noise. It should be noted that the ADC conversion (mV/code) is different for sampled and continuous time operating modes.

The noise is plotted in Figure 3 for different DAC/SRAM speeds. The readout speed from the device was fixed at 48MHz to give approx. 9 frames per second. The Source follower noise was calculated from

$V_{NSF} = \sqrt{(V^2_{NTOT} - V^2_{NADC})}$ where V_{NTOT} is the total noise and V_{NADC} is the ADC noise.

It can be seen that the ADC temporal noise shows a gradual increase with the ADC/SRAM operating frequency. However a slight increase in the SF noise must also occur to account for the total noise. A thermal change may account for this increase.

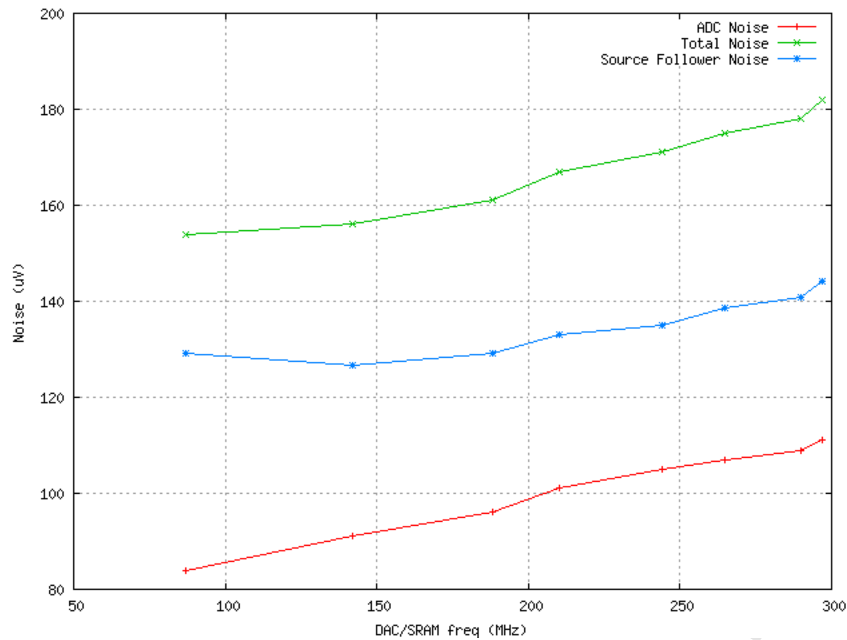
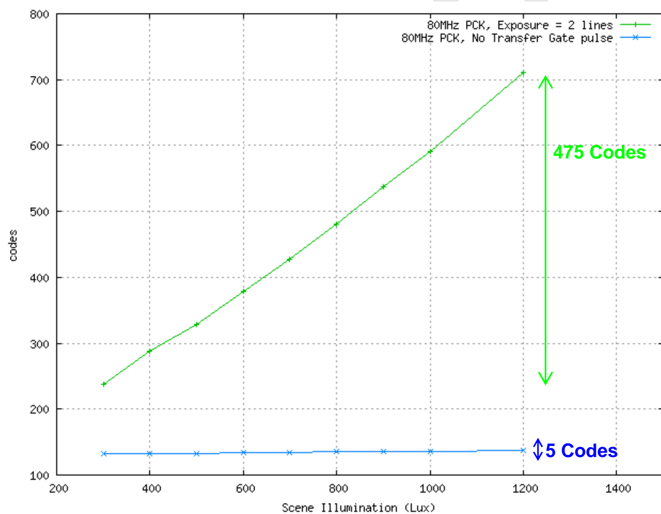
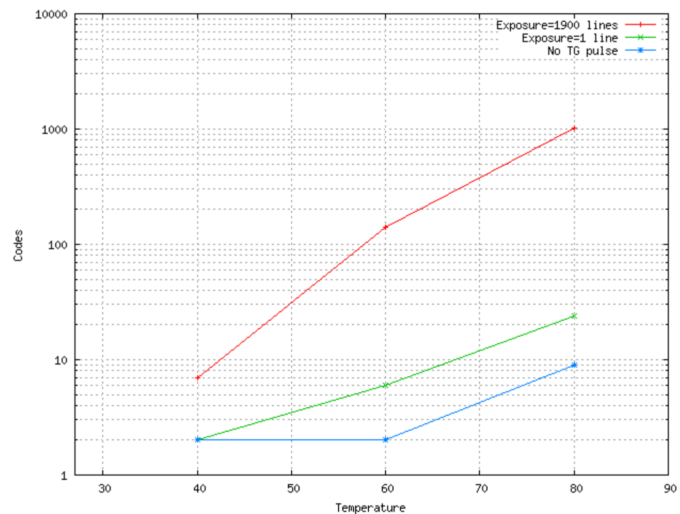


Figure 3: Plot of temporal noise v's Conversion speed.

An important consideration of the continuous time readout is how well charge is stored on the floating diffusion node. Since the voltage needs to be held for the duration of the ADC conversion it is important it is not degraded or corrupted. Illumination and temperature are two important parameters to consider. Since the floating diffusion is located in the pixel array it will be subject to the incident illumination. Microlens' if used will help direct light away from the FDN, however, in the same way that dark current increases with temperature, the leakage on the FDN will do likewise. The leakage is measured by disabling the transfer gate pulse. The plots of Figure 4 provide additional curves without the transfer gate disabled so that the leakage can be compared to the signal generated by the photodiode. The measurements were taken with a reduced ramp range so that one code is less than 8uV.



(a)



(b)

Figure 4: Plot of leakage on FDN (a) with scene illumination (80MHz PCK, image average) (b) with temperature(48MHz PCK, per pixel difference with image at 27deg).

Figure 4(a) compares an image with exposure of 2 lines with an image where the transfer gate is disabled. This worst case test condition shows the signal is still dominant over the leakage. Figure 4(b) provides the same comparison against temperature and shows the FDN leakage to have a much reduced effect compared to the dark current of the pixel.

Conclusion

We have presented a low noise readout architecture for a CMOS image sensor by removing the noise generated in a sampled system. The simplicity of the continuous time architecture allows for a compact layout of the column parallel readout. A full 12-bit linear slope for the ADC is achieved with a high speed DAC and SRAM.

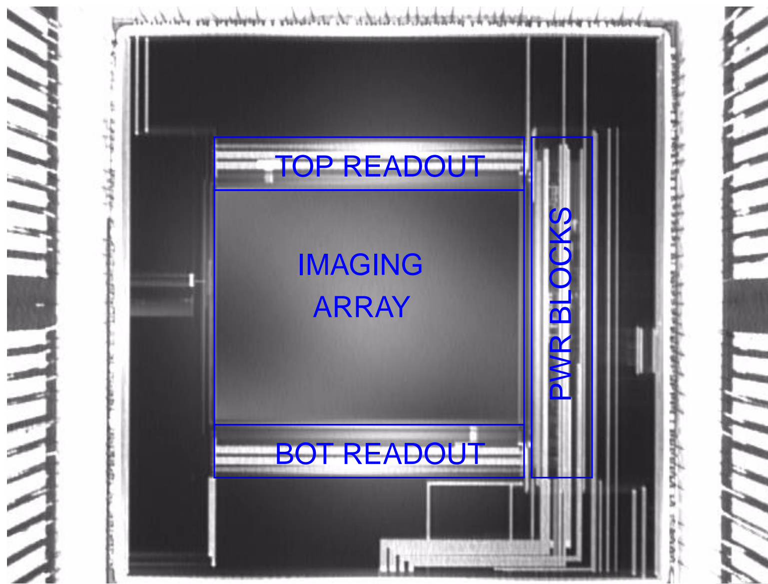


Figure 5: Test chip plot.

Parameter	
Pixel pitch	1.75um
Transistors/pixel	1.75
Array dimensions	2640x1992
Conversion gain at column bitline.	70uV/e$^-$
Full Well	600mV(8500e-)
Temporal Noise (G16) 210MHz DAC/SRAM -Total -SF -ADC	 167uV (2.4e-) 133uv (1.9e-) 101uV (1.4e-)
VFPN	10uV

Table 1: Imager Characteristics

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References

[1] A. Krymski, N. Khaliullin and H Rhodes, "A 2e$^-$ Noise 1.3Megapixel CMOS Sensor", in Proc. IEEE Workshop on CCD and AIS, Elmau, Germany, 2003.

[2] M. Mori, M. Katsuno, S. SKasuga, T. Murata, T. Yamaguchi, "A 1/4in 2M Pixel CMOS Image Sensor with 1.75Transistor/Pixel", in IEEE ISSC Dig. Tech Papers, pp110-111, Feb 2004.

[3] Y. Nitta, Y. Muramatsu, K. Amano, T. Toyama, J. Yamamoto, K. Mishina, A. Suzuki, T. Taura, A. Kato, M. Kikuchi, Y. Yasui, H. Nomura, N. Fukushima, "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor", in Proc. IEEE Solid-State Circuits conference, pp.500-501, 2006.

[4] M.F. Snoeij, A.J.P. Theuwissen, J.H. Huijsing, "A Low-Power Column Parallel 12-bit ADC for CMOS Imagers", in Proc IEEE Workshop on CCD and AIS, Nagano, Japan, 2007.

[5] T. Otaka, Y. Lee, T. Bales, P, Smith, J. MacDowell, S. Smith, I. Takayanagi, "12-Bit Column-Parallel ADC with Accelerated Ramp", in Proc IEEE Workshop on CCD and AIS, Nagano, Japan, 2007.

[6] R.W.G. Hunt, "The Reproduction of Colour", WILEY, 2004.

Analysis of Source Follower Random Telegraph Signal Using nMOS and pMOS Array TEG

Kenichi Abe[1], Shigetoshi Sugawa[1], Rihito Kuroda[1,4], Shunichi Watabe[1], Naoto Miyamoto[2], Akinobu Teramoto[2], Tadahiro Ohmi[2], Yutaka Kamata[3] and Katsuhiko Shibusawa[3]

[1]Graduate School of Engineering, Tohoku University, [2]New Industry Creation Hatchery Center, Tohoku University, 6-6-10, Aza-Aoba Aramaki Aoba, Sendai, 980-8579, Japan

+81-22-795-3977, fax: +81-22-795-3986, e-mail: k-abe@fff.niche.tohoku.ac.jp

[3]Miyagi Oki Electric. Co., Ltd., [4]JSPS Research Fellow (DC1)

***Abstract* - In this work, Random Telegraph Signal (RTS) in source follower circuits is studied using an advanced TEG including dependency on MOSFETs carrier type, gate size and operation bias conditions. Appearance probabilities and noise intensities of RTS for pMOSFETs are shown to be less problematic than these of nMOSFETs for various gate sizes and bias conditions.**

I. Introduction

It has been recently recognized that Random Telegraph Signal (RTS) noise occurs in source follower circuits in pixel is one of the most crucial contributor to the image quality degradation of deep sub-micron CMOS image sensors because it is difficult to be eliminated by noise reduction circuitry [1-2]. It has been reported that the RTS amplitudes become more significant as MOSFETs' gate size are scaled down [3-4]. Then, understanding of the physical origin of RTS and its suppression are of the urgent tasks for the further increase of image sensor performances, such as higher density, higher speed and wider dynamic range. To understand RTS occurrence mechanism, statistical analysis of RTS is indispensable. However, there is no efficient evaluation method of RTS until now. Then, this work employs an advanced Test Element Group (TEG) for evaluation of both nMOSFETs and pMOSFETs with total number of over 10^6 MOSFETs to statistically analyze RTS. Dependence of appearance probabilities of RTS in enormous number of MOSFETs on carrier type, gate size, gate overdrive voltage and substrate bias conditions are extensively studied using the TEG. And then, RTS parameters such as amplitude, mean time to capture ($<\tau_c>$) and mean time to emission ($<\tau_e>$) can be analyzed in a short time.

II. TEG Structure and Evaluation System

Fig. 1 shows circuit schematic of the TEG for nMOSFETs (a), pMOSFETs (b) and the picture image of TEG (c), respectively. Bias voltages V_{DD} and V_G are applied to all the measured MOSFETs simultaneously. The operating point of the measured MOSFETs can be controlled by the values of V_G and I_{DS}, where I_{DS} is the drain current of the current source transistors placed in every column and that is tunable by the value of V_{ref}. As shown in Fig. 1 (d), electrical characteristics of each MOSFET in the source follower circuit is obtained as V_{gs}, which is given by an output voltage V_{out} and a setting V_G under a constant I_{DS}. A large number of MOSFETs' characteristics can be measured in a very short time by scanning the values of V_{out} from each cell using the horizontal and vertical shift resistors. Variation of stationary electrical characteristics in the MOSFETs is observed from variation of time mean values of V_{gs}. Figs. 2 (a) and (b) show the result of the stationary V_{gs} variation under constant I_{DS} = 1μA, which can be assumed threshold voltage variation of MOSFETs included in the array TEG [5]. Random noise within a MOSFET is obtained by measurement of transition of V_{gs} in time-scale. A typical result of RTS is shown in Fig. 3. In this system, since I_{DS} is kept constant during a measurement, random noise in a MOSFET would account for the random signals in V_{gs}. Thus, higher and lower V_{gs} states that are indicated in Fig. 3 correspond to the captured and emission states, respectively. It is because that when a conduction carrier is trapped, a higher gate overdrive voltage is needed for a MOSFET to keep the drain current constant since the inversion layer carrier mobility is degraded as well as the number of the carriers becomes smaller due to the trapped carrier. Several gate sizes of both n- and pMOSFETs are included in the designed TEG that is summarized in Table 1, and manufactured by a 0.18 μm, 1 Poly 2 Metal standard CMOS technology.

III. Results and Discussions

Fig. 4 (a) shows the distribution of the standard deviations of the V_{gs} fluctuation for one MOSFET in time-scale (σ_R) obtained by measuring the continuous 300 outputs of each MOSFET of which sampling rate is 0.7 sec/cell. Fig. 4 (b) shows the time-domain V_{gs} behaviors of nMOSFETs at various σ_R points. In an image sensor system, RTS is more problematic when its amplitude (*A*)

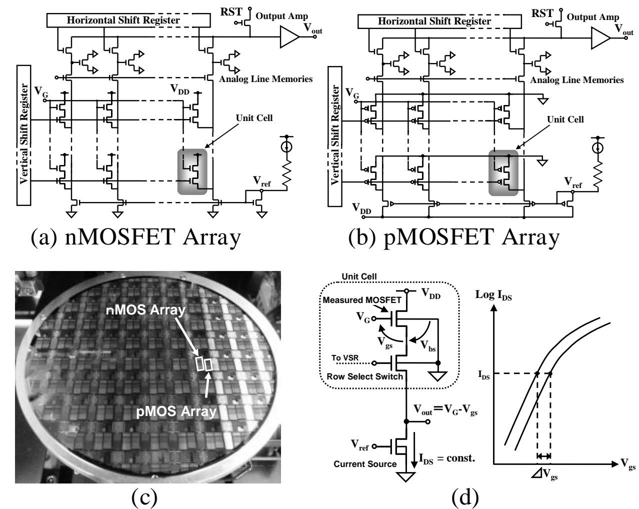

Fig. 1 (a), (b) Circuit schematics for n- and pMOSFET arrays, (c) picture image of TEG in a wafer and (d) method to measure electrical characteristics of MOSFET in the source follower circuits.

Table 1 Gate sizes and the number of MOSFETs manufactured in the n- and pMOSFET array TEG

Gate Length (μm)	0.22	0.22	0.24	0.24	0.4	1.2	1.2	1.2	
Gate Width (μm)	0.28	0.3	0.3	1.5	1.5	0.3	1.5	15	total
No. of nMOSFETs	131,072	131,072	131,072	131,072	131,072	65,536	65,536	16,384	802,816
No. of pMOSFETs	81,920	81,920	81,920	81,920	81,920	40,960	40,960	10,240	501,760

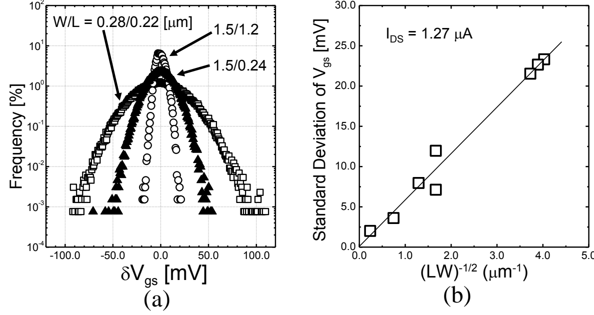

Fig. 2 (a) Distribution of stationary δV_{gs} which is difference value between V_{gs} of each MOSFET and the mean value of V_{gs} under constant I_{DS} = 1μA with various gate sizes for nMOSFETs and (b) dependence of the standard deviation of stationary V_{gs} variation on gate sizes.

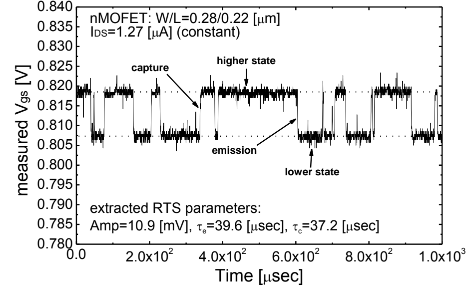

Fig. 3 V_{gs} behavior of a nMOSFET in time-scale. Constant I_{DS} of 1.27 [μA] is applied during the measurement. Signal transitions due to trapping and emission of a conduction carrier are indicated.

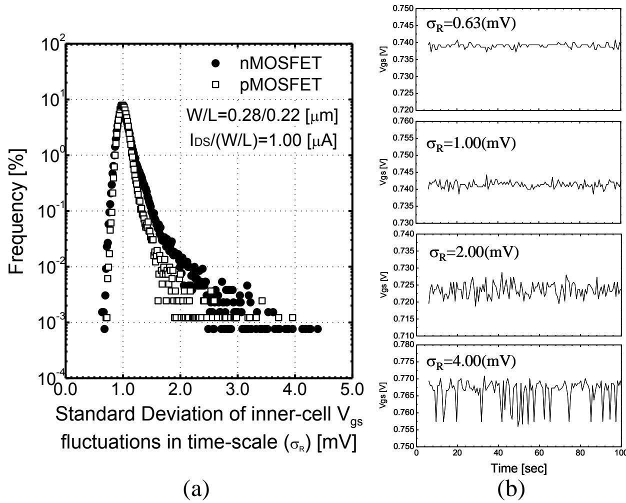

Fig. 4 (a) Distribution of the standard deviation of V_{gs} fluctuation for one MOSFET in time-scale of n- and pMOSFETs with W/L=0.28/0.22 [mm] and (b) time-domain V_{gs} behaviors of nMOSFETs with various σ_R when sampling rate = 0.7 sec/cell.

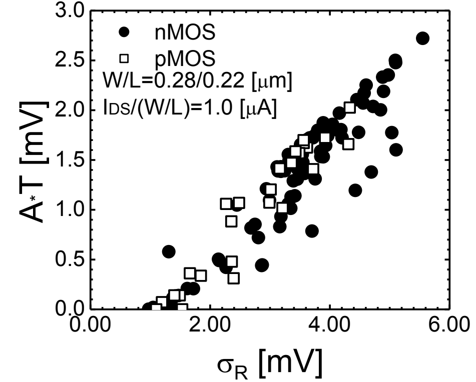

Fig. 5 Correlation diagram between σ_R and $A{*}T$ when sampling rate = 0.33 μsec/cell. A strong correlation is observed.

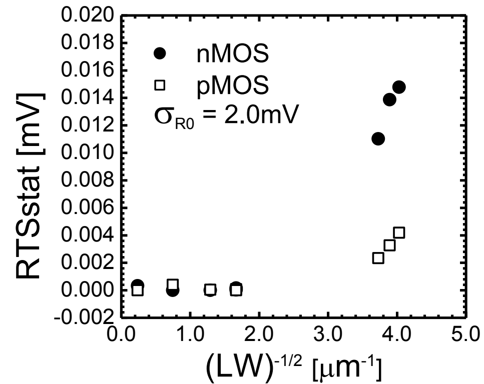

Fig. 6 RTS statistical indicator: *RTSstat* as functions of gate size for nMOSFETs and pMOSFETs for σ_{R0} = 2.0 [mV]. Results clearly show that pMOSFETs has smaller *RTSstat* than nMOSFETs.

become higher [6]. Here, signal transition probability is given by the following equation [7].

$$T = \frac{<\tau_e><\tau_c>}{(<\tau_e>+<\tau_c>)^2} \qquad (1)$$

where $<\tau_e>$ and $<\tau_c>$ are mean value of time-to-emission and time-to-capture for the trap to generate RTS, respectively. Then, $A{*}T$ is defined as a factor to characterize RTS noise intensity of a MOSFET. To examine the correlation between σ_R and $A{*}T$, we measured various MOSFETs and extracted A and T each MOSFET. Fig. 5 shows the correlation between σ_R and $A{*}T$. It is obviously shown that σ_R and $A{*}T$ have a strong correlation. Then, following parameter is defined as a statistical factor to evaluate RTS among MOSFETs with various gate sizes or bias points.

$$RTSstat = \sum_{\sigma_R=\sigma_{R0}}^{\infty} \sigma_R \cdot freq(\sigma_R) \qquad (2)$$

where σ_{R0} is a minimum value of the range of σ_R to be analyzed and $freq(\sigma_R)$ is the appearance probability corresponding to each σ_R. Fig. 6 shows the extracted *RTSstat* from the σ_R measurement results as functions of the gate size for n- and pMOSFETs. The results clearly show that *RTSstat* increases as gate size is scaled down. Moreover, pMOSFETs have smaller *RTSstat* than that of nMOSFETs for various gate sizes indicating that RTS is more problematic in nMOSFETs than pMOSFETs.

Fig. 7 shows the correlation between $A*T$ and stationary V_{gs} of each nMOSFET at $I_{DS}/(W/L) = 1\mu A$. The results show that the correlation is very small indicating that the origins of the RTS and stationary V_{gs} variation are not same.

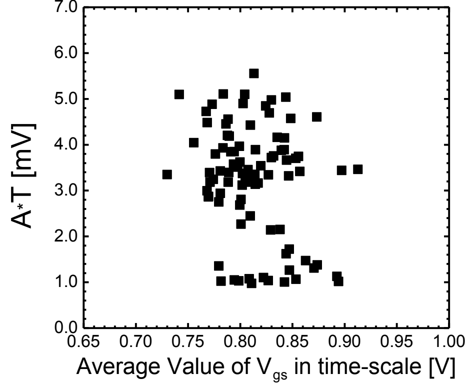

Fig. 7 Correlation between $A*T$ and stationary V_{gs} of each nMOSFET with W/L = 0.28/0.22 [μm]. The correlation is confirmed to be very small.

In addition to the gate size, RTS characteristics are analyzed for various bias conditions. Figs. 8 (a-e) show the RTS results of a nMOSFET and a pMOSFET at various I_{DS} and a fixed $|V_{bs}| = 1.0$ V. Figs. 9 (a) and (b) show the $<\tau_e>$, $<\tau_c>$ and RTS amplitudes as a function of I_{DS} for the n- and the pMOSFET with W/L = 0.28/0.22 μm. Figs. 10 (a) and (b) show Gumbel distributions in terms of σ_R for various I_{DS} for n- and pMOSFETs and Fig. 10 (c) shows *RTSstat* as a function of I_{DS}, respectively. The results show that as gate overdrive voltage increases, $<\tau_e>$ increases, $<\tau_c>$ decreases, the RTS amplitude decreases and RTS appearance probability of large σ_R cells decreases. Thus, *RTSstat* decreases as gate overdrive voltage increases as Fig. 10 (c) shows. Moreover, *RTSstat* of pMOSFETs are smaller than nMOSFETs in all the measured I_{DS}.

Figs. 11 (a-e) show the RTS results of a nMOSFET and a pMOSFET at various $|V_{bs}|$ and a fixed $I_{DS}/(W/L) = 1$ μA. Figs. 12 (a) and (b) show the $<\tau_e>$, $<\tau_c>$ and RTS amplitudes as a function of $|V_{bs}|$, Figs 13 (a) and (b) show Gumbel distributions in terms of σ_R for various $|V_{bs}|$ for n- and pMOSFETs and (e) shows *RTSstat* as a function of $|V_{bs}|$. The results show that as $|V_{bs}|$ increases, for the nMOSFET, $<\tau_c>$ decreases, $<\tau_e>$ increases and T

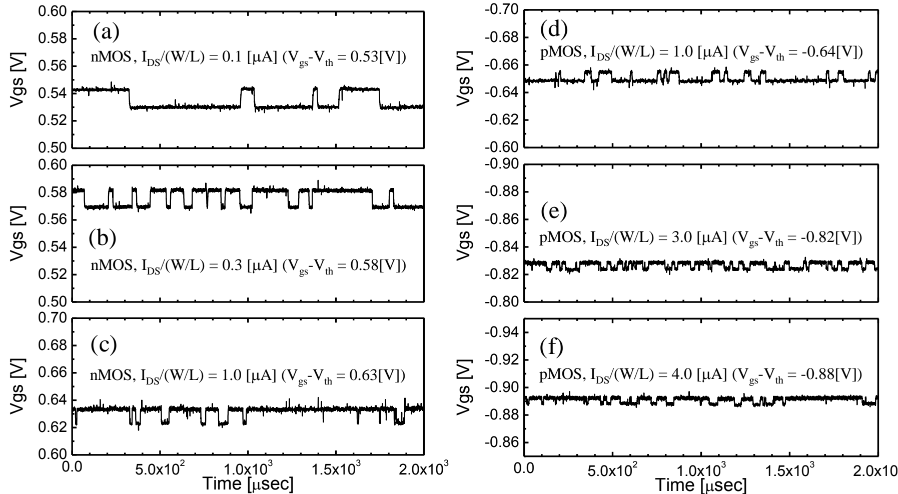

Fig. 8 Time-domain V_{gs} behaviors of nMOSFETs (a-c) and pMOSFETs (d-f) with gate size of W/L=0.28/0.22 [μm] for various I_{DS}, respectively. $|V_{bs}|$ during the measurements is 1.0 [V]. The results show that amplitudes of RTS decreases as I_{DS} increases. Also, probability of higher state (captured state) increased as I_{DS} increases.

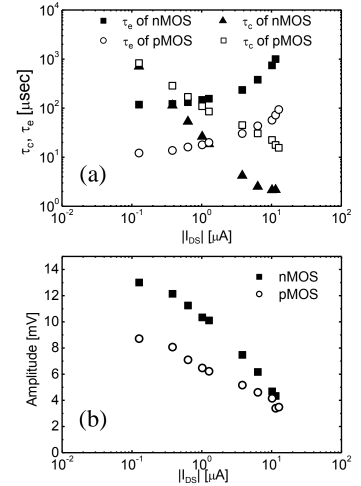

Fig. 9 (a) Capture and emission time constant, (b) RTS amplitude as function of gate overdrive voltage, respectively.

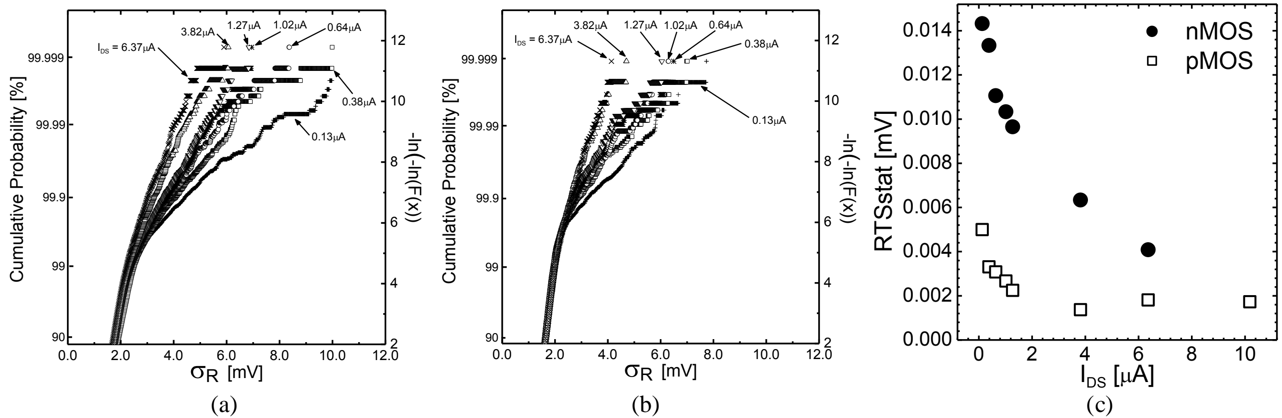

Fig. 10 (a) Gumbel distributions of the σ_R for nMOSFETs, (b) pMOSFETs and (c) shows the *RTSstat* as function of I_{DS} for n- and pMOSFETs.

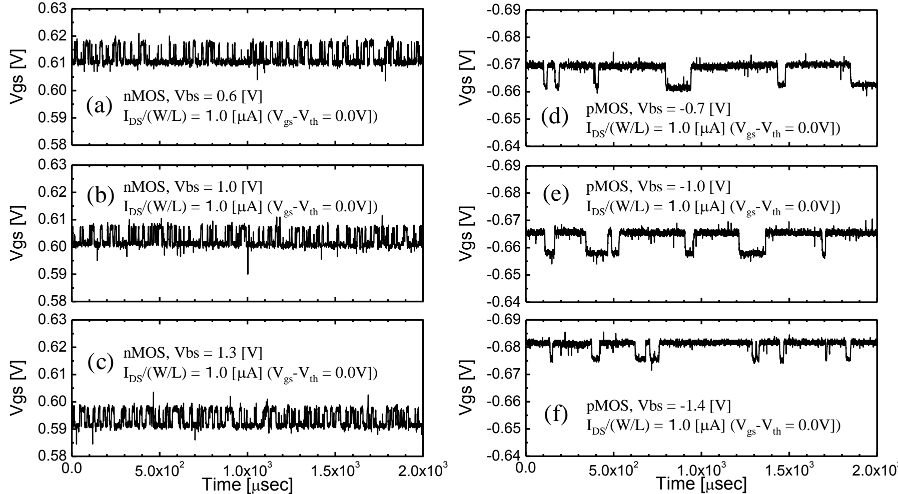

Fig. 11 Time-domain V_{gs} behaviors of nMOSFETs (a-c) and pMOSFETs (d-f) with the gate size of W/L = 0.28/0.22 [μm] for various $|V_{bs}|$, respectively, where I_{DS} during the measurements is 1.0 [μA] (at threshold voltage).

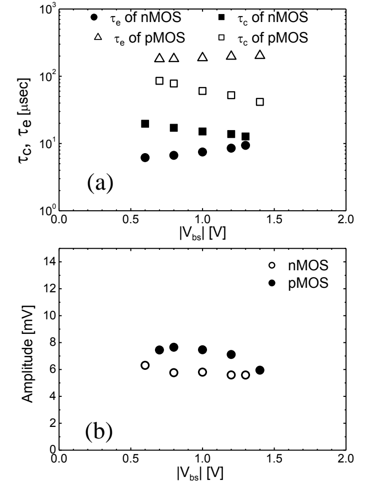

Fig. 12 (a) Capture and emission time constant and (b) RTS amplitude as functions of back substrate voltage(V_{bs}).

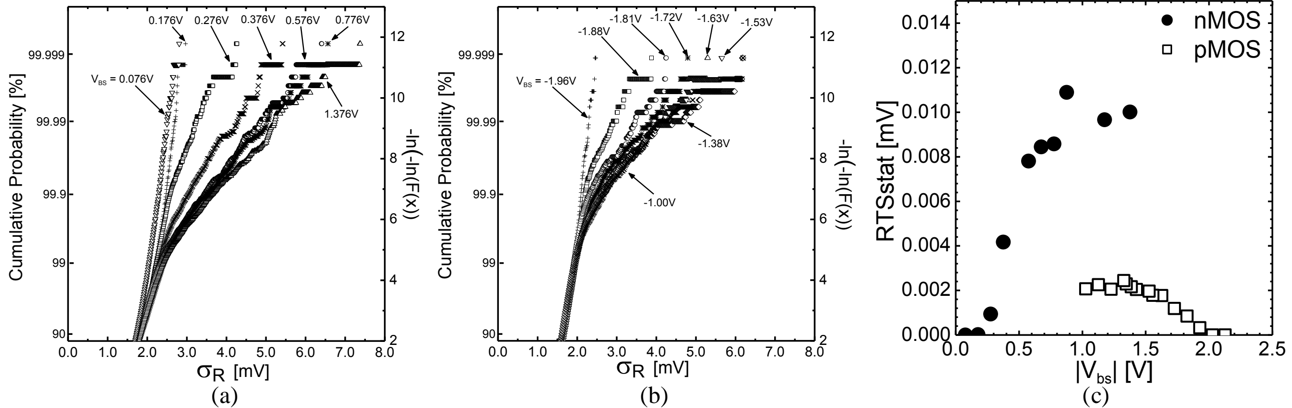

Fig. 13 (a) Gumbel distributions of the σ_R for nMOSFETs, (b) pMOSFETs and (c) shows the *RTSstat* as a function of $|V_{bs}|$ for n- and pMOSFETs.

increases. Also, as $|V_{bs}|$ increases, the RTS amplitude does not change much and RTS appearance probability of large σ_R cells increases. On the other hand, as $|V_{bs}|$ increases for the pMOSFET, $<\tau_e>$ increases, $<\tau_c>$ decreases and then T decreases. Also, as $|V_{bs}|$ increases, the RTS amplitude does not change much and RTS appearance probability decreases for pMOSFETs. Consequently *RTSstat* increases for nMOSFETs and decreases for pMOSFETs as $|V_{bs}|$ increases as Fig. 13(c) shows. Moreover, *RTSstat* of pMOSFETs are smaller than that of nMOSFETs in all the measured $|V_{bs}|$. These tendencies would indicate that energy level distributions of traps contributing to RTS are different for electrons and holes.

IV. CONCLUSION

In this work, Random Telegraph Signal in source follower circuits is statistically evaluated using the newly developed array TEG for characterizing nMOSFETs and pMOSFETs. The results obtained from more than 10^6 sample cells revealed the following four key findings.

1. RTS is severer in nMOSFET than in pMOSFET.
2. *RTSstat* increases as transistor gate size becomes smaller.
3. RTS appearance probability, RTS amplitude and *RTSstat* decrease as applied gate overdrive voltage increases for both nMOSFETs and pMOSFETs.
4. *RTSstat* increases for nMOSFETs and decrease for pMOSFETs as applied substrate voltage increases.

Findings obtained using the developed array TEG would give very useful information to the circuit design of highly noise tolerant image sensors. Moreover, statistical RTS measurement using the TEG would give an efficient evaluation of LSI manufacturing processes.

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REFERENCES

[1] J. Y. Kim et al., *IEEE Workshop on CCDs & AIS*, p.142, 2005.
[2] X. Wang et al., *IEDM Tech. Dig.*, p.115, 2006.
[3] A. Asenov et al., *IEEE Trans-ED*, **50**, 3, p.839, 2003.
[4] N. Tega et al., *IEDM Tech. Dig.*, p.491, 2006.
[5] S. Watabe et al., *JJAP.*, **46**, 4B, p.2054, 2007.
[6] C. Leyris et al., *Proc. 32nd ESSCIRC*, p,376, 2006.
[7] K. S. Ralls et al., *Phys. Rev. Lett.*, **52**, 3, p.228, 1984.

CONSIDERATION OF DARK CURRENT GENERATION AT THE TRANSFER CHANNEL REGION IN THE SOLID STATE IMAGE SENSOR

Yoshihisa Kunimi†, Bedabrata Pain‡

†Asahi Kasei EMD Corporation. 5-4960, Nakagawara-cho, Nobeoka, Miyazaki, 882-0031, JAPAN

Tel.: +81-982-22-5528, Fax: +81-982-22-5509, e-mail: kunimi.yb@om.asahi-kasei.co.jp

‡Jet Propulsion Laboratory, California Institute of Technology. 4800 Oak Grove Drive, Pasadena, CA 91109

Abstract

One interesting CMOS image sensor structure is proposed, which can suppress the inflow of dark current from the transfer channel region into buried photodiode. In this structure, P-type polysilicon is partially formed in the N-type polysilicon of transfer gate electrode. This structure becomes operative when dark current is drastically generated at the transfer channel region due to insufficient passivation of Si/SiO2 interface levels.

Introduction

CMOS image sensors are attractive devices because of their low power consumption and applicability for on-chip signal processing [1]. During the several decades, intensive researches focus on the improvement of their performance, especially dark current reduction. And nowadays, high quality images can be taken by putting a buried photodiode to use [2]. When buried photodiode structure is optimized for usage in each process technology, much attention has to be paid on the achievement of complete charge transfer. One of the solutions to accomplish it is to set down the threshold voltage of transfer transistor [3]. To make threshold voltage lower indicates lower doping concentration in the channel region. Generally, lighter impurity dope leads longer lifetime of minor carrier. Therefore, if dark current is generated in the channel region where doping concentration is low, it can easily flow into buried photodiode because of its longer mean free path. Fortunately, it is well known that one of the most effective ways to suppress the dark current generation in the transfer channel region is to passivate the interface levels at the Si/SiO2 interface by hydrogen or deuterium [4]. This passivation of interface level surely promises the reduction of the amount of dark current generation. But, if this passivation is insufficient or if desorption of hydrogen/deuterium occurs, dark electrons easily generate at Si/SiO2 interface and, again inflow into photodiode.

This paper proposes an interesting structure which can keep dark current lower even if interface levels are insufficiently passivated. Especially, one structure which can suppress the inflow of dark current from channel region into buried photodiode is proposed. Additionally, it also suggests that this structure has potential to make charge transfer period shorter.

Structure and Experimental

Prototype chip (Figure 1) was fabricated based on 0.35μm process technology. Its outline is listed in Table 1. Notable point in the proposed structure is that p-type polysilicon partially exists at the edge of n-type polysilicon of the transfer transistor's gate electrode. Process sequence is shown in Figure.2, and cross section of transfer gate electrode was observed by both Scanning Capacitance Microscopy (SCM) and Tunnel

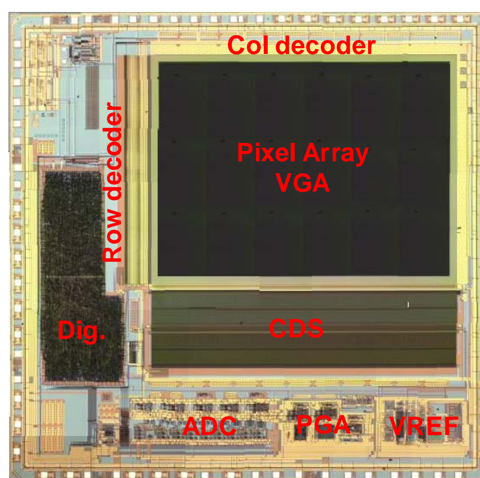

Figure.1, Photograph of VGA CMOS Image Sensor. (ES chip)

Electron Microscopy (TEM), as shown in Figure 3, simultaneously. For the consideration of dark current at the transfer channel region, 2 kinds of transfer gate electrodes were prepared; (S1) transfer gate consists of entire all n-type polysilicon, (S2) transfer gate polysilicon has partially p-type polysilicon in n-type one. Then, these 2 kind structures were treated under the 3 different process conditions, respectively; (A) interface level passivation process wasn't done, (B) interface level passivation treatment was done, but it was insufficient, (C) interface level was sufficiently passivated by hydrogen. Measurement results are summarized in Table.2. These results indicate that, if interface level at Si/SiO2 interface is insufficiently passivated, the amount of dark current generated at transfer channel region is larger, but partially p-type polysilicon gate can suppress the inflow of dark current into photodiodes to make dark current lower. In contrast, if interface level is sufficiently passivated, obvious suppression of dark current inflow can't be observed because the amount of dark current generation around transfer channel region is very small. Next, potential profile along the transfer channel was simulated by process / device simulators. Process simulation was done by TSUPREM-4, and device one by Medici. Simulated potential profiles in the silicon substrate, especially potential profiles around transfer channel region, are shown in Figure.5; (P1) is potential profile when the width of P-type polysilicon region in gate electrode is narrower, (P2) is when that is wider. These results indicate that the existence of P-type polysilicon in the N-type polysilicon gate electrode causes the potential gradient in the transfer channel region. Furthermore, the width of p-type polysilicon region is wider, potential gradient is widespread. In other word, wider p-type electrode can make dark electrons tend to flow away from photodiode region. Therefore dark current accumulated in buried photodiode can be kept lower. This is also explained by using illustrations shown in Figure.6. This structure

Figure.2, process sequence for parital p-type polysilicon formation in the transfer gate.

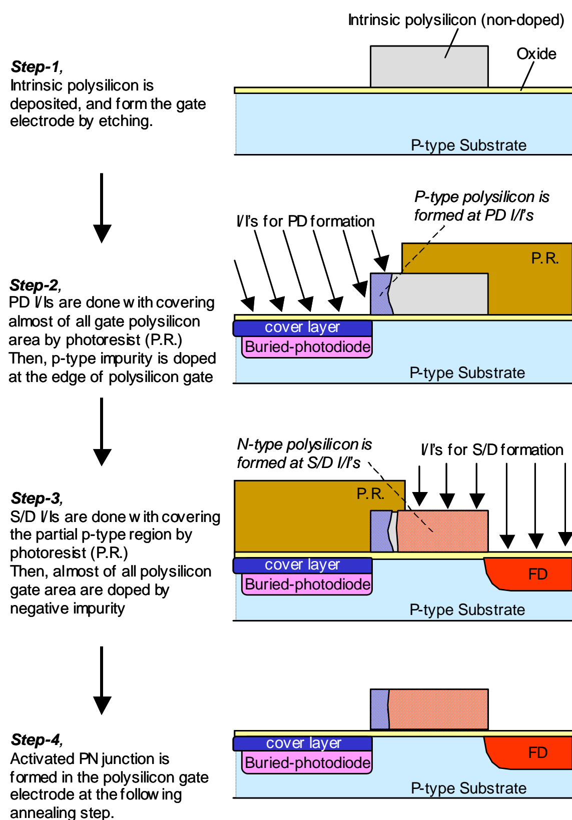

Table.1 Outline of prototype chip

Sensor Technology	CMOS / 4T
Optical format	1/4-inch VGA
Pixel pitch	5.6 μm x 5.6 μm
Color filter array	R,G,B, Bayer pattern
Process rule	0.35 μm 2P3M CMOS
Frame rate	30 fps
Shutter	Electric rolling snap
ADC	On-chip 10-bit
Supply voltage	Analog: 2.7 V to 3.6 V

Table.2 Measurement results of dark electrons at 25C

Transfer gate poly	Entire all N+ polysilicon (S1)	Partially P-type (S2)
(A); No passivation	197 e-/sec.	176 e-/sec.
(B); Insufficient passivation	123 e-/sec.	115 e-/sec.
(C); Enough passivation	43 e-/sec.	45 e-/sec.

can give us a help to reduce the amount of dark current in cmos image sensor, and can give us better quality image, as shown in Figure.4.

But, if the width of P-type polysilicon region is too wide, the extraction of electrons from buried photodiode to transfer channel during the charge transfer period becomes more difficult. It leads big image lag. It is necessary to optimize not only the width of p-type region but also the impurity profile of buried photodiode, carefully.

Additionally, potential gradient in the transfer channel region might also contribute to making the charge transfer faster. Specifically, potential gradient causes the drift diffusion of electrons in the transfer channel region. Therefore charge transfer can be done during the shorter period. Furthermore, when transfer channel is turn ON into OFF, this potential gradient can push the signal electrons in transfer channel toward FD region. That is, this structure can also contribute to the reduction of image lag; especially suppression of spill back of electrons from transfer channel to photodiode.

Conclusions

Partial existence of P-type polysilicon in N-type transfer gate polysilicon electrode is considered in this paper. Measurement results imply that it might contribute to the suppression of the inflow of dark current generated at transfer channel region into buried photodiode. It is due to the potential gradient in the transfer channel. And this unique structure has potential to make charge transfer faster. Additionally it might suppress the spill back of the signal electrons into photodiode when the transfer channel turns ON into OFF.

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References

[1] E.R.Fossum, "CMOS Image Sensor: Electronic Camera on A Chip", IEDM Tech. Dig., p17, 1995

[2] N.Teranishi, et.al. "An Interline CCD Image Sensor with Reduced Image Lag", IEEE Trans. Electron Dev., p1829, 1984

[3] I.Inoue, et.al. "New LV-BPD (Low Voltage Burried Photo-Diode) for CMOS Imager", IEDM Tech. Dig., p883, 1999

[4] K.Cheng, et.al. "A New Technique to Quantify Deuterium Passivation of Interface Traps in MOS Devices", IEEE Elect. Dev. Lett., p203-205, 2001

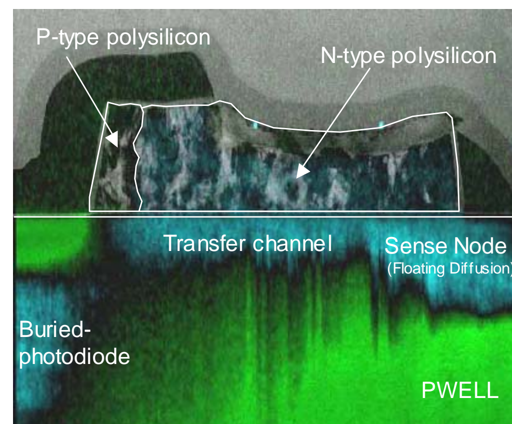

Figure.3, Cross-sectional image of Transfer-Transistor in 4T/CMOS image sensor. This image was obtained by combining a TEM image with a SCM (Scanning Capacitance Microscopy) image.

Figure.4, A captured image.

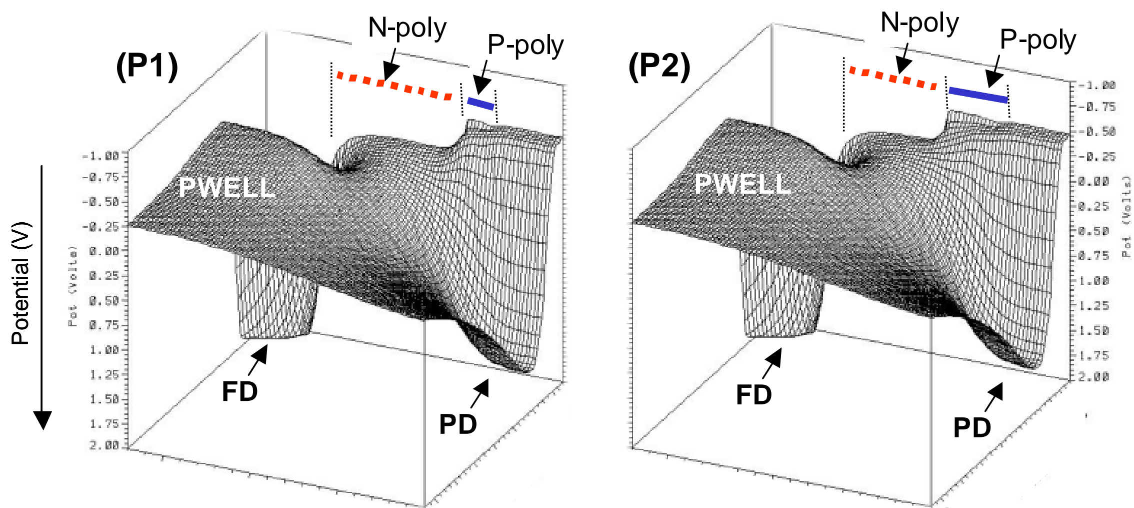

Figure.5, Simulation results of potential distribution in the Si-substrate, especially around the transfer channel region. (A) Potential distribution when the width of P-type polysilicon in the transfer gate electrode is 0.05 μm. (B) Potential distribution when width of P-type polysilicon is 0.30 μm.

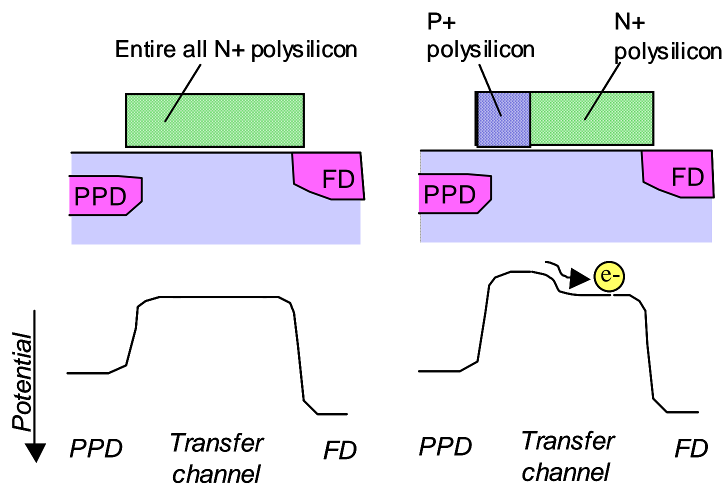

Figure.6, The upper left is a cross sectional image of transfer transistor whose gate electrode consists of entirely N+ polysilicon, and the lower left is horizontal potential profile image in transfer channel. The upper right is a cross sectional one which has partial P-type region in the N+ polysilicon electrode, its transfer channel potential is shown at the lower right.

Gamma-Ray Irradiation Effects on CMOS Image Sensors

in Deep Sub-Micron Technology

Padmakumar R. Rao[1], Xinyang Wang[1], Adri J. Mierop[2], and Albert J.P. Theuwissen[1,2] (IEEE Fellow)
[1]Electronic Instrumentation Laboratory, Delft University of Technology,
Delft, the Netherlands
[2]DALSA, Eindhoven, the Netherlands
email: p.ramachandrarao@tudelft.nl, Ph: +31152781602, Fax: +31152785755

INTRODUCTION

CMOS Active Pixel Sensors (APS) excel in domains that include low power operation and on-chip integration of analog and digital circuitry. Since these sensors are utilized for applications involving the detection of signals as low as a few electrons, radiation tolerance of such devices is of primary concern. All possible radiation effects are usually grouped into three basic types: transient effects (not dealt in this study), ionization damage and displacement damages [1], [2], [6]. Ionization damage has been considered to be the dominant mechanism when energetic photons (γ and X-rays) interact with solid-state matter. The major concerns due to this damage are charge build-up in the gate dielectric and radiation induced interface states. The introduction of discrete energy levels at the *Si-Si0*$_2$ interface leads to increased generation rates and thus higher surface leakage currents. Similarly, displacement of lattice atoms in the bulk leads to modified minority carrier lifetimes and increased bulk-generated leakage currents [2], [3], [4], [5].

EXPERIMENTAL

"Pinned" CMOS photodiodes (Fig. 1) utilize a p^+ pinning layer that shields the photodiode from surface effects that contribute to the leakage mechanism. The doping of the layers are chosen such that the photodiode is depleted completely. One of the most dominant dark current mechanisms in these structures are the defective sidewalls and the edges of shallow trench isolations (STIs) separating the photodiodes [9], [10]. To test the effects of radiation, test-structures with and without p-well protected STIs (Shallow Trench Isolation) were fabricated in Philips' 0.18-μm CMOS technology (Table. 1). The gap between the STI and the photodiode is represented by the parameter NTA. The structures were tested by irradiating them with γ-rays (1.17 MeV, 1.33 MeV); dose rate of 75.9 Gray/min.

Solving the continuity equation of a usual p^+/n photodiode derives an analytic model for the internal spectral response of pinned photodiodes. An equivalent diode reverse voltage V_d, is used to represent the depleted diode. The contribution from the p-type epitaxial region is included for the contribution from carriers collected through diffusion. This model is used to estimate the optical degradation of the sensors due to irradiation. Standard CMOS process parameters have been used for the simulation.

The dispersive transport phenomenon in the SiO_2 can be modeled on the concept of *small polaron hopping*, called as CTRW (continuous-time random walk). The transport process varies with the fourth power of the oxide thickness rendering modern deep sub-micron process ($t_{ox} \approx 4\ nm$) radiation hard to ionization damage in the gate regions. We provide results that suggest that the degradation of the STIs due to irradiation is an important factor influencing the sensor performance in advanced technological processes where very thin oxides and small geometries are employed. The histograms of the dark signal of the sensors (Fig. 2 - 5; all different horizontal scales) reveal that the radiation-induced degradation mechanism is sensitive to the nature and the location of the STI. The largest degradation is seen in structures that have unprotected STIs (Fig. 6). Further, structures that have the STI closer (NTA = 0.2 μm) to the photodiode is seen to degrade faster than the structures that have the STI further apart (NTA = 0.3 μm). Since the doping density of the p-well region is relatively higher than that of n-type region of the photodiode, the STI is isolated from the depletion region during integration for structures with p-well protection [11]. This explains the lower dark signal from these structures, and also the slower degradation of these structures to irradiation. The Arrhenius plot of the dark current (Fig. 7), shows that the radiation process introduces levels in the band-gap that tends the activation energy towards $E_g/2$, conforming to a generation-recombination mechanism. A plot of the activation energies of some 1000 pixels as a function of dark current (Fig. 8) reveals a field-enhancement phenomenon that results in pixels with lower activation energies to exhibit larger leakage currents [4], [5], [7]. We have characterized this effect in a separate study [8]. Fig. 9 shows the normalized spectral response (sensors output

(DNs)/calibrated sensor output (A)) of radiated as well as un-irradiated sensors and the fit based on the model. The equivalent reverse voltage V_d for the model was found to be 1.2 V resulting in a total depletion width of ~ 1.6 μm. A very good fit for all the curves is obtained by using an attenuation factor ξ_i (acting through the front layer optical stack) as well as the term for surface recombination velocity, *s*. The change in the parameters ξ_i and *s* extracted through the model indicates monotonic optical stack as well as interface degradation for the dose range considered. High energy rays such as γ-rays change the properties of the materials they penetrate and mainly interact through electronic excitation, electronic ionization and atomic displacements. As a result, color centers are introduced in the material [12]. A change in the absorption characteristics of top layer optical stack can explain the attenuation observed. From Fig. 9, a smoothening of the sharp peaks found in the un-irradiated devices can be seen on radiated devices which can also be explained by this hypothesis. The variation of the lifetime in the epi-layer does not have much effect in the present sensor, with a thickness of ~ 4 μm.

CONCLUSION

1. The results indicate that p-well protected STI structures are inevitable for radiation-hard designs. A larger value of NTA results in higher immunity to radiation damage, but should be optimized to avoid loss of sensitivity and pixel saturation levels. 2. Radiation induced leakage mechanism is sensitive to field-enhancement processes, so efforts should be directed to reduce this effect especially in deep sub-micron technologies. 3. The results highlight the need to further study the changes in top-layer material characteristics due to radiation process, to improve sensor quality for future high-quality image sensing in harsh environments.

ACKNOWLEDGEMENTS

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REFERENCES

[1] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, “Total Dose and Displacement Damage Effects in a Radiation-Hardened CMOS APS”, *IEEE Trans. Elec. Dev,* 50(1), pp. 84–90, January 2003.

[2] C. Claeys and E. Simon, “Radiation Effects in Advanced Semiconductor Materials and Devices”. *Springer Series in Material Science*, 2002.

[3] E. S. Eid et al., “Design and Characterization of Ionizing Radiation-Tolerant CMOS Image APS Image Sensors 30 MRad (Si) Total Dose”, *IEEE Trans. Nucl. Sci.*, 48(6), pp. 1796–1806, 2001.

[4] G. R. Hopkinson, “Radiation Effects in a CMOS Active Pixel Sensor”, *IEEE Trans. Nucl. Sci.*, 47(6), pp. 2480–2484, December 2000.

[5] J. Bogaerts, *“Radiation-Induced Degradation Effects in CMOS Active Pixel Sensors and Design of a Radiation Tolerant Image Sensor”*, PhD thesis, pp. 5–15, 37–95, Katholieke Univ. Leuven, April 2002.

[6] X. T. Meng, A. G. Kang, J. H. Li, H. Y. Zhang, S. J. Yu, and Z. You, “Effects of Electron and Gamma-ray Irradiation on CMOS Analog Image Sensors”, 43, pp. 1151–1155, *Microelectron. Reliab.* 2003.

[7] M. Cohen, J. P. David, “Radiation-Induced Dark Current in CMOS Active Pixel Sensors”, *IEEE Trans. Nucl. Sci.*, 47(6), pp. 2485-2491, December 2000.

[8] X. Wang, P. R. Rao and A. J. P. Theuwissen, “Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels”, *Proc. ESSDERC.*, pp. 331–334, September 2006.

[9] C. R. Moon, J. Jung, D. W. Kwon, J. Yoo, D. H. Lee and K. Kim, “Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors”, *IEEE Elec. Dev. Lett.*, Vol. 28, No. 2, pp. 114–116, February 2007.

[10] L. S. Riley, S. Hall and J. Schitz, “Evaluation of Surface Generation Velocity of Sidewall Oxide Interfaces Formed by Dry Etching for Shallow Trench Isolation”, *Sol. St. Elec.*, Vol. 44, No. 11, pp. 2093–2095, November 2000.

[11] H. I. Kwon, I. M. Kang, B. G. Park, J. D. Lee and S. S. Park, “The Analysis of Dark Signals in the CMOS APS Imagers From the Characterization of Test Structures”, *IEEE Trans. Elec. Dev.*, Vol. 51, No. 2, pp. 178–184, February 2004.

[12] K. Arshak , O. Korostynska, “Gamma Radiation–induced Changes in the Electrical and Optical Properties of Tellurium Dioxide Thin Films”, *IEEE Sensor Journal*, Vol. 3, No. 6, December 2003.

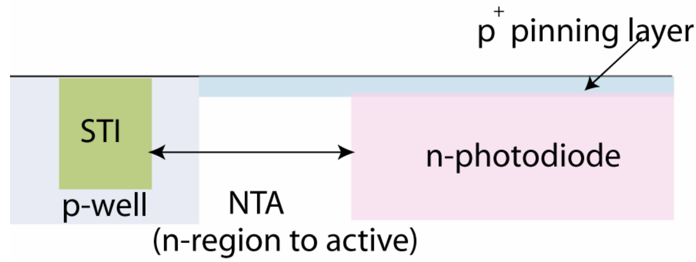


Figure 1: Layout schematic of the pixels.

Parameter	Value
Pixel pitch	3.5 µm
Conversion gain (g) (photon shot-noise method)	39.7 $\mu V/e^{-}$
Transfer gate length	0.6 µm
Operating voltage	3.3 V
Integration time	6.4 ms

Table 1: Sensor and measurement details.

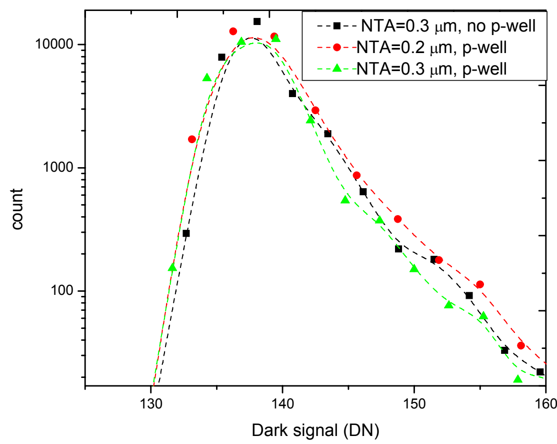


Figure 2: Histogram of the dark signal for the unradiated sensors.

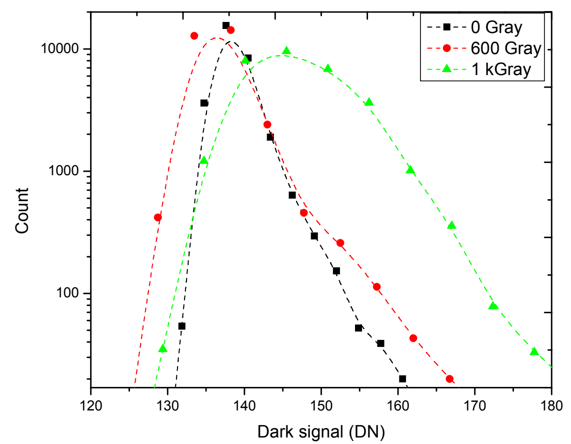


Figure 3: Histogram of the dark signal for sensor with NTA=0.3 µm, p-well protected.

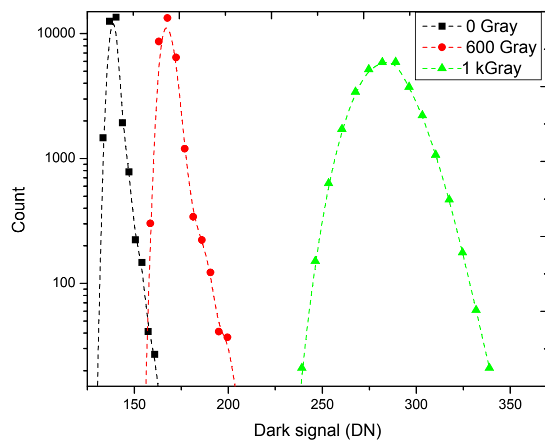


Figure 4: Histogram of the dark signal for sensor with NTA=0.2 µm, p-well protected.

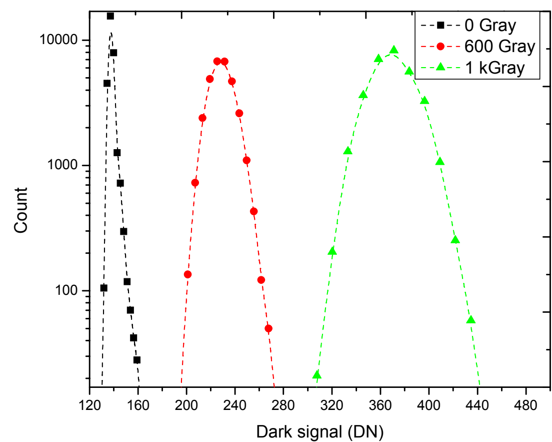


Figure 5: Histogram of the dark signal for sensor with NTA=0.3 µm, no p-well protection.

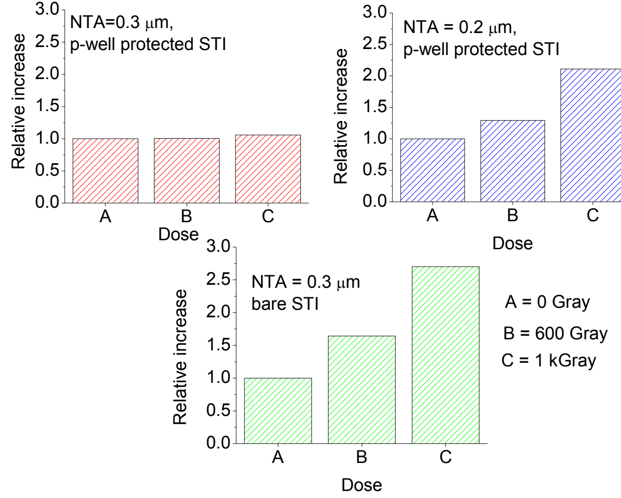


Figure 6: Relative increase in the mean dark signal of the sensors.

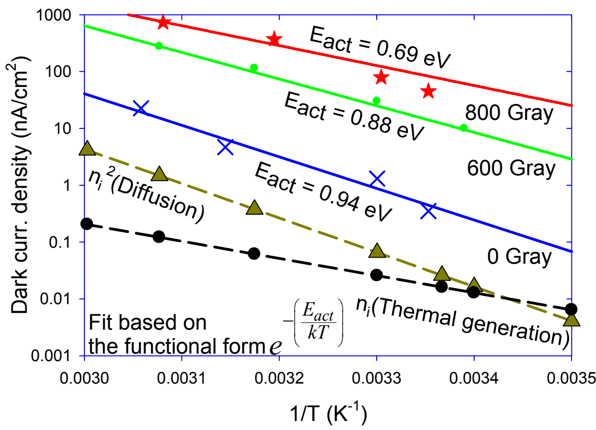


Figure 7: Arrhenius plot of the dark current of sensor (NTA=0.3 μm, no p-well).

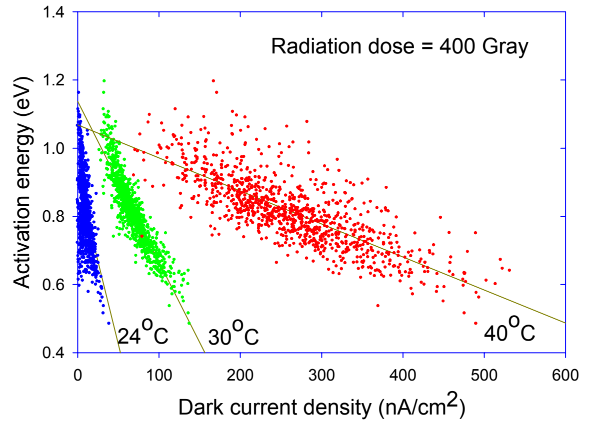


Figure 8: Leakage current vs. activation energy of 1000 pixels (NTA=0.3 μm, no p-well).

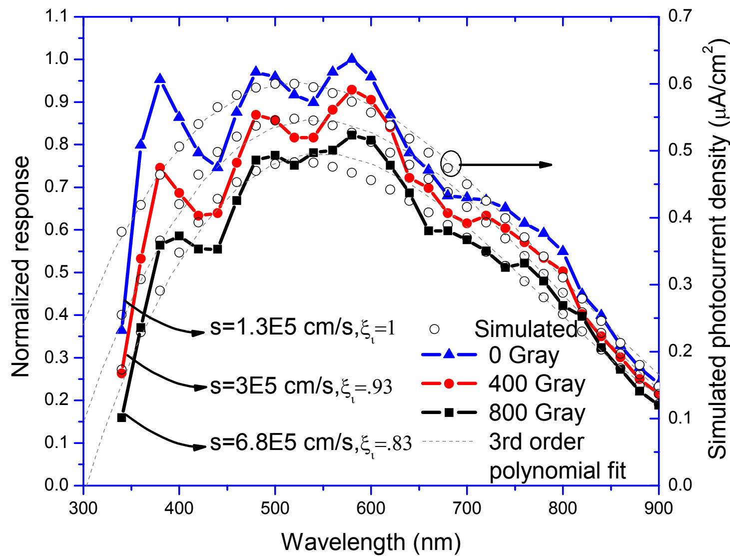


Figure 9: Normalized spectral response of radiated and unradiated sensors (NTA=0.3 μm, no p-well) as a function of wavelength and the fit.

1.4Gpix/s, 2.9Mpix CMOS image sensor for readout of holographic data memory

Roel Aerts, Steve Domer, Judy Fong, Kellie Vanda, Ray Rubacha, Brannon Harris, Tomas Geurts and Manuel Innocent
Cypress Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
Roel.Aerts@cypress.com tel +32 15 446 333, fax +32 15 448 780

This paper presents a high speed CMOS image sensor for a high-end holographic data storage application. For this emerging application, high performance primarily translates into a high data throughput which requires a high frame rate. A high frame rate requires both a short readout time and a short integration time, which implies high sensitivity. This performance needs to be obtained at a moderate power consumption to limit the self heating of the sensor.
The presented sensor is a high sensitivity image sensor of 1696 by 1710 pixels that operates at 485 fps. The sensor contains 64 on-chip 8 bit ADCs operating at 26 Msamples/s each, resulting in an aggregate pixel rate of 1.4 Gpix/s. The outputs of the 64 ADCs are multiplexed onto 32 LVDS serial links operating at 416 Mbit/s each resulting in an aggregate date rate of 13.3Gbit/s. The sensor is designed in a standard 0.25µm CMOS process and consumes 1.1W in normal operation.

1. Introduction

Contrary to traditional optical data storage devices like e.g. CDROM, that read one bit of data at a time, holographic storage devices obtain a high data transfer rate by reading complete holograms containing over a million bits in a single operation. At the same time they achieve a high storage capacity as hundreds of these holograms can be stored in the same volume of material. Holographic data storage is expected to be a huge step forward in both speed and storage capacity of optical storage devices.

A high speed image sensor is the key component for building such a holographic data reader. The most important specification for the sensor is the high data throughput, which relates directly to the data read throughput of the holographic memory. A high data throughput requires both a short integration time and a short readout time. A short integration time requires high quantum efficiency and a high conversion gain since typically the amount of incoming light is small. A short readout time is obtained by having a high number of parallel readout paths. On the other hand, holographic data storage poses only moderate requirements on the image quality as it is basically reading a binary image.

This paper presents, to our knowledge, the first image sensor that is custom designed for emerging market of holographic data storage. It achieves 485 fps for an array of 2.9Mpix resulting in an aggregate pixel rate of 1.4Gpix/s. Given the massive data rate, the power consumption needs to be kept at a reasonably low level to avoid performance degradation due to self heating. The sensor contains on-chip all required functionality for easy system integration, but stays targeted to its key specification: high frame rate, high sensitivity and low power.

The next sections discuss the sensor architecture, the pixel, the ADC, the high speed serial link and the measurements.

2. Sensor architecture

The sensor is an autonomous system that interfaces with its host through a 10Mbit/s bi-directional serial command interface, a 208 MHz LVDS input clock signal, an output clock signal, a synchronization channel and 32 416 Mbit/s LVDS data downlink channels with an aggregate date rate of 13.3Gbit/s. LVDS is emerging as an interface of choice for image sensors [1,2] since it allows a very high data rate with a limited number of pins. All required clock, control and bias signals are generated on-chip. The incoming high speed clock is divided to generate the different low speed clocks required for the operation of the sensor. The sensor generates all its bias signals from a bandgap reference. An on-chip sequencer generates all the required control signals for the image core, the ADCs and the on chip digital data processing path. The settings of the sequencer are stored in registers that can be programmed through the serial command interface. The sequencer supports windowed readout at frame rates up to 10000 fps. The sensor operates in slave mode where the exposure is triggered by the host.

Figure 1 shows the floorplan of the sensor.

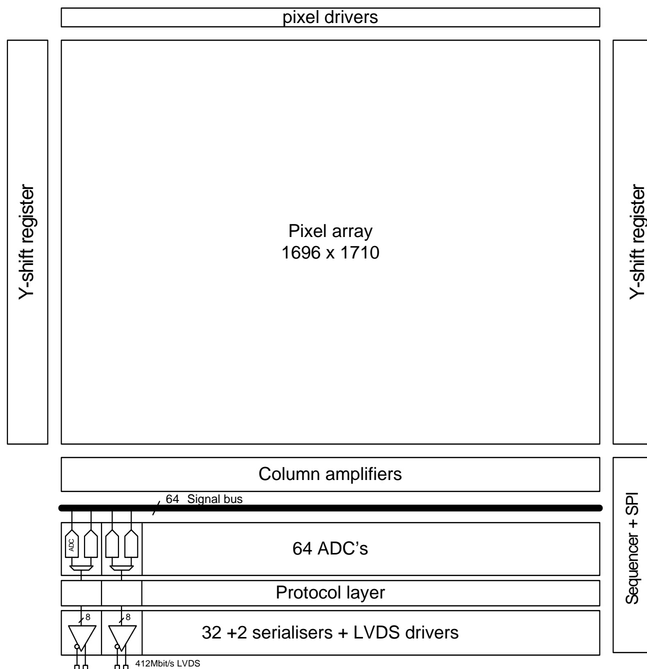


Figure 1: Floorplan of the sensor. The global pixel array control signals are driven from the top, while the high speed read-out related signals are driven from the two sides in parallel. The ADCs and serial links are organized in 32 identical blocks, each containing two ADCs together with the one serial link on which their outputs are multiplexed.

3. 6T pixel

The sensor has 6T pixels with an N-well photo diode and a storage capacitor. Figure 2 shows the pixel schematic.

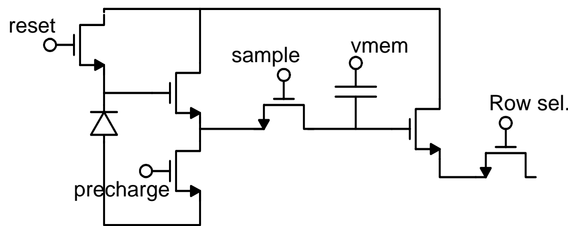


Figure 2: Schematic of the 6T pixel. The pixel consists of an n-well photo diode with its associated reset transistor. The first source follower with its load transistor connects to the storage capacitor through a sample switch. The second source follower connects to the column through the select switch.

The capacitor can sample and hold the photo diode signal for readout at a later time. This type of pixel supports three different operating modes. It allows correlated double sampling in rolling shutter mode, where the reset signal is stored at the beginning of the exposure time and read together with the signal at the end of the exposure time to cancel both FPN and reset kT/C noise. It also allows double sampling in snapshot shutter mode, where the signal is stored at the end of the exposure time and the reset signal is generated during readout to cancel the FPN. The reset kT/C noise is not cancelled as the signal and reset values originate from different reset operations. Finally the pixel supports pipelined snapshot shutter mode where the signal is stored at the end of the exposure time and it is read out single ended, so without reading the reset signal. This mode ensures maximum data throughput as it allows integrating the current frame while still reading the previous frame. A drawback of using a 6T pixel in this operating mode is that there is no on-chip FPN correction. As maximal data throughput is a key specification for the presented sensor, the pixels operate in pipelined snapshot shutter mode.

A key performance measure of a pixel used in pipelined snapshot shutter mode is its parasitic light sensitivity (PLS), which expresses the ratio of the sensitivity of the pixel during readout relative to the sensitivity during integration. It expresses the influence of the current image on the previous image which is still being read-out. This influence should be as low as possible and here the 6T pixel performs better than e.g. a 5T buried diode pixel that can also be used in pipelined snapshot shutter mode. The PLS of the used pixel is better than 1/4000.

The pixel is used in hard reset mode which maximizes the signal swing and avoids the non-linearity problems typically associated with soft reset. The disadvantage is a slight increase in temporal noise, which is not critical for this application.

Considering the sensor is built in a 0.25µm technology, the 6T pixels are at a small pitch of 8µm. Thanks to the use of micro lenses they maintain a good quantum efficiency (including fill-factor) of 37% at 600nm (Figure 3). Their high conversion gain of 40 µV/e^- minimizes the required integration time.

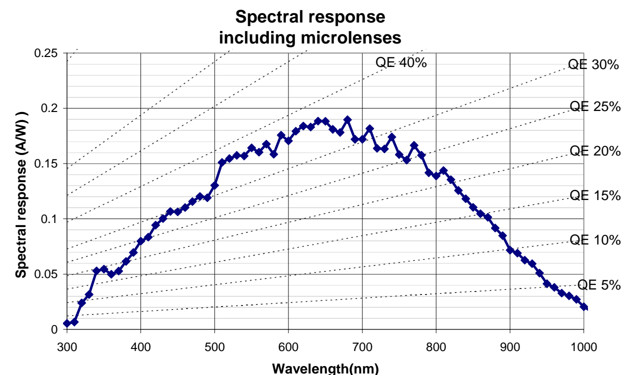


Figure 3: Spectral response as a function of wavelength for a sensor with microlenses.

4. ADC

The pixel output signals are digitized by 64 on-chip pipelined 8 bit ADCs operating at 26 Msamples/s each. The ADCs are designed using fully differential circuits to improve their performance and noise immunity. A redundant signed digit (RSD) architecture with 1.5 bit /stage and digital error correction ensures a good DNL and no missing codes, even in the presence of mismatch between the comparators. The inter-stage ADC gain errors are reduced by a commutation technique for capacitor matching and auto-zeroing removes the offsets. Data from the 64 ADCs is multiplexed on 32 high speed serial links.

5. High speed serial link

The sensor accepts a 208 Mhz LVDS input clock. This incoming high speed clock is divided to generate the different low speed clocks required for the operation of the sensor. It is also used to generate the serial output streams at 416Mbit/s. The outputs operate in double data rate (DDR) mode, which means a new data bit is put on the output at each clock transition (twice per clock cycle).

Synchronization between the sensor and the host requires a means to send control information across. This can either be done by embedding the control information in the data e.g. by employing the industry standard 8B/10B encoding or by adding a separate data channel, just to send the control information. Apart from 256 data words, 8B/10B encoding also has a set of additional control word available, which allow embedding control information into the same data stream as the payload while still allowing to distinguish it as control information at the receive end. 8B/10B has a number of other advantages such as DC balancing the data stream and guaranteeing minimum number of transitions per data word, both of which facilitate clock recovery on the receive-end. However, 8B/10B does introduce a 25% overhead in the amount of data that needs to be sent across the link. Taking into account that the control information is redundant between all channels, this is not an acceptable solution in a system with 32 data channels. That is why this sensor uses the alternative approach of simply adding two channels: one output clock channel and one synchronization data channel, which brings the total to 34 output channels. The output clock signal can be used to recover the data on the receive end without the need for clock recovery on the data channels themselves. However, the receiver should have per-channel skew correction to account for on-chip mismatches and intrinsic delays as well as for interconnect medium mismatches. The sensor has a training mode where it sends a known training pattern over each of the links to allow the host to do that calibration.

The synchronization channel sends start-of-frame, start-of-line, end-of-frame and end-of-line information the host. The current line number is also transmitted over the synchronization channel at the beginning of each line. To allow error detection at the receive-end, the sensor inserts a cyclic redundancy check (CRC) word into the data stream on each date channel at the end of every line.

The physical layer of the high speed link uses LVDS drivers. These drivers are designed in compliance with the ANSI/TIA/EIA-644-A-2001 standard for “Low Voltage Differential Signaling”. The circuit consists of a programmable current sink that defines the drive current, a dynamically controlled current source, a 4-transistor bridge that steers these currents to the differential outputs and a common-mode feedback circuit to balance the sink and source currents. The drive current can be changed by a register setting to allow operation outside the specified ANSI standard to reduce power and/or enhance speed.

6. Package and measurements

The sensor is processed in a 0.25µm 1P3M CMOS process. It is packaged in a custom made ceramic package with a 399 ball BGA. The package is made as small as possible to minimize the system size and at one side the pixel array is placed as close as possible to the edge of the package to relax the optical design. Figure 4 shows a picture of the packaged sensor.

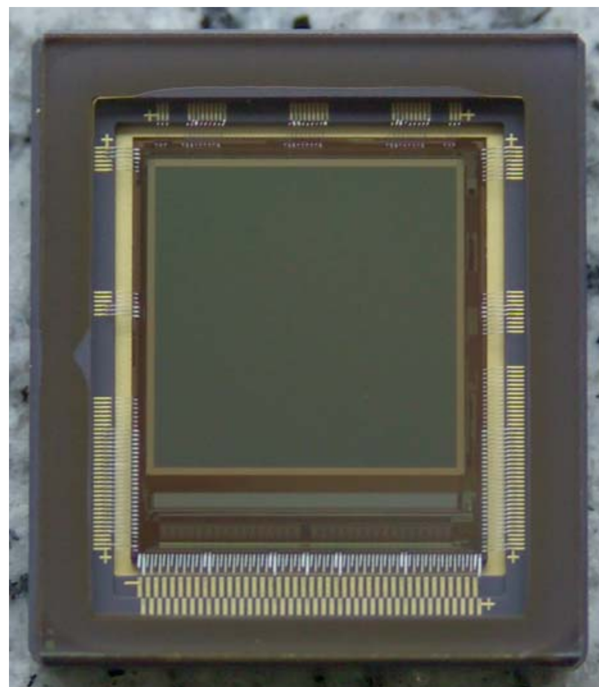


Figure 4: Photograph of the packaged sensor. The orientation of the sensor is identical to the floorplan shown in Figure 1.

Table 1 shows the key specifications and measurements of the sensor. The sensor has an on-chip reference photo diode for measuring photo current and a temperature diode for die temperature monitoring.

7. Conclusion

This paper presents a high speed image sensor design that fulfills the needs of a holographic data reader: high sensitivity and maximal data throughput at a moderate noise level and power consumption. This custom image sensor is suited for use in a high-end consumer holographic data reader.

Technology	0.25µm 1P3M CMOS process
Die size	16.0 mm (H) x 19.0 mm (V)
Packaged chip size	25.0 mm (H) x 29.0 mm (V)
Array size	1696 (H) x 1710 (V)
Frame rate	485 fps at full resolution
Shutter type	Pipelined snapshot shutter
Supply voltage	2.5V and 3.3V
Power consumption	1.1 W
Operating temperature	0ºC to 60ºC
Color	Monochrome only
Pixel type	6T N-well
Pixel size	8.0 µm x 8.0 µm
Peak QE	37% 600nm, with micro lenses
Sensitivity	2800 V m²/Watt s @600nm, with microlenses
Conversion gain	40 µV/e^-
Temporal dark noise	21 e^-
Pixel saturation charge	27000 e^-
Dark current	277mV/s at 40ºC
PRNU	2.5 % @ half saturation
FPN	17mV
PLS	<1/4000
ADC DNL / INL	0.31 LSB / 0.56 LSB
ADC resolution	8 bit
Data rate	208MHz input clock, 416Mbit/s data rate per channel 13.3Gbit/s aggregate data rate 1.4Gpix/s aggregate pixel rate
Interface	LVDS
Package	Ceramic package with 399 ball BGA

Table 1: key specifications and measurements.

References

[1]N. Bock, et al., “A Wide-VGA CMOS Images Senosr with Global Shutter and Extended Dynamic Range“ Proc. of IEEE Workshop on CCDs and AIS, Karuizawa, pp. 222-225, 2005

[2]Alex Krymski, Kenji Tajima, “CMOS Image Sensor with Integrated 4Gb/s Camera Link Transmitter”, in ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2005

A High Speed 4 Megapixel Digital CMOS Sensor

Alex Krymski

Alexima, 1028 N Lake Suite 204, Pasadena, CA 91104, USA
krymski@alexima.com

Abstract

We developed, fabricated and characterized a shuttered 4 Mpixel digital CMOS sensor running at the rate over 400 Frames/s. This paper discusses the pixel, the column ADC and the data readout architecture. The sensor delivers over 1.8 GPix/s of data at the maximum clock rate of 120 MHz. We also discuss the techniques implemented in the chip to reduce electronic noises.

The closest published sensor is a 4 Mpixel sensor developed by Photobit Technology [1], and which has become a popular product to machine vision and motion capture industries. The chip reported here achieves better functionality (shutter replacing rolling shutter, 2X frame rate, less column f.p.n., less electronic noise) with different circuits.

A simplified schematic of one column including the pixel, the column amplifier, and the ADC is drawn in Fig.1.

The conventional 5T shutter pixel based on a regular (non-pinned) photodiode can not have good dark uniformity because the switches resetting the photodiode and the pixel memory have statistically different feedthrough. The responsivity of the pixel is reduced to approximately a half of the photodiode responsivity because of the charge sharing between the photodiode and the pixel memory.

These disadvantages were addressed when designing a T-shape 5T shutter pixel which has a common reset switch for the photodiode and the memory, the solution that removes some of the fixed pattern noise. Responsivity was also improved almost twice because the pixel topology allows charge transfer rather than charge sharing. Implemented pixel was based on a traditional photodiode, so we observed some small-signal nonlinearity even when using flushing of the pixel. The non-linearity comes from the tail of the subthreshold current during the charge transfer through the transfer gate. An incomplete transfer should also give rise to the photodiode kTC noise. Implementing the photodiode as a pinned photodiode would improve the pixel linearity and should also remove this component of kTC noise.

The column ADC implemented in the chip is of the successive-approximation type [2], same as of the prototype sensor [1], however it is built of different components. Instead of an offset-reduction calibration DAC in each column, the new ADC extensively uses auto-zeroing. To achieve both good f.p.n. suppression and short decision time (e.g. 10 ns), the autozeroing comparator is made of a 3-stage offset-canceling pre-amplifier (similar to the one from reference [3]) and the reconfigurable dynamic latch which also uses an auto-zeroing for its offset reduction while in reset state. As a result, column f.p.n. was removed to the level non-detectable in the measurements. Instead, we started observing column f.p.n. from the source we did not expect before. The f.p.n. came from the ADC offset circuit generating the offset in each column with small area capacitor. The more bias is applied to the capacitor the more the offset is, and the more is the nonuniformity of the offset.

During the ADC operation, the data is stored in column ADC registers. To increase the readout data rate from the registers, we split the readout into 4-quadrants (Fig.2.). Register bit lines and the data lines were

thereby shortened by the factor of 2 and this was one of the techniques to increase the throughput from the chip twice compared to the prototype chip. To avoid clock skew issues driving the controls to the ADCs and the registers from both left and right, the clock is applied separately to the bottom and the top of the chip to I/O pads which are in the center of the top I/O pad frame and the bottom one, respectively.

We implemented several techniques in the sensor to carry out the experiments on electronic noise reduction.

A pseudo differential pixel readout was the first technique. Our column amplifier was built as a fully differential one while the pixel remained essentially single-ended. To verify pseudo-fully-differential pixel readout, an auxiliary circuit generated a copy of the ground noise with no signal. This copy was fed into the reference input of the column amplifier with the timing identical to the pixel readout. Two different noise reference generation solutions were tried with approximately same result.

The second technique was in reducing transient currents in digital circuits of the column ADCs. Instead of typically used SRAM cells we used DRAM cells to store the data and to control the status of the ADC conversion capacitors.

The third technique to reduce electronic noises was the supplying of the substrate of the ADC digital circuits with analog ground.

The combination of the three techniques gave a good overall result. The electronic noise which typically shows as a row-wise noise, did not come up, whereas it was a big issue in the sensors we developed using the previous sensor technology [1]. It remains unclear which technique contributed into the noise reduction the most.

There also was one negative outcome from the ground noise experiment- a worsening of the yield of the column ADCs, somewhat we never experienced before with the previous ADC topology. The yield loss was proven to be attributed to the leakage from some column DRAM cells, facilitated with the digital ground bounces. In average, one ADC in a thousand was failing. When running corner lots, the yield has been higher for slow-slow transistor models. With little redesign of DRAM cells this yield issue can be completely solved with no impact on the achieved substrate noise rejection.

The results of the sensor characterization are summarized in Table 1, and Fig.4 presents a minimally color-corrected JPEG-compressed image from the sensor.

References

1. A. Krymski, N. Bock, N. Tu, D. Van Blerkom and E. Fossum “A High- Speed, 240- Frames/s, 4.1-Mpixel CMOS Sensor”, IEEE Trans. Electron Devices, Vol.50, 2003, pp.130- 135.
2. R. E. Suarez, P. R. Gray, and D. A. Hodges “All- MOS Charge Redistribution Analog-to-Digital Conversion Techniques- Part II,” IEEE J. Solid-St. Circuits, Vol 10, pp. 379-385, 1975.
3. P. E. Allen, CMOS Analog Circuit Design. Oxford University Press, 2002, pp. 483- 485.

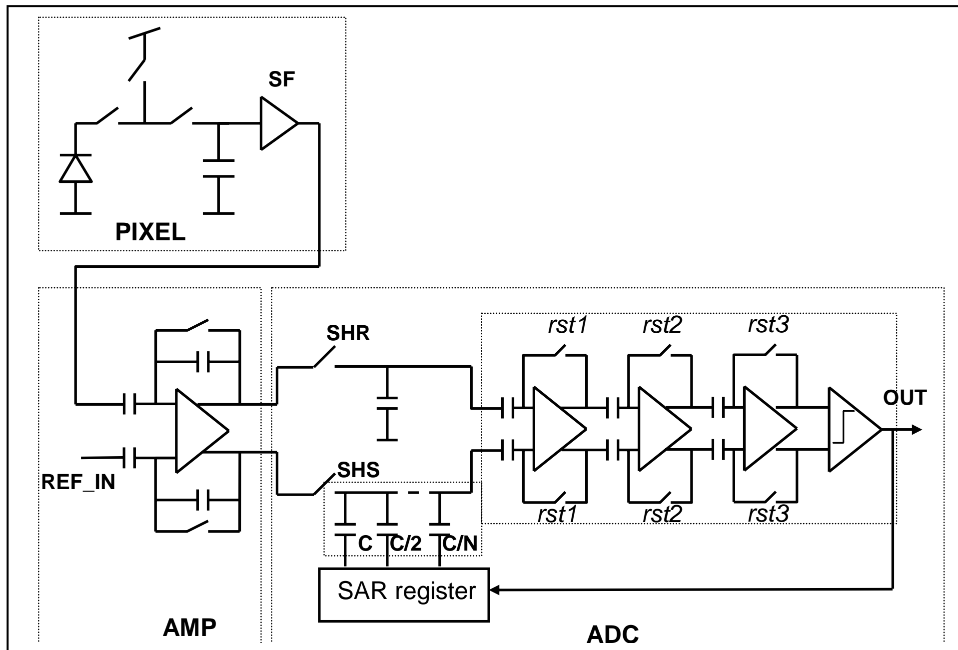


Fig.1. Pixel and column readout simplified schematic

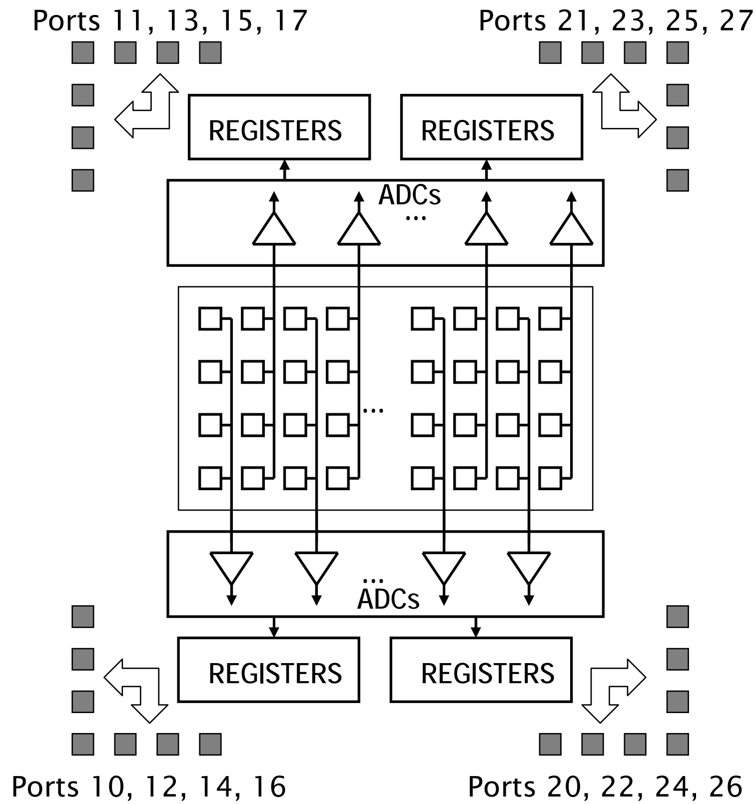


Fig.2. Readout architecture of the 4 Mpixel sensor

Fig.3. A sample picture taken with the 4 Mpixel sensor, with minimum color correction

Table 1

Process	0.25um 1P4M
Array size	4.1Mpix, 2368x1728
Pixel	7um 5T shutter, T-type
Output	16 ports x 10 bit
Max clock rate	120 MHz
Max frame rate	440 Fps @ full resolution
Power	<1.5W
Full well/ noise	25,000e-/30e-
Responsivity	4V/Lux*s @550nm
DSNU	150e- rms

Comparison of Global Shutter Pixels for CMOS Image Sensors

Stefan Lauxtermann, Adam Lee, John Stevens, Atul Joshi

Teledyne Imaging Sensors
5212 Verdugo Way
Camarillo, CA 93012 (USA)
Tel: (805) 484-6420
FAX: (805) 373-4687
E-mail: slauxtermann@teledyne.com

Abstract

In this paper we are presenting preliminary results from 4T technology based CMOS image sensors with global shutter, i.e. all pixels in the active array integrate light simultaneously. The global shutter operation mode is particularly important for high-speed video applications, where the more commonly implemented rolling line shutter creates motion blur. Our chips were fabricated using a 0.18 micron 4T, CIS technology with pinned photodiode and transfer gate. Different from conventional 3T type CMOS image sensors with global shutter pixel, in these 4T technology based global shutter pixels, the charge is transferred, not just sampled, onto the sense node. This translates into very high sensitivity and low readout noise at low power. For an imager with 7 transistors per pixel that is operated in global shutter, "Integrate While Read" mode, we measure an input referred noise of 10 electrons. The extinction ratio at full well signal charge is ~ 97.7%.

1. Introduction

Electronic exposure time control is a standard feature in digital still picture and video cameras, and for many applications this feature can be integrated directly into the sensor, eliminating the need for an external shutter mechanism. In CMOS image sensors (CIS) there are two fundamentally different shutter implementations, i.e. rolling line or global shutter. Due to the lower transistor count per pixel, the rolling line shutter has been the standard approach for electronic exposure time control in monolithic visible CMOS image sensors. Although a rolling line shutter imager (RLSI) can provide a very short integration time, artifacts are created when imaging fast moving scenes because each line of pixels is integrating light at a slightly different moment in time. For a RLSI the minimum possible scene time, defined as period between light integration in the first row of pixel to integration in the last row of pixel, is the frame readout time. This frame readout time can be much longer than the exposure time, required to image a fast moving scene without artifacts.

Over the past years pixels have become so small, that the true imager resolution is becoming defined by the fundamental optical diffraction limit [1]. Further shrinking of minimum feature size can therefore be applied to integrate more functionality, f.e. a global shutter, which requires a higher transistor count per pixel. Also, a reduction in the "as drawn" fill factor of a pixel is less critical to achieve maximum light sensitivity, due to the availability of micro lenses and the arising possibilities of backside illumination for CMOS image sensors. Only the full well capacity is reduced by the potentially smaller size of the photodiode. However, a GSI camera with global shutter imager is especially operated at short integration times, i.e. low effective signal levels, and maximum light sensitivity, defined by the sense node capacitance, is typically more important than full well capacity.

Therefore in order to maximize light sensitivity, low readout noise is particularly important in GSI cameras. However, a conventional 3T technology is not very well suited for 3 reasons: 1. Charge can only be shared between the photodiode and the sense node so that there is no voltage gain [2], 2. kTC noise can only be reduced by partial reset techniques like soft reset that are inherently prone to image lag which is not acceptable in high speed cameras, 3. kTC noise from photodiode and sense node reset, respectively contribute independently to the total noise, leading to a factor $\sqrt{2}$ higher noise compared to rolling line shutter imagers with the same full well capacity. These drawbacks cause lower light sensitivity but can be overcome by using a 4T process with pinned photodiode. Some operating constraints may still apply, depending on the number of transistors per pixel. For example, when using a CMOS image sensor process with pinned photodiode and transfer gate, a 4 or 6 transistor pixel can only be operated at moderate photon flux levels where the photodiode

full well capacity is large enough to integrate all photo charge carriers that are generated during the readout period. But many GSI sensors are operated under very strong lighting conditions, where the photon flux level exceeds the available full well capacity many times, causing image ghosting from shutter leakage. Fundamentally no such constrains exist for pixels with 7 transistors, although shutter leakage is critical in any monolithic GSI sensor [2].
4T type pixels with rolling line shutter have already been demonstrated to deliver very low noise [3]. We analyzed the performance of GSI sensors with 4, 5, 6 and 7 transistors per pixel, based on a 0.18 micron CIS technology with pinned photodiode and transfer gate. In addition to standard 4T CIS technologies, CCD type electrodes are available in this process for noise free charge domain signal processing. Our results are summarized in the following section. Initial results confirm the low noise capabilities of such pixels for applications in global shutter CMOS image sensors.

2. Results

The goal of our designs was the development of a low noise global shutter pixel for operation in "Integrate While Read" (IWR) mode, i.e. the 7T pixel. Consideration of 4, 5, and 6T pixels is for reference only. An overview of global shutter pixels is given in figure 3. The 4T ITR pixel was listed for completeness, but was not tested, because it is not compatible with 4T process technology. All pixels were integrated on a test imager with analog output and have a size of 8x8 micron^2. 12bit digitization is provided off-chip using a customized in-house readout board.

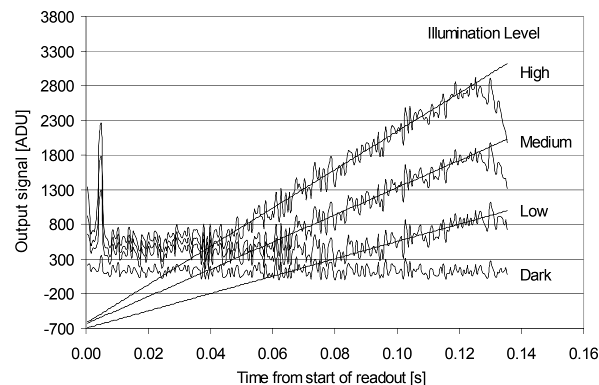


Figure 1: *Output signal as a function of delay time between end of shutter gate pulse on TG and readout time*

At low illumination levels, a 4T IWR pixel can be operated in global shutter mode, although it can only be read out using double sampling, i.e. not correlated double sampling. At higher illumination levels the shutter does not block light from parasitic charge integration on the sense node, because no proper charge drainage is provided on the photodiode. The same applies to the 6T pixel, which was qualitatively confirmed by not clocking the RsPD transistor in the 7T pixel. Figure 1 shows the output signal as a function of delay time between setting the shutter transistor TG to zero and the beginning of the readout for the 4T IWR pixel. As soon as the photodiode capacity limit is reached the transfer gate does not isolate the PPD from SN anymore. Because the signal charge per frame usually exceeds the available full well capacity, the 4T and 6T IWR pixels will perform poorly in any practical GSI camera application.
For a global shutter pixel with pinned photodiode and transfer gate the maximum achievable frame rate is determined by the time that it takes to remove the signal charge from the photodiode onto the sense node. We measured this time for a 4T IWR pixel by modulating the pulse width of the transfer gate pulse, TG. The measurement results are shown in figure 2. From this measurement it can be concluded that the charge transfer is complete after ~10 micro seconds in these pixels. The longer decay time of this response curve can be attributed to the RC time constant on the TX node after it is switched back to zero.

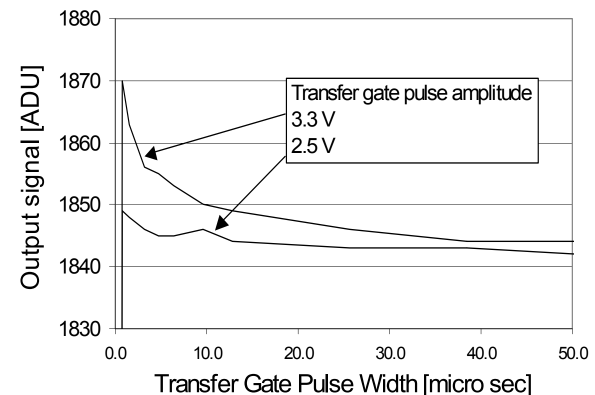


Figure 2: *Output signal as a function of transfer gate pulse width for TG pulse amplitudes of 2.5V and 3.3 V, respectively*

Although the presented 4T pixel does not perform well in global shutter imagers due parasitic charge integration on the storage node, the results of this characterization produce valuable insight into how photo generated charge carriers can reach the sense node SN.

#	Circuit	Type	Description
#1	Vsupply, RsSN, TG, SN, SF, PPD, RD	4T	Integrate while read (IWR) Double Sampling (DS) readout Only suited for low photon flux levels kTC noise limited FWC defined by PPD or SN capacity Measured: 2.75 e^- noise in rolling line shutter mode ~30 e^- in global shutter mode
#2	Vsupply, RsPD, SS, SN, SF, PD, RD	4T	Integrate Then Read (ITR) Double sampling (DS) readout combined with global reset and signal sampling Suited for high photon flux levels kTC noise limited FWC defined by PD capacity Signal sampling onto SN (not possible with PPD+TG technology) Estimated: ~30e- if PD has similar FWC as PPD in pixel #1
#3	Vsupply, RsPD, RsSN, TG, SN, SF, PPD, RD	5T	Integrate while read Double sampling readout Suited for high photon flux levels kTC noise limited FWC defined by PPD or SN capacity Charge transfer onto SN (based on PPD+TG technology) Estimated: ~30e- if SN has same dimensions as pixel #1
#4	Vsupply, RsSN, TG, SH, SS, SN, SF, PPD, RD	6T	Integrate then read Correlated Double Sampling (CDS readout) Only suited for low photon flux levels kTC noise free FWC defined by PPD, SH or SN capacity Charge transfer onto SN Same performance as pixel #5 when RsPD kept at zero
#5	Vsupply, RsPD, RsSN, TG, SH, SS, SN, SF, PPD, RD	7T	Integrate While Read (IWR) Correlated Double sampling (CDS readout) Suited for high photon flux levels FWC defined by SH and SN capacity Charge transfer onto SN Measured: 10 e^-

PPD	- Pinned Photo Diode	SN	- Sense Node
PD	- Photodiode	RsPD	- Reset Photodiode
TG	- Transfer Gate	RsSN	- Reset Sense Node
SH	- Sample Hold Gate	SF	- Source Follower
SS	- Sample Signal Gate	RD	- Read
FWC	- Full Well Capacity		

Figure 3: *Overview of global shutter pixels. The 5T and 7T pixels can be operated in "Integrate while Read" mode. Correlated Double Sampling (CDS) readout is only possible for a 6T and 7T pixel*

Using the same 0.18 µm CMOS process, a global shutter imager with 7T IWR pixel was fabricated. For characterization the chip was mounted in a camera like setup and basic imaging performance was demonstrated. For all further measurements the lens was removed and the sensor was illuminated with a white light source. No IR radiation filter was applied. In order to measure the temporal noise, we recorded the standard deviation as a function of signal intensity in the shot noise limited domain for a single pixel. The slope of this curve represents the sensitivity in ADU/e^-. Using the conversion factor of 0.5 ADU/e^-, the input referred noise in number of electrons was measured to be 10e^-. The noise measurement for the 7T pixel is presented in figure 4. In this measurement the signal level was modulated via integration time and light intensity, respectively. Both methods result in the same noise level for the same input intensity.

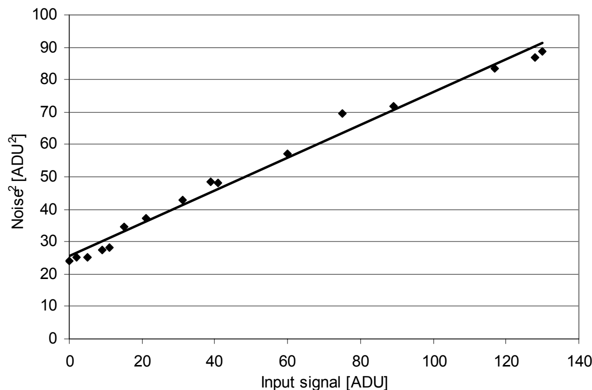


Figure 4: *Noise^2 versus input signal. From RMS line fit: sensitivity = 0.5 ADU/e^-, readout noise = 10 e^-*

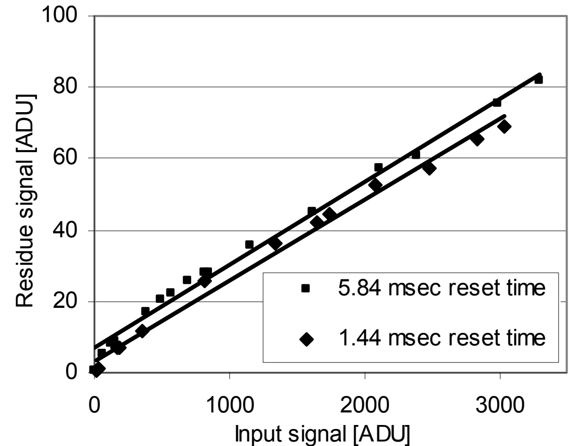


Figure 5: *Residue Signal as a function of input signal after TX gate in pixel #7 is switched to zero*

3. Summary

Based on a 7 transistor pixel with pinned photo diode and transfer gate, we demonstrated a global shutter imager with a temporal readout noise of 10e^- for an 8x8 micron^2 pixel in 0.18 µm CMOS technology. This noise level is slightly higher compared to that in a conventional rolling line shutter CMOS image sensor with comparable sense node capacitance. The shutter leakage of 2.3% for this pixel is comparatively high and is attributed to diffusion of photo generated charge carriers onto the sense node. Some improvements will be possible from modified timing and by inserting and NIR filter into the optical path. However, the main improvement is expected from modifications in the underlying CIS process.

References

[1] G. Yang, T. Dosluoglu, "Ultra High Light Shutter Rejection Ratio Snapshot Pixel Image Sensor ASIC for Pattern Recognition", CMOS Image Sensors, 2005 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Nagano, Japan June 9-11, 2005

[2] S.Lauxtermann, G.Israel, P.Seitz, H. Bloss, J. Ernst, H. Firla, S. Gick, "A Mega-Pixel High Speed CMOS Imager with Sustainable Gigapixel/sec Readout Rate", 2001 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Lake Tahoe, Nevada USA

[3] G. Agranov, T. Gilton, R. Mauritzon, U. Boettiger, P. Altice, J. Shah, J. Ladd, X. Fan, F. Brady, J. McKee, C. Hong, X. Li, I. Patrick, "Optical-electrical characteristics of small, sub-4µm and sub-3µm pixels for modern" CMOS Image Sensors, 2005 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Nagano, Japan June 9-11, 2005

Dynamic range extension of CMOS imager with linear response by hybrid use of active and passive pixel readouts

Keiichiro Kagawa[a], Yudai Adachi[a], Yugo Nose[b], Kuniyuki Tani[b], Atsushi Wada[b], Masahiro Nunoshita[a], and Jun Ohta[a]

[a]*Graduate School of Materials Science, Nara Institute of Science and Technology, 8916-5 Takayama, Ikoma, Nara 630-0101 JAPAN*

Phone: +81-743-72-6054, Fax: +81-743-72-6052, E-mail: kagawa@ms.naist.jp,

[b]*Sanyo Electric Co., Ltd.*

ABSTRACT

We present a new dynamic range extension method of CMOS imager by hybrid use of active and passive pixel readout methods with electrical calibration for image reproduction. Based on a CMOS imager with a lateral overflow integration capacitor, we have introduced the passive pixel readout to reading the charges in the overflow capacitor for high illumination to achieve high linearity, wide dynamic range more than 120dB, and no moving image deterioration as well as high-sensitivity given by the active readout. We have fabricated a 128x96-pixel prototype image sensor in a 0.35-μm CMOS technology. In this paper, we demonstrate image acquisition by the prototype sensor, and show offline image reproduction to enhance the dynamic range by 18.5dB with electrical calibration. After image reproduction, column fixed pattern noise in the passive readout was reduced from 10.6%rms to 0.97%rms.

I. INTRODUCTION

CMOS imagers are promising in wide dynamic range image acquisition due to their capability of integrating various kinds of electronic circuits. In this paper, a new dynamic range extension method of CMOS imager by hybrid use of active and passive pixel readouts with electrical calibration for image reproduction is presented. A CMOS imager with a lateral overflow integration capacitor[1] provides high-sensitivity, linearity, and wide dynamic range around 100dB, and is free from moving image deterioration, which is a significant problem in multi-sampling methods[2]. We propose to utilize the passive readout method[3] to read the overflowed photocharges, and demonstrate acquisition of the reproduced images with a prototype sensor. By use of the advantage of the passive readout method such as large charge capacity, available voltage range of the overflow capacitor can be increased to further extend the dynamic range. The amount of the saturation charges can be several times as much as that by the active readout method. Moreover, nonlinear region of the MOS capacitor as an overflow capacitor can be utilized without degrading the linearity to maximize the dynamic range. In this paper, we show a 128x96-pixel prototype image sensor fabricated in a 0.35-μm CMOS technology, and demonstrate image acquisition by the prototype sensor. We show offline image reproduction to enhance the dynamic range with electrical calibration, and demonstrate that our image reproduction method has effect of reducing column fixed pattern noise (FPN) in the passive readout.

II. CMOS IMAGER BASED ON HYBRID PIXEL READOUT ARCHITECTURE

Figures 1 and 2 show the pixel structure and an example of the potential diagram. The pixel has a MOS capacitor as an overflow capacitor(C_{OF}), overflow-control transistor(M_{OF}), an anti-blooming transistor(M_{AB}), source follower transistor(M_{SF}) for active readout, and select transistors for active and passive readouts(M_{RSA} and M_{RSP}). The procedure for readout of each pixel is composed of 1) non-destructive active readout of the photodiode potential, 2) decision of the actual readout mode based on the non-destructive readout result, and 3)

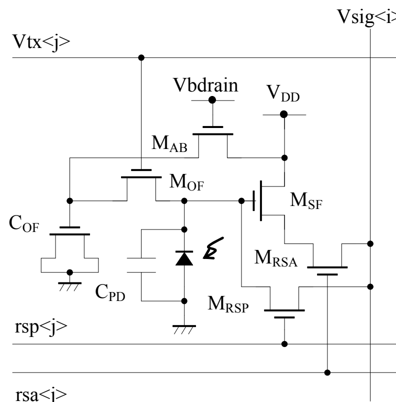


Fig. 1. Pixel schematic.

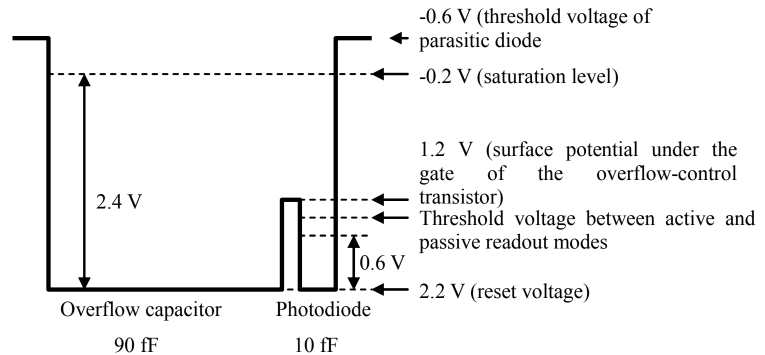


Fig. 2. Simplified potential diagram for explaining dynamic range extension by the proposed method.

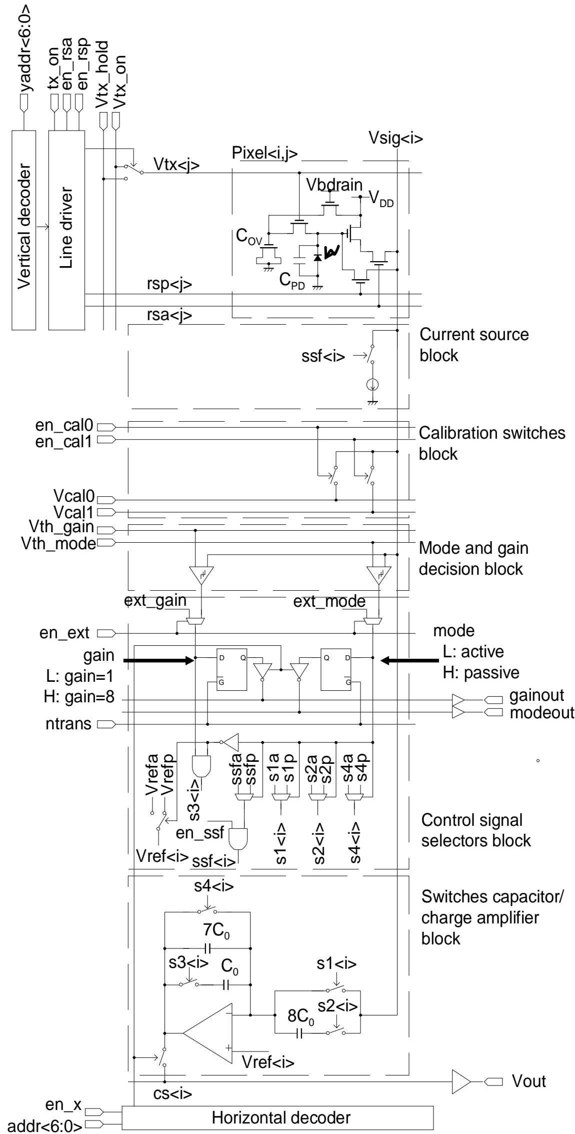


Fig. 3. Pixel structure and a simplified schematic of the CMOS imager.

Table 1. Specifications and characteristics of the prototype sensor.

Item	Value
Technology	0.35-µm standard CMOS (2P, 4M)
Chip size	4.5 mm x 8.2 mm
Pixel size	15 µm sq.
Components in pixel	1 PD, 5 transistors, and 1 MOS capacitor
Pixel count	128×96
Frame rate	30 fps
Sensitivity	3.3 V/lx·s (APS) 0.036 V/lx·s (PPS)
Dynamic range	54.3dB (APS)/ 45.7dB(PPS)
Dynamic range extension by PPS	18.5dB
Total dynamic range	72.8dB
Column FPN	0.28%rms (APS)/ 10.6%rms (PPS before mapping)/ 0.97%rms (PPS after mapping)
Pixel FPN	0.64%rms (APS)/ 0.10%rms (PPS before mapping)/ 0.55%rms(PPS after mapping)

actual pixel readout and reset. The actual readout for the active or passive readout is performed by use of a switched capacitor amplifier or a charge amplifier, respectively. As shown in Fig. 2, the advantage of the passive readout is large charge capacity given by large overflow capacitance and large voltage range whose lower limit is smaller than the threshold voltage of the select transistor M_{RSP}. We can utilize the voltage range under the threshold of the switch transistor and even under 0 V, which increases the amount of the saturation charges, and enlarges the dynamic range. Another advantage is good linearity due to usage of the charge amplifier, while the capacitance of the MOS capacitor is highly nonlinear under the threshold voltage.

Figure 3 and Table 1 show the simplified schematic of the CMOS imager and its specifications, respectively. To select pixel readout methods, passive or active, according to the illumination pixel by pixel, the pixel has two readout paths to the vertical signal line of each column. One of paths is composed of a source follower transistor and a switch transistor for active readout, and the other is only a switch transistor for passive readout. Readout mode is determined by the source follower output of the non-destructive active readout followed by the actual readout. The column amplifier works as a switched capacitor in the active readout mode or a charge amplifier in the passive mode.

Figure 4 and Table 2 show a timing chart for one horizontal period and operations for each elemental period, respectively. At first, source follower output by a non-destructive active readout is compared with the predetermined threshold voltage, and the readout mode is determined. Then, pixel readout is executed in the appropriate readout mode at each column. Note that row control signals such as rsa<j>, rsp<j>, and tx_on<j> are shared in a row. To avoid the confliction of pixel operation between two readout modes, no operation (NOP) is

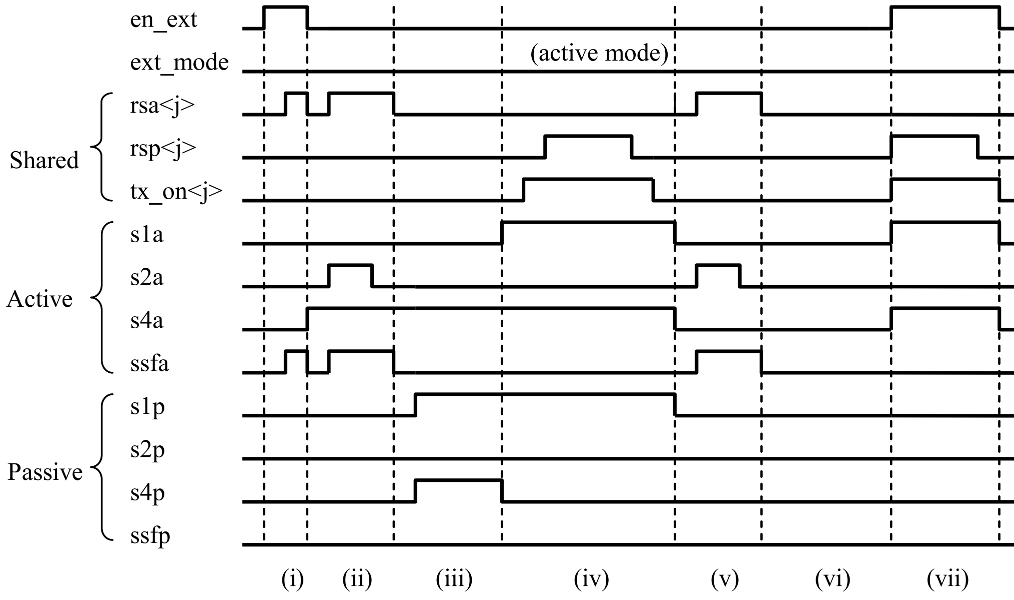


Fig. 4. Timing chart.

Table 2. Operations in one horizontal period.

Period	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)
Active	mode and gain decision	auto-zeroing	NOP	pixel reset	amplification	readout off-chip	pixel reset
Passive		NOP	auto-zeroing	amplification	NOP		

properly inserted in the pixel readout procedure.

In the case of the configuration shown in Fig. 3, dynamic range can be extended by 32dB at most with the passive readout. Disadvantage of the passive readout is large noises concerning the capacitance of the vertical signal line is suppressed in our sensor because the feedback capacitance C_0 of the charge amplifier is comparable with the parasitic capacitance of the vertical signal line to extend the dynamic range. C_0 is 100fF in this case.

III. EXPERIMENTAL RESULTS

Table 1 summarizes the characteristics of the prototype imager. Figure 5 shows relationship between illumination and the voltage of the sensor output. The dynamic range is enhanced by 18.5dB with the passive readout.

The sensor has calibration switches that can supply test voltages directly to the photodiode in a pixel. By use of the sensor outputs for two different test voltages in two readout modes, the outputs by the passive mode can be mapped on the active outputs. The mapping function is given by the following equation.

$$V_{out,A} = \frac{v_{A1} - v_{A2}}{v_{P1} - v_{P2}} \cdot V_{out,P} + \frac{v_{P1}v_{A2} - v_{P2}v_{A1}}{v_{P1} - v_{P2}}. \quad (1)$$

The readout result in the passive mode, $V_{out,P}$, is mapped on $V_{out,A}$. V_{A1}, V_{A2}, V_{P1}, and V_{P2} are the outputs of the imager for the test voltages of Vcal0 and Vcal1. Note that Vcal0 and Vcal1 do not appear in Eq. 1.

As shown in Fig. 5(b), we can see that the passive outputs can be successfully mapped on the line of the active outputs. Vcal0 and Vcal1 were 1.6 V and 2.1 V, respectively. Figure 6(a) and (b) show the captured images in active and passive readout modes, respectively. Figure 6(c) and (d) show the operation mode for each pixel and the reproduced image with off-line processing. They were calculated from the images in Fig. 6(a) and (b) and four images for two test voltages read out in the active and the passive modes. As shown in Fig. 6(d), the dynamic range has been successfully enlarged. Image reproduction mapping given by Eq. 1 enables us to decrease the FPN in the passive readout because the information of the FPN is included in the mapping functions. As shown in Table 1, column FPN was reduced from 10.6%rms to 0.97%rms after the image reproduction. Note that the mapping function given by Eq. 1 was obtained for each pixel in the offline processing because that was a preliminary demonstration. However, in the goal, the mapping function is acquired for each column because pixel-wise FPN is eliminated by the column amplifier.

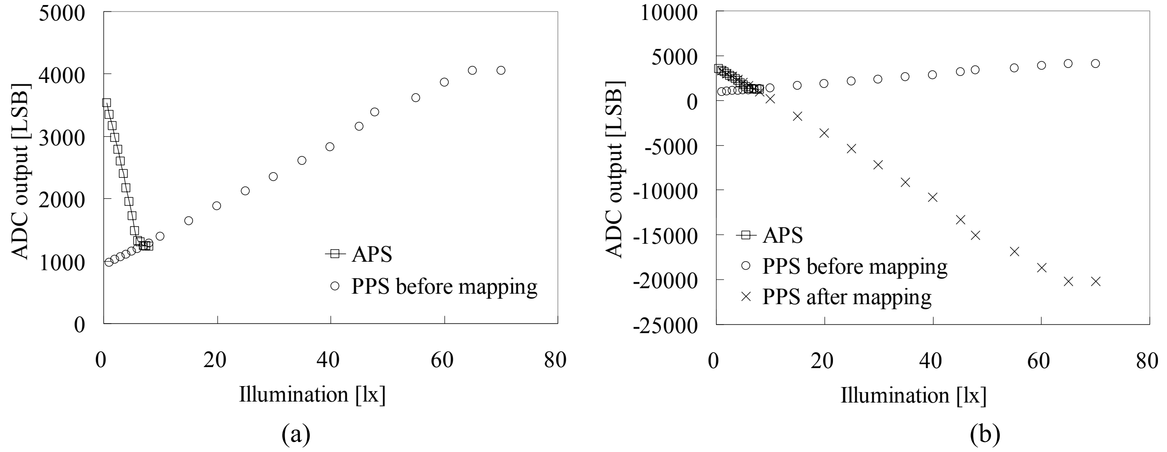


Fig. 5. Relationship between illumination and sensor outputs (a) before and (b) after reproduction mapping.

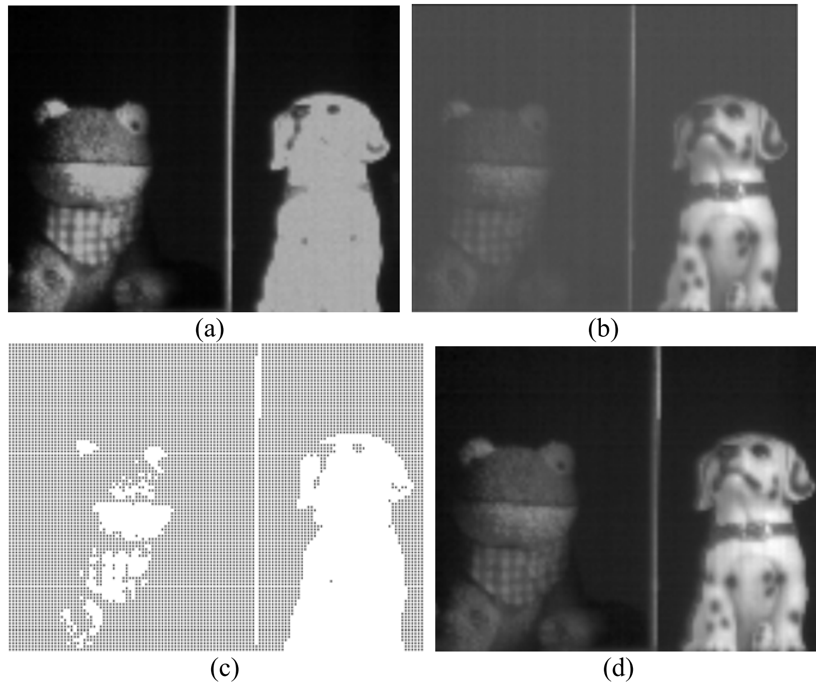


Fig. 6. Captured images by (a) APS and (b) PPS modes (γ=1.0), (c) operation modes of each pixel (black: active, white: passive), and (d) off-line reproduced image with enhanced dynamic range (γ was controlled with 2.0). Only column CDS is performed on the sensor.

IV. CONCLUSIONS

We have proposed dynamic range extension by hybrid use of active and passive readout methods. We have fabricated a 128x96-pixel CMOS imager with the proposed scheme in a 0.35-μm CMOS technology. From the experiments, image reproduction and dynamic range extension of 18.5dB have been successfully demonstrated.

The dynamic range will be increased by up to 32dB by optimizing the feedback capacitance of the charge amplifier (400 fF). Total dynamic range can be enlarged to about 120dB, which is required in the automotive applications, with an adaptive gain method [4]. By use of 0.18-μm CMOS technology, the pixel size will be shrunk to about 5 μm sq without decreasing overflow capacitance.

REFERENCES

1. S. Sugawa *et al.*, Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf.(2005) 352.
2. M. Mase *et al.*, Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf., 19.3 (2005) 350.
3. I. L. Fujimori et al., IEEE J. Solid-State Circuits, **35**, 12 (2000) 2031.
4. S. Kawahito *et al.*, Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf., 12.7(2003) 224.

A Wide Dynamic Range CMOS Image Sensor With Dual Capture Using Floating Diffusion Capacitor

Dongsoo Kim, Dongmyoung Lee, Youngcheol Chae, and Gunhee Han
Department of Electrical and Electronic Engineering
Yonsei University, 134, Sinchon-dong, Seodaemun-gu, Seoul, Korea
Phone:+82-2-2123-7710, Fax:+82-2-312-4584
Email: soo@yonsei.ac.kr

***Abstract*—A wide dynamic range CMOS image sensor with dual capture using floating diffusion capacitor is proposed. The proposed structure performs dual capture without on-chip frame memories and the dynamic range of the proposed image sensor is controllable with dual electronic rolling shutter. The chip includes 320 (H) × 240 (V) effective pixels. Each pixel has 33% fill factor in an area of 5.6 × 5.6 μm^2. The measurement results show that the dynamic range can be maximally expanded by 48 dB and the leakage voltage of the floating diffusion is 27% of the conventional contact metallization. The core area is 3000×2700 μm^2 and total power consumption of the system is 12 mW with 3.3-V analog and 1.8-V digital supply voltages.**

I. INTRODUCTION

A wide dynamic range CMOS image sensor that is capable of capturing natural scenes without black level saturation and white crushing is a requisite for many applications such as automobile cameras, security cameras and consumer products. Numerous methods to expand the dynamic range of CMOS image sensor were reported in the literatures. The one of the well known techniques is using nonlinear response of the pixel devices or circuits. The use of logarithmic response [1], the combination of logarithmic and linear response [2], and photodiode capacitance adjusting [3] are well known. However, these approaches are disadvantageous in low signal-to-noise ratio (SNR) and large fixed pattern noise (FPN) [1-3]. The most common technique for wide dynamic range is the dual (multiple) capture technique with different exposure [4-7]. The conventional dual capturing techniques require large size on-chip digital frame memories [4-6] or in-pixel overflow integration capacitor which considerably decreases the pixel fill factor [7].

In dual capture method, the dynamic range is decided by the ratio of short integration time (T_S) to long integration time (T_L) as blow

$$DR = 20\log\frac{Q_{\max}}{Q_{\min}}\frac{T_L}{T_S} \tag{1}$$

where $Q_{\max}$ is the maximum signal charge that can be handled in the pixel and $Q_{\min}$ is the minimum signal charge determined by the noise level and exposure time.

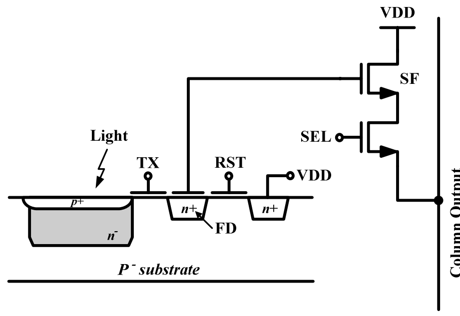
This paper proposes a wide dynamic range CMOS image sensor with dual capture which does not need on-chip frame memories. The proposed dual capture structure stores the integrated signal of different exposure time in the floating diffusion (FD) capacitor instead of digital frame memory. The removal of the contact metallization between FD and source follower gate reduces the leakage current of FD capacitor and increases pixel fill factor. The dynamic range of the proposed image sensor can be controllable with dual electronic rolling shutter. In Section II, we present the pixel structure for dual capture. Section III describes the proposed system of wide dynamic range image sensor and dual electronic rolling shutter. In Section IV, the experimental results is presented. Lastly, we conclude in Section V.

II. PIXEL STRUCTURE FOR DUAL CAPTURE

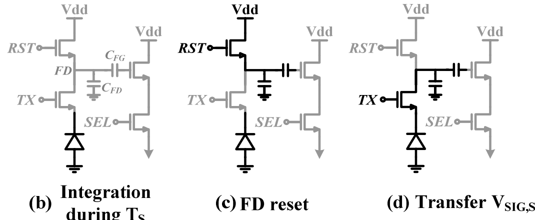
Fig. 1 shows the schematic, the operation flow and the timing diagrams of the proposed pixel for dual capture. The pixel is composed of a pinned photodiode, a parasitic FD capacitor C_{FD}, a floating gate capacitor C_{FG}, and readout circuits such as a reset transistor, a transfer transistor, a source follower, and a selection transistor.

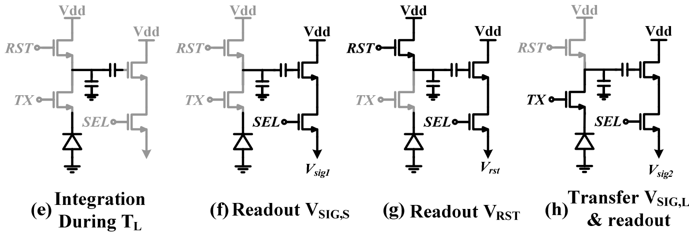
The connection between FD node and source follower gate is made with a contact metallization in the conventional 4-transistors/pixel structure. The contact metallization causes leakage current by the carrier trap in interface between silicon and contact and occupies large pixel area due to process design constraints of contact and metal. In the proposed pixel structure, as FD node and source follower gate is connected with not the contact metallization but poly-to-diffusion capacitor C_{FG}, the leakage current of FD capacitor is decreased and the pixel fill factor is increased. C_{FG} is overlap and fringe capacitances between source follower gate and FD as shown in Fig. 1 (a).

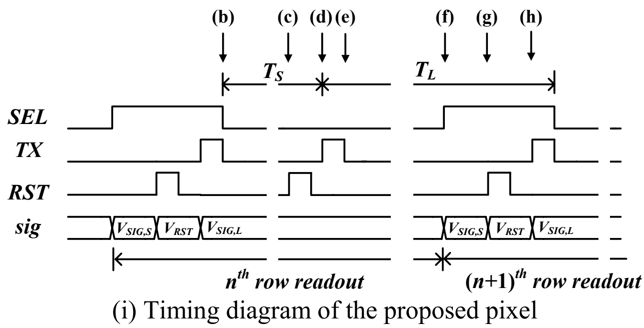
The operation procedure is as follows. The photodiode generates electronic charge of an amount corresponding to the incident light intensity during short exposure time (b). The FD is reset by pulsing *RST* (c) and the integrated signal $V_{SIG,S}$ of short exposure time (T_S) is transferred and stored in C_{FD} (d). Then the photodiode is started to generate again the integrated signal $V_{SIG,L}$ of long exposure time (T_L) before the readout turn



(a) Proposed pixel schematic







(i) Timing diagram of the proposed pixel

Figure 1. Schematic, operation flow and timing diagram of the proposed wide dynamic range image pixel

of the pixel comes (e). When the pixel transfers the pixel signals to column readout circuit, $V_{SIG,S}$ of C_{FD} is transferred to column readout circuit by turning on the selection transistor (f). Next, the FD reset signal, V_{RST} and the integrated signal, $V_{SIG,L}$ of T_L are transferred sequentially to column readout circuit by pulsing *RST* (g) and *TX* (h). The V_{RST} is used to eliminate the offset, switch charge injection, and noises including kT/C noise and low frequency noise using digital correlated double sampling (DCDS) by performing (V_{RST} -$V_{SIG,S}$) and (V_{RST} -$V_{SIG,L}$) [9].

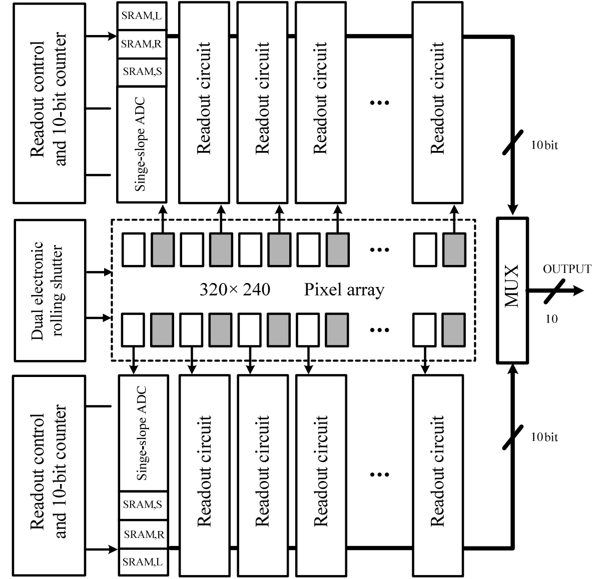


Figure 2. Block diagram of the proposed wide dynamic CMOS image sensor

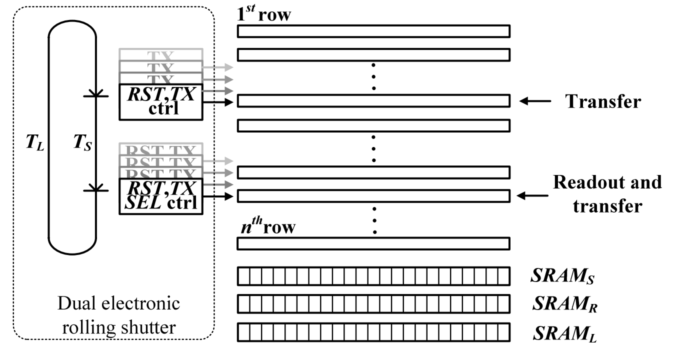


Figure 3. Block diagram of dual electronic rolling shutter

III. THE PROPOSED WIDE DYNAMIC IMAGE SENSOR AND DUAL ELECTRONIC ROLLING SHUTTER

The proposed wide dynamic CMOS image sensor is composed of 320×240 pixel array, dual electronic rolling shutter, column readout circuits including single-slope ADC and SRAM array, readout control and 10bit counters as shown in Fig. 2. Readout circuits are located in even and odd column and the stored 10-bit data is outputted though MUX.

Dual electronic rolling shutter is required to capture dual images having different exposure times in a frame readout timing as presented in Fig. 3. Dual electronic rolling shutter is composed of two rolling control units. One is for resetting FD and transferring $V_{SIG,S}$ from photodiode to C_{FD} by pulsing *RST* and *TX* as shown in Fig.1 (c) and (d). The other is for outputting pixel signals ($V_{SIG,S}$, V_{RST} and $V_{SIG,L}$) to column readout circuit by

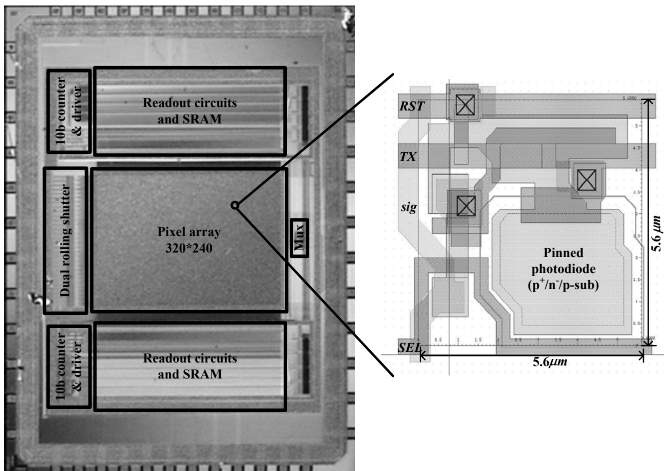


Figure 4. Microphotograph of the fabricated image sensor and layout of the wide dynamic pixel

turning on *RST, TX*, and *SEL* as shown in Fig. 1 (f), (g) and (h). The two row control units revolve independently with a time interval. The time interval decides the short and the long exposure times, T_S and T_L. Therefore, the minimum T_S is a column readout time and maximum T_L is the (n-1) times of T_S when n is the number of row. The dynamic range can be extended maximally by 20log(n-1). The transferred pixel signal, $V_{SIG,S}$, V_{RST} and $V_{SIG,L}$ are converted to digital data and stored in $SRAM_S$, $SRAM_R$, and $SRAM_L$, respectively.

IV. Experimental Results

The proposed CIS system was designed and fabricated by 0.35-μm 2-poly 3-metal CMOS process. The microphotograph of the prototype image sensor and layout of the wide dynamic pixel are shown in Fig. 4. The proposed image sensor is integrated with QVGA (320×240) pixels and the pixel size is 5.6 μm × 5.6 μm. The photodiode is p^+/n^-/p-substrate pinned structure and fill factor is 33%. The core area is 3000×2700 μm^2 and total power consumption of the system is 12 mW with 3.3-V analog and 1.5-V digital supply voltages. The measured column FPN is 0.0073% of full code.

Fig. 5 shows the captured sample images from the fabricated image sensors. The black level saturation at short exposure time and white crushing at long exposure time are occurred in normal image sensor mode as shown in Fig. 5 (a) and (b). However, the synthesized wide dynamic range image from dual captured images of the proposed image sensor does not have the white crushing around the light bulb or the black level saturation around the resolution chart in Fig. 5(c)

The integrated signal of short integration is stored in the FD capacitor during long integration time and gives information about the highly illuminated region. The low leakage current is

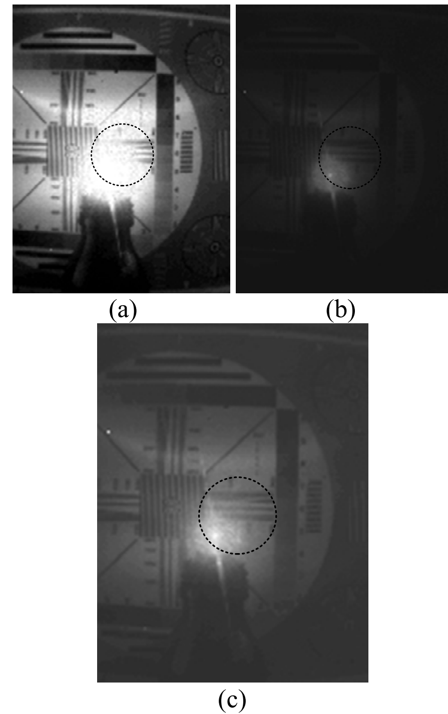


Figure 5. The captured sample images from the fabricated chip at (a) short exposure time (b) long exposure time (c) synthesized wide dynamic range image

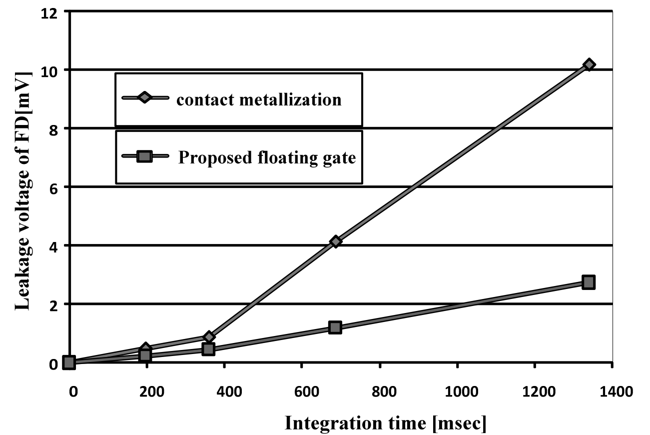


Figure 6. Measured leakage voltage comparison of FD in contact metallization and proposed contactless floating gate

a prerequisite for dual capture using FD capacitor. Fig.6 presents the leakage voltage comparison of FD node in the conventional contact metallization method and the proposed floating gate method. The measurement results indicate that the leakage voltage of the proposed contactless floating gate method is 27% of the conventional contact metallization method.

TABLE I

PERFORMANCE SUMMARY

Process	0.35-µm CMOS 2-poly 3-metal
Core area	3 mm x 2.7 mm
Array format	320 x 240
Pixel size / Fill factor	5.6 µm x 5.6 µm / 33 %
ADC	Column-wise single-slope ADC
Dynamic range enhancement	Controllable with T_S/T_L (47 dB is increased maximally)
Video output	10 bit digital
Shutter	Dual electronic rolling shutter
Column FPN	0.0073 % of full code
Power supply	3.3 V (analog) / 1.8V (digital)
Power consumption	12 mW

Design specifications and performances of the proposed wide dynamic range CMOS image sensor are summarized in Table I.

V. CONCLUSION

This paper proposed a wide dynamic range CMOS image sensor with dual capture using floating diffusion capacitor. The proposed wide image sensor can capture dual image with different exposure times in one frame. The dynamic range is expanded maximally by 48 dB. The dual electronic rolling shutter can easily control the dynamic range with the time interval between the rolling control units. The experimental results show that the contactless source follower gate decreases the leakage current of 27% compared to the conventional contact metallization. The influence of the fixed charge in the floating gate capacitor can be eliminated by correlated double sampling.

ACKNOWLEDGMENT

This work was supported in part by the Ministry of Information Technology Research Center Support Program, and in part by Samsung Electronics Co. Ltd.

REFERENCES

[1] S. Decker, R. Mc Grath, K. Brehmer, and C. Sodini, "A 256 _ 256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 1998, pp. 176–177.

[2] K. Hara, H. Kubo, M. Kimura, F. Murao, and S. Komori, "A linear-logarithmic CMOS sensor with offset calibration using an injected charge signal," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2005, pp. 354-355.

[3] Y. Chae, K. Choe, B. Kim, and G. Han, "Sensitivity Controllable CMOS Image Sensor Pixel Using Control Gate Overlaid on Photodiode", *IEEE Electron Device Lett.*, Jun. 2007.

[4] M. Mase, S. Kawahito, M. Sasaki, S. Wakamori, "A wide dynamic range CMOS image sensor with multiple exposure-time signal outputs and 12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2787-2795, Dec. 2005.

[5] M. Sasaki, M. Mase, S. Kawahito, Y. Tadokoro, "A Wide Dynamic Range CMOS Image Sensor with Multiple Short-Time Exposures," *in Proc. IEEE Sensors*, Vlenna, Oct. 2004. pp. 967-972.

[6] O. Yadid-Pecht, E. R. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling," *IEEE Trans. Electron Devices* , vol. 44, no. 10, pp. 1721−1723, Oct. 1997.

[7] S. Sugawa, N. Akahane, S. Adachi, K. Mori, T. Ishiuchi, K. Mizobuchi, "A 100 dB dynamic range CMOS image sensor using a lateral overflow integration capacitor, *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2005, pp. 352- 353.

[8] D. Kim, J. Kim, B. Hwang, D. Cho, K. Kim, S. Kim, J. Hong, J. Park, M. Lee, "Borderless contact leakage induced standby current failure onsub-0.15 µm CMOS device," *in Proc. The 8th Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore, Jul. 2001, pp. 165-168.

[9] S. Yoshihara, M. Kikuchi, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, K. Koseki, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, "A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS image sensor with seamless mode change," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2006, pp. 492–493

Analog Readout Circuitry for Wide-Dynamic-Range CMOS image sensors

Jose Tejada, Hirokazu Sawada, Shigetoshi Sugawa † and Nana Akahane †
jose.tejada@ti.com, sawada@ti.com; Texas Instruments Japan
† sugawa@fff.niche.tohoku.ac.jp † nana@fff.niche.tohoku.ac.jp; Tohoku University, Japan

Abstract

This paper describes the readout circuitry of a SVGA wide-dynamic-range (>90dB) CMOS image sensor, which is the first of its class to operate at 60 frame/s. Lateral-overflow capacitor CMOS image sensors [1,2] require two images per frame as well as low noise and highly linear circuits. To achieve these specs, high-output impedance pixel current sources with smooth start-up and a 36MHz segmented line memory were implemented. Supporting blocks like the voltage regulators and output amplifier are described too. The chip was made in a 2P3M CIS 0.18µm process.

Signal Flow

Although the fundamental operation of this type of wide dynamic range sensor had been previously published [1,2]; the readout circuitry was still left to be explained. The basic signal flow has not changed: pixel offset (N) and offset+signal (NS) are sampled in a line memory to then flow through a common bus up to a differential amplifier, which subtracts N from NS to make a single ended output.

The S1 (low-light) and S2 (high-light) signals are processed in parallel so the readout circuitry is twice that of a regular CMOS sensor. Both the top and bottom of the pixel array are used to place these circuits (figure 1).

Pixel Biasing

The column current source that biases the pixels uses a cascode in order to increase the pixel linearity. A buffer is needed to drive the 820 gates (figure 2) of the cascode transistors. An original amplifier using common-mode feed-forward was used to speed up the turn-on process (figure 3).

The pixel line and sampling capacitor reset voltage is chosen so as to allow a smooth start-up. On start-up, the line voltage prevents the pixel buffer from turning on and so the capacitor gets linearly discharged until current starts to flow progressively through the pixels.

This start-up approach is very gentle on the voltage supply and prevents fixed-pattern noise. The current sources for the S1 and S2 images have been made independent of each other in order to improve circuit symmetry.

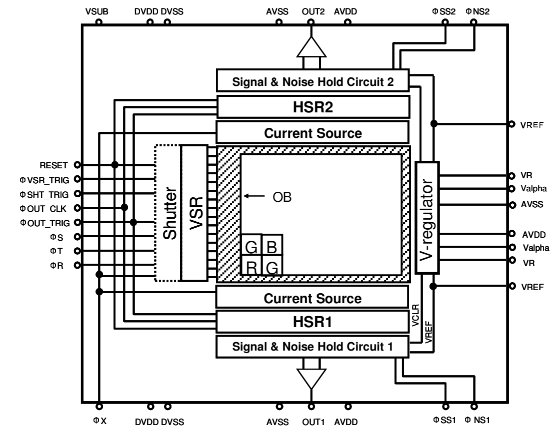


Figure 1, block diagram and pinout

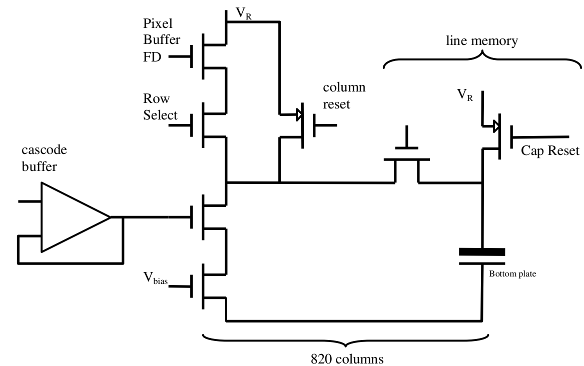


Figure 2, pixel current source

Line Memory

In order to reduce the effects of the common output bus, the capacitors are grouped in "segments" which are connected to the main bus through a switch (figure 5). This reduces dramatically the parasitic capacitance due to the capacitor switches and the lines connecting them to the output bus.

Dividing the image into segments usually causes fixed pattern noise making either each block distinguishable from the other or, in the most benign case, it produces artefacts (like vertical lines) around the segment swap. These effects are prevented by swapping the segments during the reset part of the output (figure 4) and minimizing crosstalk.

As a passive analog circuit, the line memory requires careful attention to layout parasitics and device sensitivities. All digital lines are symmetric in respect to the N-NS signals and the whole layout is designed to match the N and NS paths. Many other cross-talk counter measurements were also taken in the capacitor and segment layout.

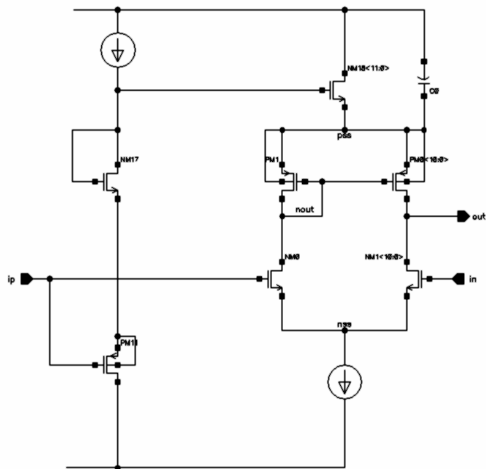


Figure 3, pixel current source, cascode buffer

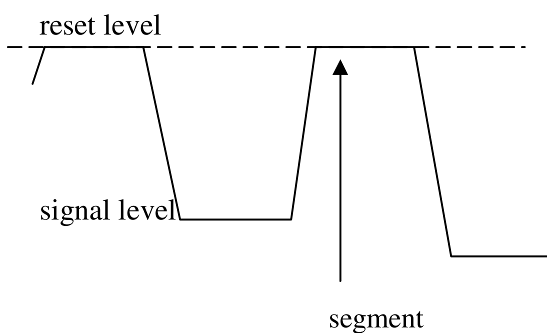


Figure 4, Segment change timing

Ground Layout

In order to avoid horizontal shading (figure 6) due to the pixel biasing, all ground lines from the pixel current sources are collected into a metal funnel whose voltage drop does not cause shading. This avoids the use of dynamic current mirrors [3] and low ρ metal layers.

As this funnel is laid out across the line memory up to the AVSS pin, the placement of the readout circuits had to be changed (figure 1) to reduce the risk of noise coupling. The new order takes into account that the noisiest element (the horizontal scanner) and the most sensible one (the pixel biasing) do not operate at the same time (figure 7).

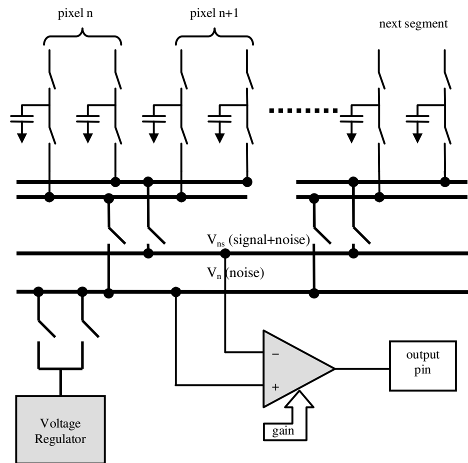


Figure 5, segmented line memory

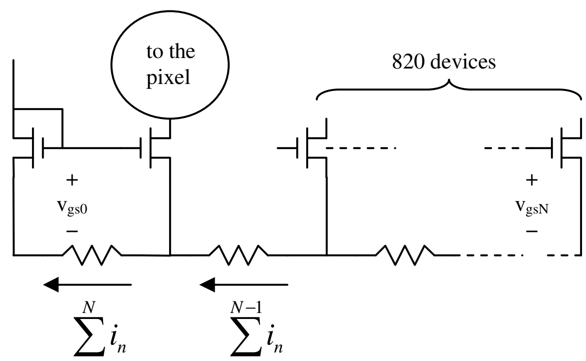


Figure 6 IR drops cause shading in the image

Voltage Regulators

The pixel voltage source is generated on the chip using a low drop out regulator (see figure 8). The line memory bus is reset using another regulator which is made of a simple buffer (figure 9). These regulators track AVDD to guarantee that there is enough headroom to operate the switches adequately.

Differential Amplifier

As the S1 and S2 images use different gains, a PGA (Programmable Gain Amplifier) was used. The amplifier is divided into three stages (figure 10): input buffer, current-mode gain stage and output buffer.
The PGA follows a fully differential architecture [4] for all the inner stages.

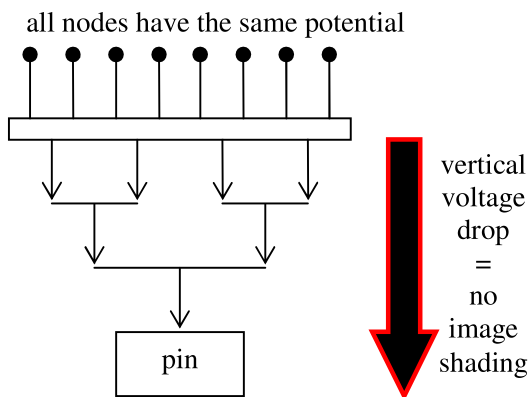


Figure 7, funnel layout

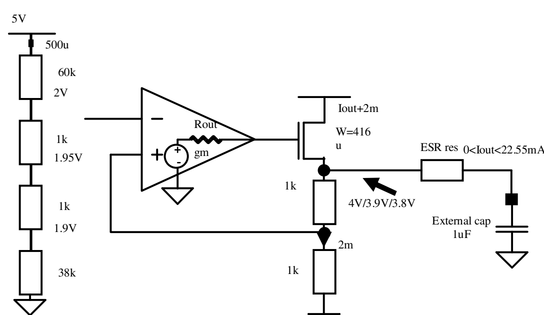


Figure 8, LDO Regulator

Results

This new implementation of the line memory results in a much higher data rate while reducing random and fixed pattern noise. Ghost images and shading due to saturated pixels have also been eliminated (figure 13) thanks to the amplifier-driven cascoded current source with funnel-shaped ground. Pixel linearity, too, is improved (figure 12) by it. On-chip voltage regulators and supply decoupling reduce fixed pattern noise and the use of a differential amplifier rather than two separate buffers highly increases the CDS effectiveness.

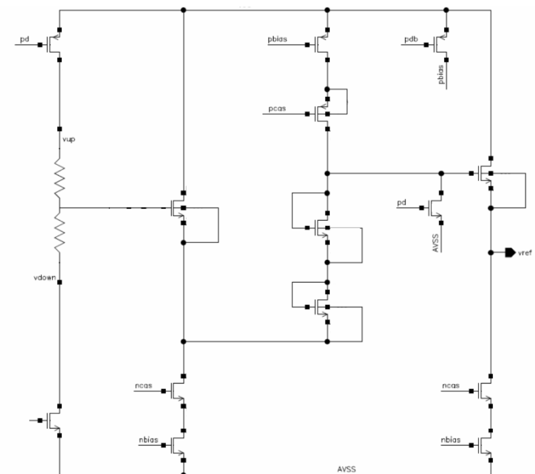


Figure 9, output bus reset voltage buffer

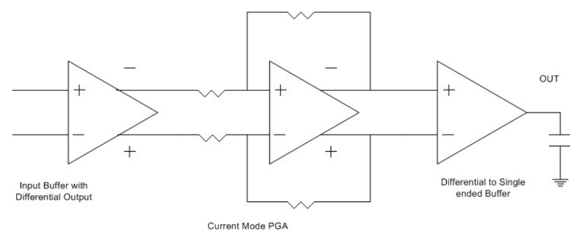


Figure 10, PGA block diagram

References

[1] S. Sugawa et al., 2005 ISSCC Dig. Tech. Papers, pp.352-353, 2005

[2] N. Akahane et al., IEEE J. Solid-State Circuits, vol.41, no.4, pp.851-858, 2006

[3] C. Toumazou et al. "*Analogue IC design: the current-mode approach*", chapter 7. ISBN-13: 978-0863412974

[4] Duque-Carrillo, J.F. et al., IEEE Trans. Electron Devices, vol.42, no.3, pp.190-192, 1995

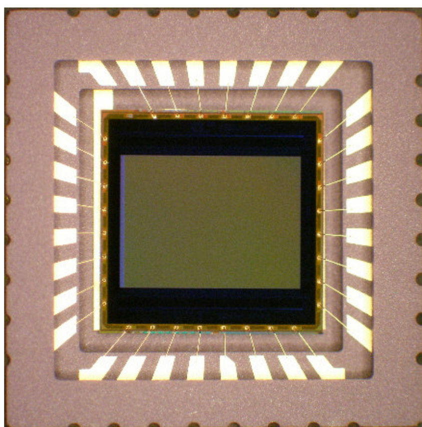


Figure 11, packaged chip

Table 1

Technology	2P3M CIS 0.18µm	
AVDD/DVDD	5	V
Effective pixels	800×600	
pixel pitch	5.6	µm
Frame rate	60	FPS
Pixel rate	36	MHz
Sensitivity	5.7	V/lux-s
Saturation voltage for S1 and S2	1.2	V
Dynamic range	93	dB
PRNU	0.8	%

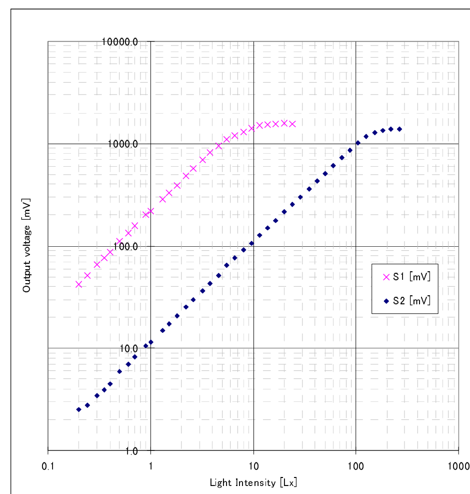


Figure 12, output voltage vs light

Figure 13, image sample

Monolithic Active Pixel Matrix with Binary Counters in an SOI Process

Grzegorz Deptuch
Brookhaven Nat. Lab., P.O. BOX 5000, Upton, NY, 11973, USA, deptuch@ieee.org, phone: 631 344 2615
Raymond Yarema
Fermi National Accelerator Laboratory, P.O. BOX 500, Batavia, IL, 60510, USA

Abstract:

The design of a prototype monolithic active pixel matrix, designed in a 0.15 µm CMOS SOI process, is presented. The process allowed connection between the electronics and the silicon volume under the layer of buried oxide (BOX). The small size vias traversing through the BOX and implantation of small p-type islands in the n-type bulk result in a monolithic imager. During the acquisition time, all pixels register individual radiation events incrementing the counters. The counting rate is up to 1 MHz per pixel. The contents of counters are shifted out during the readout phase. The designed prototype is an array of 64×64 pixels and the pixel size is 26×26 μm^2.

Introduction:

The best detector performances in imaging are achieved by providing an electric field in a depleted volume of a semiconductor detector and processing of information in each pixel. Processing functions require complementary transistors and sufficient space, not compromised with charge collecting elements, in each pixel. High resistivity (HR) substrate allows the depletion depths required for good detection efficiency, typically at a bias equal to a few tens of Volts. Unfortunately, HR substrates are not compatible with standard CMOS circuitry. Hence, both elements, i.e. detector wafers and readout chips are typically optimized and processed separately and connection is finally made using bump-bonding or similar process [e.g. 1]. The bump-bonding is expensive and troublesome. Silicon-on-insulator (SOI) process with a detector-grade silicon substrate allows fabrication of a monolithic imager fulfilling the requirements for optimisation of the detector and the processing electronics. The idea of using a thick silicon substrate as a detector volume and processing information in the electronics seated atop of it in an SOI process dates to early 90s [2]. These first attempts were not successful due to still not matured technology and cross-talks. The idea of a monolithic SOI detector was seized on later, resulting in fabrication of testable structures [3]. However, yield was rather poor, and due to the 3 µm technology, the pixel sizes were big with little integrated functionality.

Technology:

The current design is done in the 0.15 µm CMOS fully depleted SOI process by OKI, Japan [4]. The original CMOS process has been modified to include etching of vertical vias, smaller than 1 µm in diameter, in a 200 nm BOX. The resistivity of the silicon substrate is roughly 1 kΩcm. The vias are openings in BOX during source/drain implantation steps of the formation of MOS transistors, letting implants reaching the bulk [5]. Islands of p^+ or n^+ type are thus obtained avoiding additional implantation or annealing. The general concept of an SOI monolithic active pixel sensor (MAPS) on a HR silicon substrate is shown in Fig.1. The rectifying junctions are on the BOX side and reverse voltage is applied using a bottom Al plate and/or n^+ contacts on the top side.

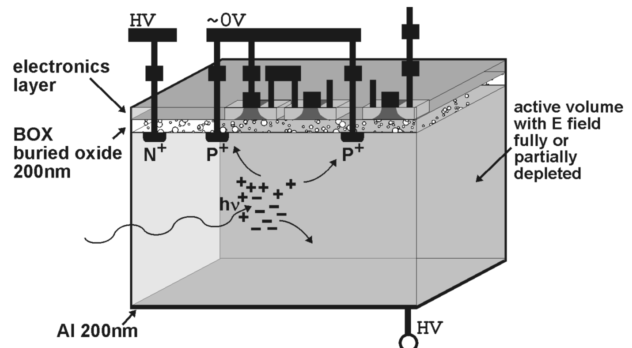


Fig. 1: Concept of a SOI monolithic active pixel sensor on a detector-grade high-resitivity silicon substrate.

A portion of the applied reverse bias is gradually distributed between the p^+ regions in the n-type bulk. This lateral gradient of potential in the surface zone leads to undesired shifts of the threshold voltage of transistors as the bulk may be seen as a back gate electrode. Respecting proper distances between diode implants and using as low as possible voltages for the reverse bias are required to minimize effects on transistors. It is worth noticing that voltage as low as 10 V is sufficient to deplete about 50 µm of n-type 1 kΩcm silicon. Remarkably, detector of this thickness is adequate for applications in high energy physics, electron microscopy and imaging of soft X-rays. The separation of 13 µm between diodes was chosen for the current design. The cross-section of the wafer part showing one pixel, peripheral circuitry and bias rings is shown in Fig. 2. The critical dimensions are shown in Fig. 2. The matrix of pixels extends to the right side. The thickness of the detector, delivered from the foundry, is 350 µm.

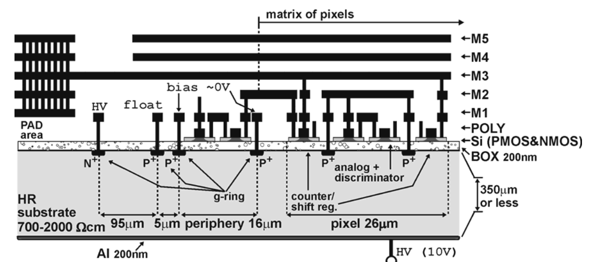


Fig. 2: Cross-section of the wafer part showing one pixel, peripheral circuitry and bias rings designed in the OKI 0.15µm SOI process.

Pixel Design:

Counting on a single event basis was chosen for the pixel operation, leading to a virtually noiseless image creation. The p-on-n type of the detector implies collection of holes. The pixel circuitry consists of a charge integrating preamplifier with a pole-zero cancellation block, an active continuous time CR-RC^2 shaping filter, a single threshold discriminator with positive feedback and a 12 bit, binary, ripple counter. A simplified schematic diagram of the pixel circuitry is shown in Fig. 3. The total continuous bias current of the processing chain is below 1 µA per pixel. The design makes use of three types of transistors available in the process, i.e. high V_T, low V_T and depletion transistors. The depletion NMOS transistors were used for floating capacitors in the design. The size of the pixel is 26×26 µm^2 and it contains 280 transistors.

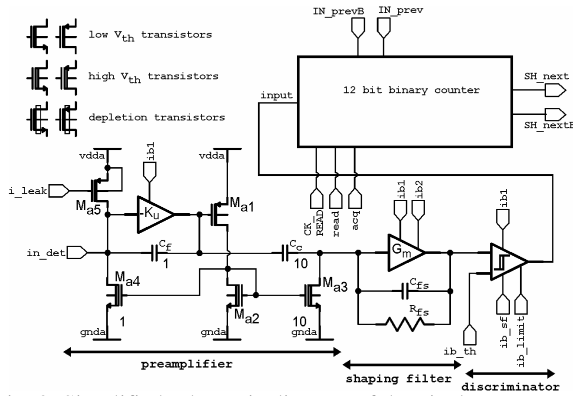


Fig. 3: Simplified schematic diagram of the pixel.

A basic, 12-bit, ripple counter architecture was used in the pixel. This crude counter configuration was chosen rather than the most area efficient pseudorandom counter [6] in order to be able to read directly pixel counts without decoding. The ripple counter was considered easier for handling and debugging during tests. A single bit cell of the counter is a static differential flip-flop built with only 12 transistors. Each cell is equipped with switches, to allow changing the configuration of individual counters in each pixel into a shift register for readout. Pixels are daisy chained and the readout is done with the external clock (*CK_READ*). During shifting out the contents of counters new initial values, typically all 0s, are shifted in to the matrix. A block diagram of the in-pixel counter configurable to a shift register and a block diagram of the single bit cell are shown in Fig. 4 and Fig. 5, respectively.

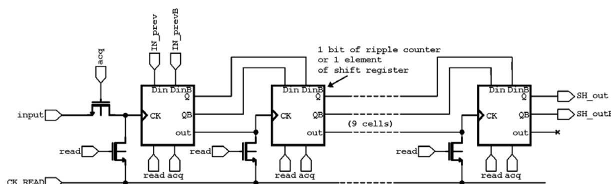


Fig. 4: Schematic diagram of the counter reconfigurable to the shift register.

A differential structure was chosen for the flip-flop in order to limit net cross-talk to the depleted volume underneath the BOX. The schematic diagram of the master/slave flip-flop is shown in Fig. 6. The use of only NMOS transistors as switches required a lowered power supply of 0.7 V for the counter, while the configuration selection is done with signals swinging from 0 to 1 V. All transistors in the counter are designed without connection to the bulk as it is allowed in an SOI process to save area.

The cascade of the preamplifier and the shaping filter provides an equivalent CR-RC^2 filtering with the peaking time equal to about 150 ns. The gain is nonlinear and the amplitude of time response saturates for input charge packets above 4×10^3 h$^+$.

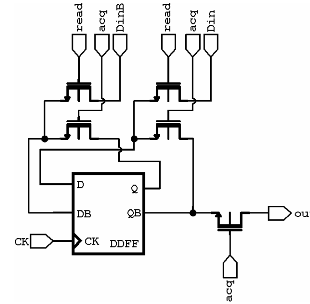


Fig. 5: Schematic diagram of the single bit cell of the counter.

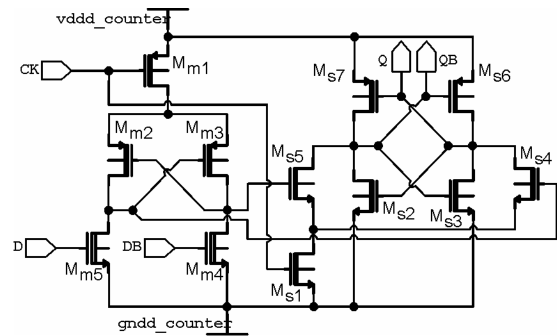


Fig. 6: Schematic diagram of the differential flip/flop used in the design of the counter.

The gain is about 300 µV/h$^+$ for signals in the order of 0.5×10^3 h$^+$, then it decreases to 200 µV/h$^+$ and 175 µV/h$^+$ for signals equal to 1.0×10^3 h$^+$ and 2.0×10^3 h$^+$, respectively. The simulated response of the analog chain for different input charge packets is shown in Fig. 7. The return to the baseline is always within 1 µs. Some undershoot is observed for higher signals due to the deviation of the transfer function from the ideal form.

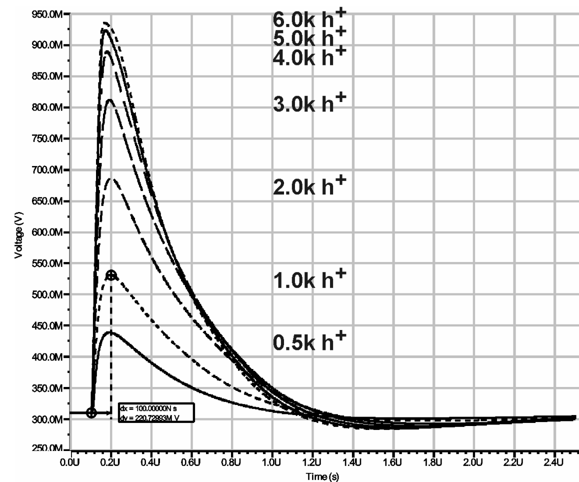


Fig. 7: Simulated response of the shaping filter.

The preamplifier is based on a simply common source inverting stage with a NMOS input transistor biased at a small current of 250 nA. The 5 fF feedback capacitor is used for charge integration. The coupling to the shaping amplifier is provided with a capacitor, whose value is scaled 10 times with respect to the integration capacitance

for gain. The preamplifier features a non-linear pole-zero cancellation circuit. The size of the input device is small, still fulfilling noise matching conditions, since the detector capacitance was estimated in the range of 10 to 20 fF. The leakage current of the detector that may be in the order of 100 fA is absorbed by the preamplifier. The pole-zero cancellation circuitry is self-adapting to the leakage current even above the expected levels [7]. The schematic diagram of the preamplifier is shown in Fig. 8. The preamplifier provides one pole in the transfer function, from the equivalent input capacitance, the feedback capacitance, MC_f, the transconductance of the input device, Ma_8, and the load capacitance, Ma_6. Large input charge packets may knock the amplifier out of normal operation for a long time compared to the shaping time. The role of the diode transistor, Ma_9, is to decrease risk of saturation of the preamplifier.

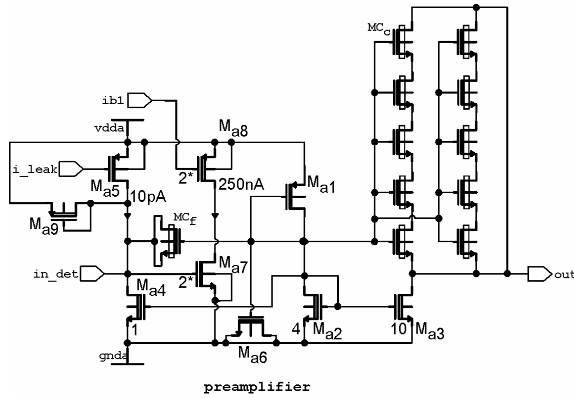


Fig. 8: Schematic diagram of the preamplifier.

The shaping filter is shown in Fig. 9. It uses the transconductance of a common source inverting stage with the NMOS transistor, Ms_1, the feedback capacitor Mc_{fs} and the high value feedback resistor MR_{fs}. The input transistor is biased at 125 nA. The required resistance of several tens of MΩs is obtained by biasing the transistor MR_{fs} at constant channel current, equal to 5 nA, and using its channel conductance as a resistance. The gate-source voltage of the transistor, MR_{fs}, is forced constant using a low pass filter realized with transistors MC_s and Ms_6.

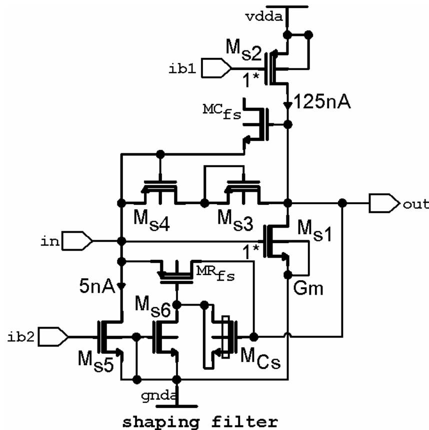


Fig. 9: Schematic diagram of the shaping filter.

Each transistor occupies its own island in a SOI process. This fact allows operation of a transistor without the body effect and is used in the design of the feedback resistance in the shaping filter. The gain limitation, described beforehand, is obtained with two diode-connected transistors Ms_3 and Ms_4. Their action is to decrease the equivalent feedback resistance for higher signal amplitudes. They turn on for output signals swinging approximately two threshold voltages above the baseline level. The simulated input referred noise of the analog chain is about 50 e^-. This value includes only thermal noise, since the model parameters for 1/f noise were not available during the design.

The core of the comparator, shown in Fig. 10, is a differential pair with outputs feeding a cross-coupled active load for adding positive feedback. This simple architecture provides a fast comparison result with some hysteresis for noise immunity. The dispersion of comparator offset voltages amidst the electronic noise is critical for a high purity discrimination of signals. The typical value reported in the literature [8] for a pixel design with a differential pair coupled comparator in a hybrid detector is $\sigma=90e^-$ referred to the amplifier input. The presented design features almost three times higher gain, thus the equivalent noise from the offset dispersion is expected to be accordingly reduced. Therefore, the current design uses only a global threshold for the comparator. Two source followers with matched layout, located at the input of the comparator, allow setting of the threshold voltage and provide individual baseline tracking for each pixel. The source follower with the transistor Md_1 is biased at low current. Its response is not linear for fast transient signals and it clips pulses from the shaping filter. The clipped signal is filtered with the low pass filter, built with transistors Md_5 and Md_7, and is used as a reference for the comparator. The second source follower with the transistor Md_2 is biased at higher current. The difference between gate-to-source voltages of transistors Md_1 and Md_2 defines the threshold for the comparator.

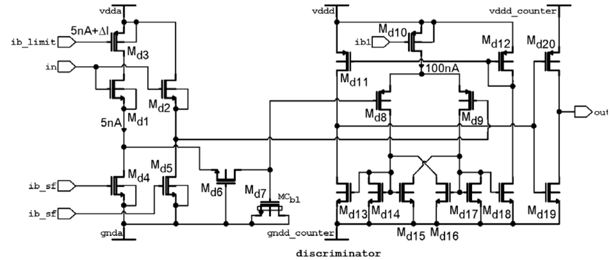


Fig. 10: Schematic diagram of the discriminator with individual for each pixel baseline tracking.

An example of the simulated discriminator response is shown in Fig. 11 for the input packet of 1.0×10^3 h^+ and the threshold current of 50 nA.

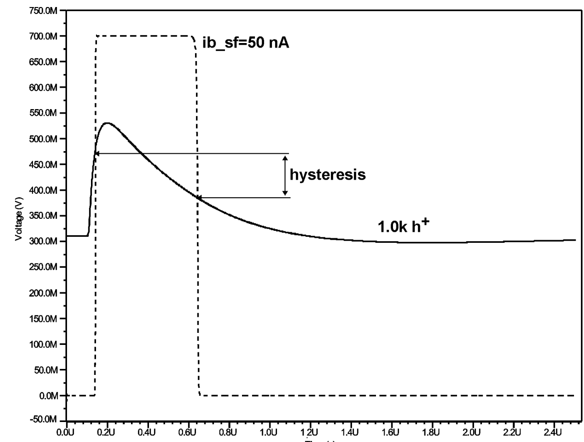


Fig. 11: Example of simulated response of the discriminator.

The analog part and the comparator operate from a single 1 V power supply. An inverter at the output of the comparator is used to adapt voltage levels for the counter. Critical transistors, like input devices of the preamplifier and the shaping filter or current sources were designed with bulk connections. The layout of the pixel is shown in Fig. 12. The central part of the pixel is occupied by the analog circuitry. There are four diodes with their anode terminals ganged and connected to the input of the preamplifier. The 12-bit counter occupies a ring around the analog part.

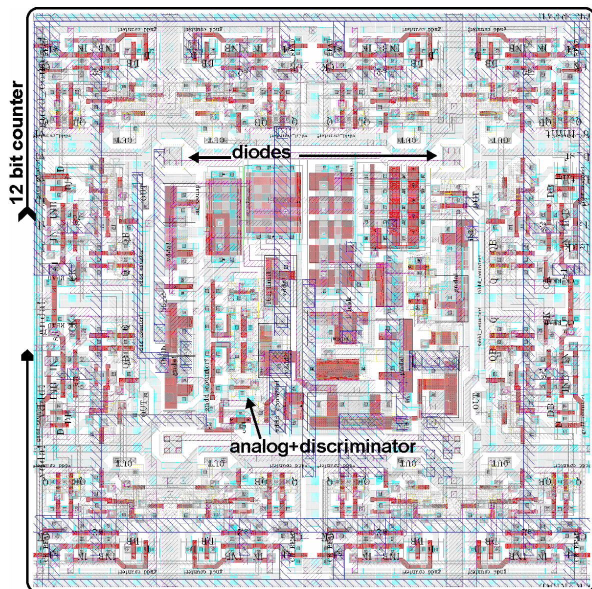


Fig. 12: Layout of the pixel.

Chip operation:

The data acquisition is done in two cycles, i.e. hit acquisition and readout. The selection of the cycle is done with external control signals. The readout of the chip is done through one differential output; the information has to be clocked through all pixels in the array. The maximum counting speed of the pixel counter is designed to be 1 MHz. The simulated response to the sequence of input pulses at 1 MHz rate is shown in Fig. 13. The first read cycle is used to reset the counter, and then the counter is counting comparator triggers in the hit acquisition phase. The second read cycle allows reading out the binary contents of the counter.

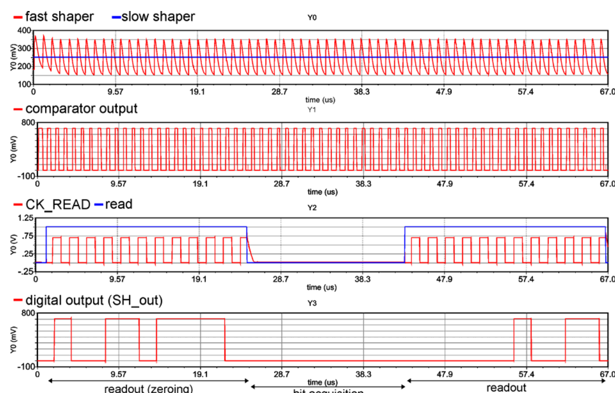


Fig. 13: Simulation of the shaping filter response, discriminator response, zeroing-counting-shifting out phases for the counter and the digital output of the pixel.

The tests of the 64×64 pixels chip are under preparation. The tests set-up is designed to allow installation inside a vacuum chamber of a transmission electron microscope. The system, consisting of two small PC boards, includes generation of all current and voltage biases, including high voltage for the reverse bias of the detector. Data transfer is done to PC with the USB 2.0 interface.

Conclusions:

The prototype called MAMBO (Monolithic Active pixel Matrix with Binary cOunters) is aimed at, but not limited to, applications of scientific imaging for direct electron detection in electron microscopy, and soft X-ray imaging in synchrotron radiation or bio-medical experiments. It is one of the first imagers fabricated in an advanced SOI CMOS process modified to the detector needs. The next generation of the imager may include some changes in the concept of the pixel, like use of pseudorandom counters or improvements in the comparator threshold distribution network including a baseline restorer. The analog core of the current pixel design may be considered as a *prêt-à-porter* solution for the particle tracking application in high energy physics using the SOI detector option. However, before this happens, an important test for this new detector technology will be assessment of coupling between the electronics and the fully depleted detector layer. The digital activity on the top layer may lead to induction of charge packets to which analog circuitry may be sensitive. If this undesired coupling takes place, the modification, consisting for example in screening blanket implantation close to BOX, will have to be studied and the process accordingly modified.

References:

[1] E.H.M.Heijne, “First operation of a 72k element hybrid silicon micropattern pixel array”, Nucl. Instrum. and Meth. A, 1994, Vol. 349, p. 138

[2] B.Dierickx, et al, “Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers”, IEEE Trans. on Nuclear Sci. 1993, Vol. 40, p. 753

[2] M.Amati, et al. “Hybrid active pixel sensors and SOI inspired option” Nucl. Instrum. and Meth. A, 2003, Vol. 511, p. 265

[3] H.Niemiec, et al, “Full-size monolithic active pixel sensors in SOI technology—Design considerations, simulations and measurements results”, Nucl. Instrum. and Meth. A, 2006, Vol. 568, pp. 153

[4] K.Morikawa, M. Mitarashi, “Low-Power LSI technology of 0.15 um FD-SOI”, OKI Technical Review Issue 196, Oct. 2003, Vol. 70, p. 60, http://www.oki.com/en/otr/196/downloads/otr-196-R15.pdf

[5] Y.Arai, et.al, “First Results of 0.15μm CMOS SOI Pixel Detector”, SNIC Symp., Stanford, CA, USA, 3-6 April 2006

[6] P.Fischer, “An area efficient 128 channel counter chip”, Nucl. Instrum. and Meth. A, 1996, Vol. 378, p. 297

[7] G.De Geronimo, et al., “Front-end ASIC for a GEM based time projection chamber”, IEEE Trans. on Nuclear Sci. 2004, Vol. 51, p. 1312

[8] C.Berg, et al., “Bier&Pastis, a pixel readout prototype for LHC”, Nucl. Instrum. and Meth. A, 2000, Vol. 439, p. 80

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Timepix, a 65k quantum imager readout chip for arrival time, energy and/or event counting measurements

X. Llopart, R. Ballabriga, M.Campbell, E.H.M. Heijne, L. Tlustos and W. Wong

CERN, CH-1211 Geneva (Switzerland)

Abstract-- **The Timepix is a single quantum processing chip capable of event counting, energy or arrival time measurements. The chip contains a 256 x 256 square pixel matrix covering a sensitive area of ~2 cm^2. It is controlled by an externally applied Shutter. Each pixel can be independently configured in one of four different modes: masked mode: pixel is off, counting mode: 1-count for each signal over threshold, TOT mode: the counter is incremented continuously as long as the signal is above threshold, and arrival time mode: the counter is incremented continuously from the time the first hit arrives until the end of the shutter. The chip uses an external clock with a frequency of up to 100 MHz as a time reference. Each pixel contains a Charge Sensitive Amplifier (CSA) which is sensitive to positive and negative charge, a discriminator with hysteresis and 4-bit DAC for threshold adjustment, synchronization logic and a 14-bit counter with overflow control. The pixel cell contains ~550 transistors, its dimensions are 55 x 55 µm^2 and the static power consumption is 13.5 µW per pixel. First measurements result in a sensitivity for a signal down to 750 e$^-$ corresponding to 2.7 keV energy deposition in a Si sensor.**

I. INTRODUCTION

The Medipix2 hybrid imager [1] has shown great potential in a range of applications with single quantum processing. When coupled to gaseous electron multiplication grids such as GEM [2] or Micromegas [3] the chip could be directly used to image events initiated by a single electron. The Timepix chip is an evolution from the Medipix2 which allows for measurement of arrival time, such as needed in a Time Projection gas Chamber (TPC), "time-over-threshold" (TOT) and/or event counting independently in each pixel. An external reference clock (*Ref_Clk*) is used in each pixel to increment the counter depending on the selected operation mode. The chip has the same size, readout architecture and floorplan as the Medipix2 allowing backward compatibility with the existing Medipix2 readout systems [4,5]. The architecture and functional behavior of the Timepix chip are described in this paper together with first electrical measurements and first images.

II. CHIP DESCRIPTION

Figure 1 shows the floorplan of the Timepix chip. To minimize non-sensitive area when butting together several chips, the peripheral circuitry is placed at the bottom of the chip and the sensitive area is placed at the top, with less than 50 µm of non-sensitive area between the last pixel and the chip edge. The sensitive area (top box) is arranged as a matrix of 256 x 256 pixels of 55 x 55 µm^2 resulting in a detection area of 1.98 cm^2 (87% of the entire chip area).

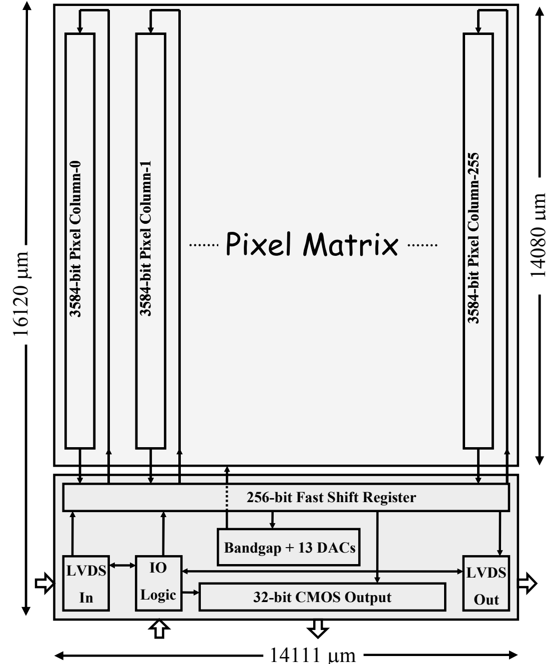

Figure 1: Schematic floorplan of the Timepix chip.

The analog part of the periphery contains one band-gap circuit [6] which generates a stable reference voltage for the 13 on-chip global DACs. There are eight 8-bit current DACs, four 8-bit voltage DACs and a single 14-bit voltage DAC which is used for the precise setting of the global threshold. The threshold DAC LSB corresponds to ~25 e$^-$. The digital part of the periphery contains all the Input/Output control logic, the IO wire-bonding pads and a 24-bit fused blown register for

unique chip identification. A full frame contains 917504 bits of data. At 100 MHz the LVDS serial read out takes <9 ms, or <300 µs in parallel through the 32-bit CMOS port. Independent 2.2 V analog (440 mW) and digital (450 mW) power supplies are used. The chip contains approximately 36 million transistors and is fabricated in a commercial 6 metal CMOS 0.25 µm technology.

III. The Pixel Cell

Figure 2 shows the schematic diagram of the Timepix pixel cell. Although the cell clearly resembles the Medipix2 pixel it has three main differences: there is only a single threshold with 4-bit adjustment, each pixel can be configured in 3 different operation modes, and the counting clock is synchronized with the external clock reference (*Ref_Clk*). As can be seen in Figure 3 the pixel is divided into two blocks. The analog side is made up of a Charge Sensitive Amplifier (CSA) and a discriminator (with polarity control pin) and 4 bit threshold adjustment. The digital side formed by the Timepix Synchronization Logic (TSL), a 14-bit shift register, a overflow control logic, the *Ref_Clk* pixel buffer, and an 8-bit Pixel Configuration Register (PCR). The PCR contains 4 bits for the pixel threshold equalization, 1 bit for Masking (*MaskBit*), 1 bit for enabling the test pulse input (*TestBit*) and 2 bits for selecting the pixel operation mode (*P0* and *P1*). The pixel cell contains ~550 transistors and the static power consumption per pixel is ~13.5 µW (in acquisition state and *Ref_Clk*=80 MHz).

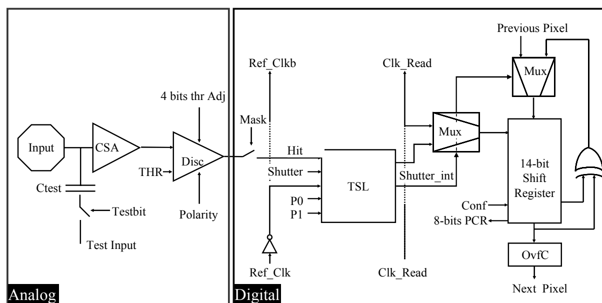

Figure 2: Timepix pixel cell schematic.

The externally applied Shutter defines two working states and is applied to all the pixels of the matrix simultaneously with a precision of ~5ns. If Shutter is high, an external clock is used to shift data from pixel to pixel. Either the 8-bit configuration register (PCR) is programmed or the 14-bit shift register is read out. For the exposure state the Shutter is low and the 14-bit shift register behaves as a linear feedback shift register counter with a single XOR tap with a dynamic range of 11810 counts. During exposure the pixel counter is incremented by the *Ref_Clk* depending on the settings of the pixel operation mode bits (*P0* and *P1*):

- *Event counting mode* (*P0*=0 and *P1*=0): Each event above threshold increments the counter by 1.
- *TOT mode* (*P0*=1 and *P1*=0): The counter is incremented continuously while the input charge is over threshold.
- *Arrival Time mode* (*P0*=1 and *P1*=1): The counter is incremented from the moment the discriminator is activated until the global Shutter signal is set high.

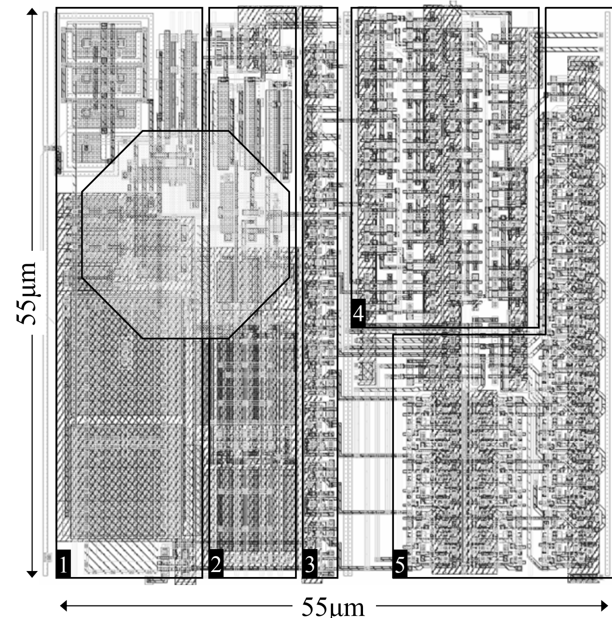

Figure 3: Timepix pixel cell layout: 1) CSA, 2) Discriminator with 4-bit threshold equalization, 3) 8-bit PCR, 4) *Ref_Clk* buffer and TSL and 5) 14-bit shift register and overflow control. Each pixel contains ~550 transistors.

A. Pixel analog section

Any charge either positive or negative collected on the octagonal 20 µm width pixel anode is integrated and compared to a global threshold. If the CSA output voltage crosses the threshold the output of the discriminator generates a pulse whose width corresponds to the length of time the CSA output voltage remains over threshold. The CSA follows the scheme proposed by Krummenacher [7] based on a cascoded differential CMOS amplifier. Global DACs control the front end. The CSA output peaking time can be set from 90 ns to 180 ns by the Preamp DAC. The return to zero of a ~10 ke$^-$ input charge can be adjusted from 500 ns to 2500 ns depending on Ikrum DAC settings. The DC output level of the CSA is controlled by the Vfbk voltage DAC and it is used to maximize the output voltage dynamic range depending on input charge polarity. Detector leakage currents in both

polarities, of up to Ikrum/2 per pixel, are compensated by the feedback loop of the CSA. The amplifier gain in the default DAC settings is ~16.5 mV/ke$^-$ with a linear voltage dynamic range up to ~50 ke$^-$. The CSA output is DC coupled to the discriminator. The discriminator contains an input multiplexer with Polarity control, a transconductance amplifier, four independent selectable current sources for threshold equalization, and a current discriminator with hysteresis. Total analog power is ~6.5 µW and area is 55 x 25 µm^2.

B. *Pixel digital section*

The analog output from the discriminator (Hit) is buffered and gated with the *Maskbit* at the entrance of the Timepix Synchronization Logic (TSL). The pixel operation mode bits (*P0* and *P1*) configure each pixel TSL in three different modes. In the acquisition state (i.e. Shutter is low) the TSL synchronizes the Hit and the Shutter with the *Ref_Clk* to generate a glitch free counting clock signal depending on the operation mode. The counter is stopped if the number of counts reaches the overflow limit of 11810 counts. The TSL core uses an asynchronous network of SR flip-flops with race-free state assignment designed with controlled initialization. The TSL core is only active when a Hit is present. The pixel digital part contains ~500 minimum-sized transistors and occupies an area of 55 x 30 µm^2.

C. *The reference clock*

The Timepix chip uses an externally generated tunable clock reference (*Ref_Clk*) as counting clock which is distributed throughout the pixel matrix. To reduce the effects of capacitive coupling and to optimize the digital power balance of the *Ref_Clk* distribution into the full matrix, each pixel includes a minimum-sized inverter to buffer the *Ref_Clk* to the next pixel up in the column. Furthermore, to minimise the digital coupling and to uniformly distribute the digital power, the *Ref_Clk* phase is alternated between columns. With a simulated propagation delay of 195 ps per pixel buffer the *Ref_Clk* is distributed to all the pixels in less than 50 ns. With a *Ref_Clk* of 80 MHz the measured digital power consumption due to clock distribution into the pixel matrix is ~450 mW.

IV. THRESHOLD EQUALIZATION

Threshold equalization is used to compensate the pixel to pixel threshold variations due to local transistor threshold voltages and current mismatches and/or more global effects like chip power drops. This compensation is done by means of a 4-bit current DAC placed in the discriminator chain of each pixel. The current range of this DAC is controlled by the THS global DAC with a LSB range of 0-40 nA. The measured INL of this 4-bit DAC in the full pixel matrix is less than 0.8 LSB. To determine the equalization mask the threshold distribution for each of the 16 threshold adjustment codes is measured. Then the adjustment code is selected for each pixel to make its threshold as near as possible to the average of the threshold distribution mean values. The threshold variation before equalization is ~240 e$^-$ rms and after equalization the achieved threshold variation is ~35 e$^-$ rms for both polarities. The minimum detectable charge is defined as the smallest input charge which all pixels are able to resolve when the global threshold is set just over the noise. This depends on the electronic noise and the uncorrelated threshold variation. Before equalization the minimum detectable charge for the full pixel matrix of a *naked* chip (i.e. without sensor material) is ~1600 e$^-$ and after equalization is ~650 e$^-$ for both polarities. This compares favorably with the ~900 e$^-$ measured in Medipix2 [8].

V. CHARACTERIZATION USING RADIOACTIVE SOURCES

Recently the first *Timepix* chips bump bonded to a 300 µm high resistivity Si sensor became available. An absolute energy calibration of a *Timepix* chip was realized using X-ray quanta from ^{109}Cd and a ^{55}Fe sources as shown in Figure 4.

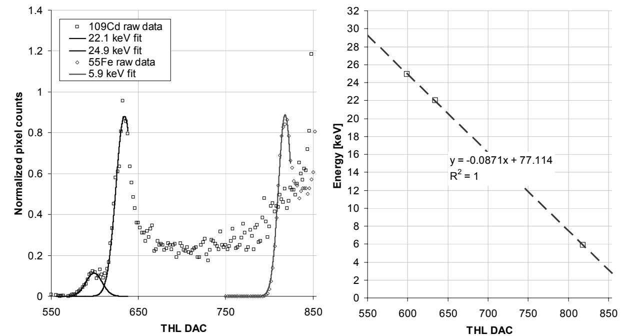

Figure 4: Energy calibration of a *Timepix* bonded to a 300 µm high resistivity Si sensor. ^{109}Cd (with 22.1 and 24.9 keV emission lines) and ^{55}Fe (with a main 5,9 keV emission line) X-ray sources are used as energy references. On the right figure, the measured calibration slope is ~87 eV per THL DAC step with a full chip minimum detectable charge of ~2.7 keV.

The effective energy threshold is calculated by scanning the THL DAC over the main emission lines of both X-ray sources (i.e. 22.1 and 24.9 keV for ^{109}Cd and 5.9 keV for ^{55}Fe). The pixel matrix is configured in event counting mode in order to exploit the linear response of the measured effective threshold. The measured slope is linear with a gain of ~87.1 eV or, in

electrons, ~24.2 e^- per THL DAC step. The minimum detectable charge for the full chip is ~2.7 keV or ~750 e^- for this setup. The measured ENC is ~113 e^- rms for the chip bump bonded to the sensor which is ~16% higher compared with a naked chip.

VI. First Images

First images have been taken with different pixel operating modes, both collection polarities and detector types. Figure 5 shows a recorded event in TOT and arrival time mode being the chip coupled to a GEM gas gain grid in electron collection polarity (negative input). The image in Figure 6 is realized with a chip bonded to a 300 µm thick Si sensor working in event counting mode in hole collection polarity (positive input).

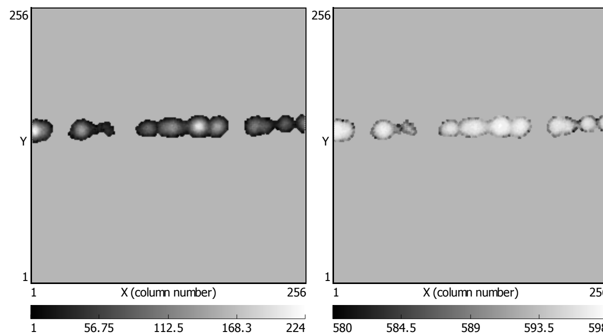

Figure 5: Image of trail of electrons left in gas volume after passage of swift ionizing particle. The full pixel matrix is in mixed-mode: alternating pixels are configured in TOT mode and in arrival time mode. After readout, two images are generated from the same event using linear interpolation: On the left a TOT measurement, and on the right the arrival time measurement. Data taken during a test beam in DESY (Hamburg, November 2006).

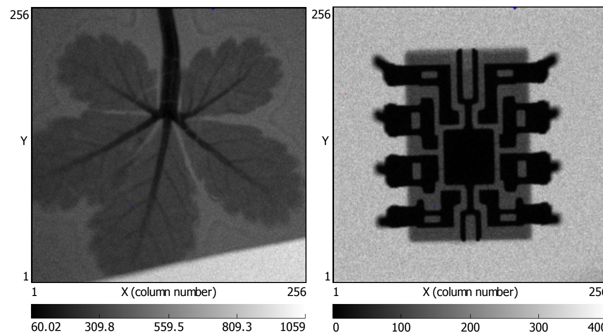

Figure 6: On the left, image of a leave under Kapton tape using a ^{55}Fe X-ray source (5.9 keV) with an acquisition time of 600 s. On the right, image of an 8-pin DIL chip using a ^{109}Cd X-ray source (22.1 and 24.9 keV) with a total acquisition time longer than 5 hours. In both images the threshold is set ~3 keV.

The TOT functionality has been further explored with a calibrated chip bonded to a Si sensor using a ^{241}Am radioactive source. The ^{241}Am source emits α radiation with an energy around 5.5 MeV together with γ radiation (i.e. photons) with main energy lines at 13.9 and 59.5 keV. Figure 7 shows on the left a full 2D image using a *Shutter* time of a 100 ms at a threshold of ~3.1 keV (THL=850). Large pixel clusters, with typically ~25 pixels, are the result of the charge deposition by single α particles due to its high energy. The small pixel clusters (1-4 pixels) are the result of the detection of gamma radiation. The 3D plot on the bottom right of Figure 7 shows the charge information measured with the TOT method. The central pixel in the large clusters has typically ~4000 counts which correspond to a pulse width of ~85 µs at *Ref_Clk* = 47.3 MHz and $Ikrum_{DAC}$=5. As each large cluster corresponds to depositions of single α radiation of ~5.5 MeV, the measured charge in the central pixels is then ~2.3 MeV or ~635 ke^-.

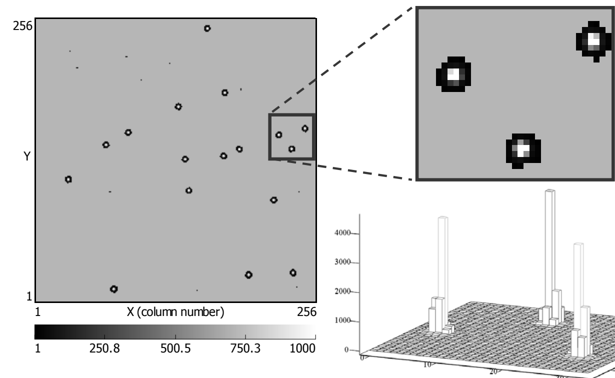

Figure 7: On the left is shown TOT raw data for the full chip exposed to a ^{241}Am radioactive source with 100 ms exposure time. The large pixel clusters are the result of the charge deposition by single α particles (above 5 MeV). Three α clusters are shown in the 3D plot revealing the energy information. The single hits are due to the ^{241}Am γ radiation (mainly 13.9 and 59.5 keV). The threshold is set ~3.1 keV, and *Ref_Clk* = 47.3 MHz.

VII. References

[1] X. Llopart et al, “Medipix2, a 64k pixel readout chip with 55 µm square elements working in single photon counting mode”, IEEE Trans. Nucl. Sci., vol. 49, iss. 5, (2002), pp.2279-2283.

[2] P. Colas et al, “The readout of a GEM or Micromegas-equipped TPC by means of the Medipix2 CMOS sensor as direct anode”, Nucl. Instr. Meth. A, vol. 53, iss. 1-2, (2004) pp. 506-510.

[3] H. van der Graaf et al, “Detection of single electrons by means of a Micromegas-covered Medipix2 pixel CMOS readout circuit”, Nucl. Instr. Meth. A, vol. 540, iss. 2-3, (2005), pp. 295-304.

[4] D. San Segundo et al, “An interface board for the control and data acquisition of the Medipix2 chip”, Nucl. Instr. Meth. A, vol. 509, Issues 1-3, (2003), pp.164-170.

[5] T. Holy et al, “Data acquisition and processing software package for Medipix2”, Nucl. Instr. Meth. A, vol. 563, Issue 1, (2006), pp. 254-258.

[6] K.E.Kuijk, “A precision reference voltage source”, IEEE Journal of Solid-State Circuits, vol. Sc-8, iss. 3, (1973), pp. 222-226.

[7] F. Krummenacher, “Pixel Detectors with Local Intelligence: an IC Designer Point of View”, Nucl. Instr. Meth. A, vol. 305, (1991), pp. 527-532.

[8] X. Llopart, “Design and characterization of 64K pixels chips working in single photon processing mode”, PhD Thesis, Mid Sweden University, (2007), pp. 98.

Dichromatic self-timed spectral measurement circuit with digital output in vanilla CMOS

Daniel B. Fasnacht, Tobi Delbruck

Inst. of Neuroinformatics
UNI-ETH Zurich, Switzerland
dfasnacht@student.ethz.ch, tobi@ini.phys.ethz.ch

Prior work [1-4] has shown that ordinary (vanilla) CMOS can spectrally separate photons using the shallow source-drain and deep well junctions (Fig 1) and that a color imaging sensor and self-timed readout structure can be built to read out these signals Here we show our first implementation of a self-timed circuit with digital output that encodes the spectral content (long vs. short wavelength content) as PWM duty cycle and the total photocurrent as PWM frequency, as in [4], but using vanilla CMOS instead of a bipolar process. This circuit is a step towards building color sensitive vision sensors using commodity CMOS processes. The potential advantage of vanilla CMOS is that it avoids the use of high-cost, low availability specialized process flows with integrated color filters, thus allowing more rapid and affordable prototyping of experimental circuits and faster evolution of new architectures.

Longer-wavelength photons penetrate more deeply. The shallow diode (U) is more sensitive to short wavelength light and the buried diode (L) is more sensitive to longer wavelengths. The ratio of the two different photocurrents is a strong function of wavelength and can provide information about the color. Because U and L diodes share the n-type region (well) and one node is "hardwired" to ground (substrate), it is hard to separate the two currents. The current of the U diode is available at the active node. The only other available current is the current at the well node, which is the sum of U and L photocurrents. If both currents were allowed to flow continuously, the photocurrent of the L diode would have to be calculated by somehow subtracting the upper current from the summed current. Because such a calculation is mismatch-prone, we measure the ratio of photocurrents by reverse-biasing both photodiodes and then letting the photocurrent discharge the U and then the L diode (Figs. 2&3). We output a signal that is low during the discharge of the U diode and high during the discharge of the L diode. The duty cycle of this signal contains the information about the long versus short wavelength content of the incident light. To generate this signal we use a self-timed control circuit (Fig. 4). This circuit implements the comparators that determine state transitions and the state machine. The design of the circuit ensures that it cannot get stuck in a parasitic state. The control circuit outputs the switch signals ϕ_n and ϕ_p.

This circuit was fabricated in a 0.5u 3M 2P 5V process. Fig. 5 shows a die photograph and Fig. 6 shows the layout of the 100x100 um^2 photodiode and control circuit, along with two poly capacitors used for characterization.

Fig. 7 shows the measured spectral response and Fig. 8 shows that the duty cycle is invariant to absolute illumination over at least 5 decades, while the frequency is proportional to illumination. Under 500 lux fluorescent illumination, the duty cycle is about 25%, while the frequency is about 150 Hz. The duty cycle varies from 50% to 7% over a wavelength range 400 nm to 750 nm. Fig. 9 shows scope traces of circuit nodes with two different pure spectral illumination conditions; the discharge rate of the A node increases when wavelength is decreased.

Circuit power consumption is about 20 uW under indoor illumination conditions; at this bias level, the circuit can run up to 90 kHz. Mismatch in response duty cycle and frequency as measured over 5 chips is under 1%. This low mismatch is due to low variability of capacitance values and independence of behavior on absolute threshold voltages.

Future developments will integrate small arrays of these circuits with self-timed readout and processing circuits for applications in low-resolution color-based visual recognition tasks.

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[1] R. F. Wolffenbuttel and P. P. L. Regtien, "A novel approach to solid state color sensing," *Sens. Actuators*, vol. 9, pp. 199-211, 1986.
[2] R. F. Wolffenbuttel, "Color filters integrated with the detector in silicon," *IEEE Electron Device Letters*, vol. EDL-8, pp. 13-15, 1987.
[3] R. F. Wolffenbuttel and G. D. Graaf, "Performance of an integrated silicon color sensor with a digital output in terms of response to colors in the color triangle," *Sens. Actuators A*, vol. 21-23, pp. 574–580, 1990.

[4] R. F. Wolffenbuttel and G. d. Graaf, "Light-to-Frequency Converter Using Integrating Mode Photodiodes," *IEEE Journal of Solid State Circuits*, vol. 46, pp. 933-936, 1997.

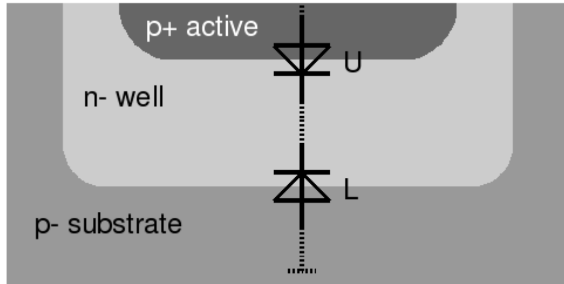


Figure 1. CMOS cross section.

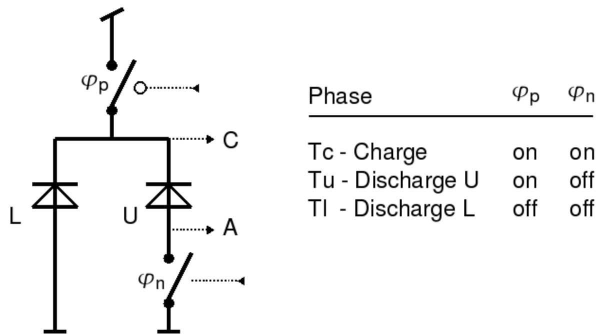


Figure 2. Control states.

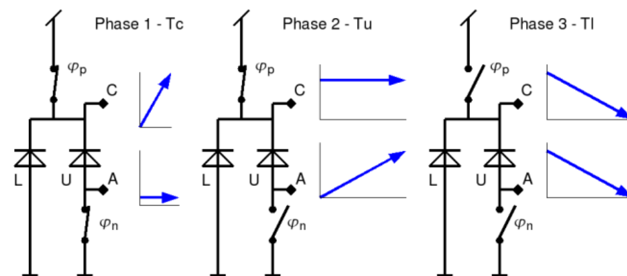


Figure 3. Cyclic operation phases.

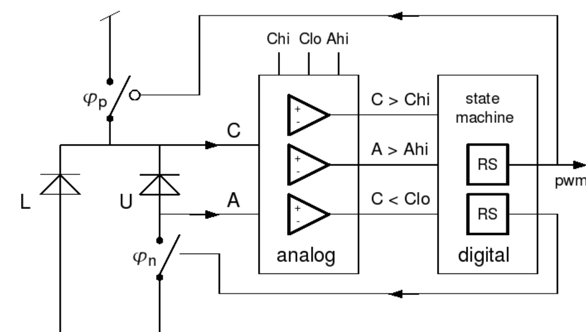


Figure 4. Control circuit schematic.

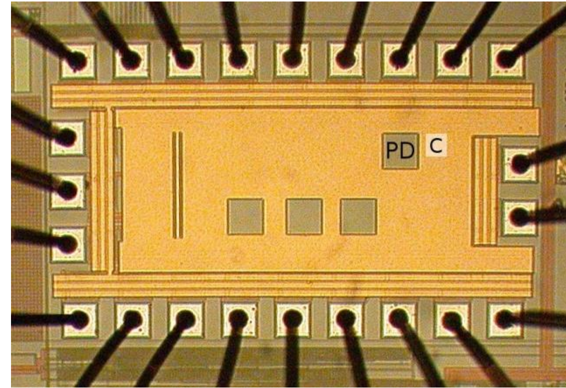


Figure 5. Die photo. PD=photodiode, C=control circuit.

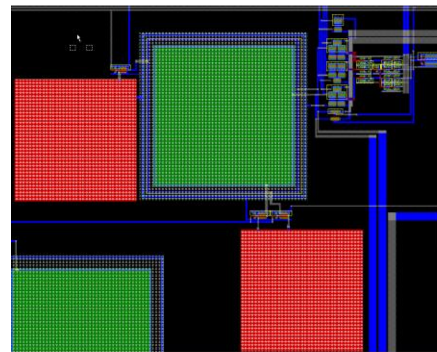


Figure 6. Layout including test capacitors.

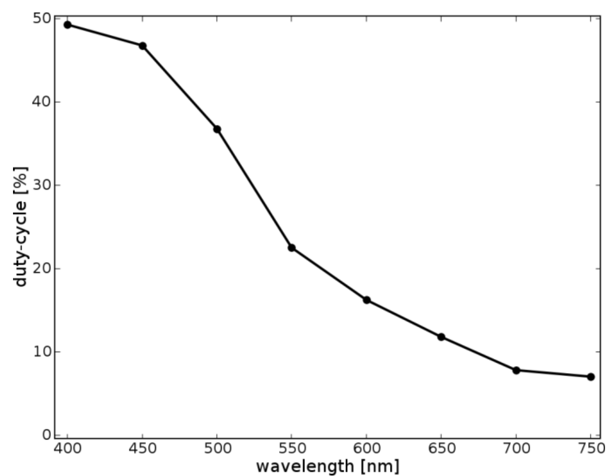


Figure 7. Spectral response.

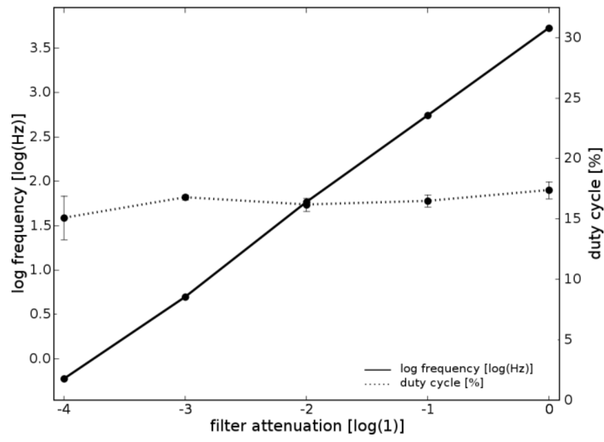


Figure 8. Invariance of duty cycle to illumination.

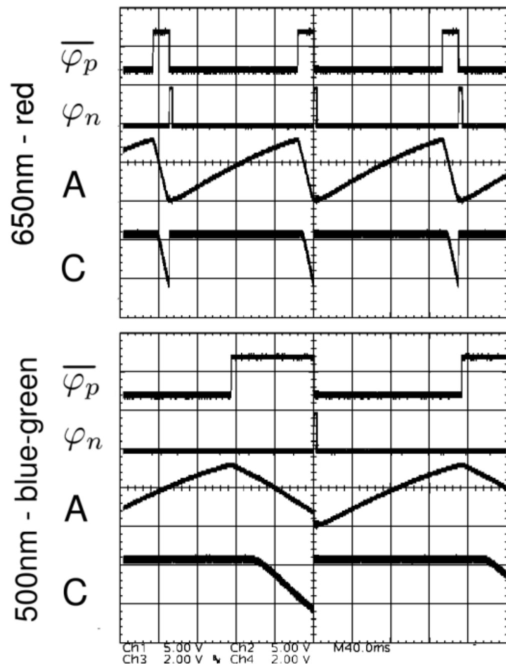


Figure 9. Scope traces.

High speed 2D motion detection image sensor with velocity filtering function

Toshiyuki Sugita , Kenichi Nakayama , Takashi Yoshida , Takayuki Hamamoto
Tokyo University of Science
1-3 Kagurazaka, Shinjuku-ku, Tokyo 162-8601, Japan
{sugita, nakayama, hamamoto}@isl.ee.kagu.tus.ac.jp

Kazuya Kodama
National Institute of Informatics
2-1-2, Hitotsubashi, Chiyoda-ku, Tokyo 101-8430, Japan
kazuya@nii.ac.jp

1. Introduction

We propose a method of objects tracking implemented on a smart image sensor. The proposed method uses not a normal block-based approach but a pixel-based approach using frame difference between neighbor pixels. In general, the methods of block-based matching are used for objects tracking systems [1]–[4]. However, the methods need large quantity of calculation to control the block size adaptively. Therefore, the block-based matching cannot be performed on a smart image sensor at a high frame rate.

In this paper, we describe new smart image sensor on which the proposed method is implemented. Because the sensor uses strong inter-frame correlation by high speed imaging, the 2D moving vector (direction and speed) can be detected into a limited area. Therefore the processing can be done by small column-parallel circuits on the sensor. Further, the sensor can detect various speeds by changing the processing interval of the detection.

2. Algorithm of on-sensor 2D motion detection

2.1 Detection of moving direction

In general, the moving pixel can be detected by comparing the frame difference of same position with a threshold as shown in Fig. 1(a). The difference between frames f and f-1, $d_{x,y}$, is given by Eq.(1).

$$d_{x,y} = \left| l_{f:x,y} - l_{(f-1):x,y} \right| \quad \ldots(1)$$

where $l_{f:x,y}$ and $l_{(f-1):x,y}$ represent pixel values at (x,y) of frames f and f-1 respectively. Motion of each pixel can be detected with $d_{x,y}$, but the velocity can't be directly detected only with $d_{x,y}$.

For detection of the direction and speed, frames f and f-1 are compared by shifting the position of

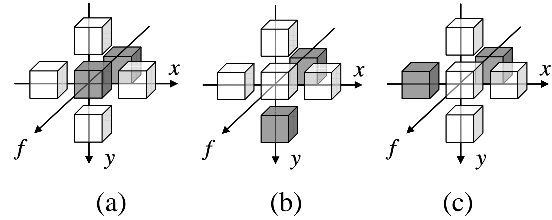


Fig.1 Detection of optical flow by frame difference; (a) without shift, (b) shift to the down, (c) shift to the left.

reference to one of the neighbor pixels as shown in Figs. 1(b) and (c). The evaluation values for directions of top, bottom, right, and left are calculated by using Eqs. (2a)–(2d) as well as Eq. (1).

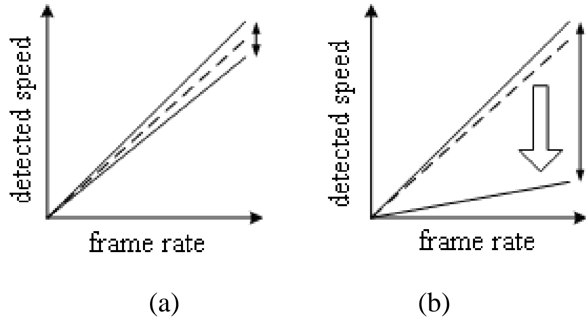
$$m_{up} = \left| l_{f:x,y-1} - l_{(f-1):x,y} \right| \quad \ldots(2a)$$

$$m_{down} = \left| l_{f:x,y+1} - l_{(f-1):x,y} \right| \quad \ldots(2b)$$

$$m_{right} = \left| l_{f:x+1,y} - l_{(f-1):x,y} \right| \quad \ldots(2c)$$

$$m_{left} = \left| l_{f:x-1,y} - l_{(f-1):x,y} \right| \quad \ldots(2d)$$

By controlling the frame rate of an image sensor, the movement quantity between two frames is adjusted to equal to or less than 1 pixel. If an object moves to a certain direction, the evaluation value of the correct direction is smaller than the other values. The optical flow for each pixel is detected by using these four values with shifting and the value without shifting. In actual, the correct moving direction is determined for vertical and horizontal directions separately.



(a) (b)

Fig.2 Relationship between detected speed and frame rate; (a) normal imaging, (b) extension of detected speed.

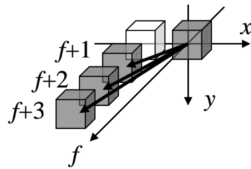
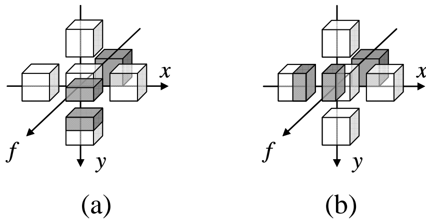


Fig.3 Interval of detecting optical flow.



(a) (b)

Fig.4 Detection of optical flow by using the pixel values of decimal accuracy; (a) 1/2 shift to the down, (b) 1/2 shift to the left.

This method is applied to the pixels in not plain part but edge part. Therefore, the edge detection is processed before the comparison.

2.2 Detection of moving velocity

2D moving direction is simply detected by the above mentioned method based on frame difference. In the method, there is a correlation between a frame rate of sensor and a speed of object. Because the moving distance between two frames is limited into about 1 pixel, there is a most suitable frame rate to detect the speed of the motion. In this method, the detectable speed range can be controlled on the sensor and moved to lower speed by two methods as shown in Fig.2. One is changing the reference timing for the frame difference from next frame to later frames and the other is changing the reference pixel position from neighbor pixel to interpolated pixels.

2.2.1 Control of the reference timing

By changing the frame rate, the detectable range of speed can be controlled. In place of controlling the frame rate, motion detection is processed repeatedly during k frames in the sensor. The moving speed can be calculated from the interval between the basis frame and the detected reference frame. As shown in Fig. 3, when the motion is detected at frame $f+3$, the detected speed is one third of the maximum speed.

2.2.2 Control of the reference pixel position

The method of detecting an optical flow compares the values of frame difference with or without shifting the reference pixel. In the method, if the moving distance for the frame interval is near 1 pixel, the speed can be calculated from the frame rate. However, the accuracy of the detection is degraded for the object that is moving at a different speed. Therefore, the pixel values of a decimal position are estimated and used to detect the speed as shown in Fig. 4. We adopt 1/2 pixel accuracy for the detection by consideration of the calculation amount. Therefore moving direction is detected by using four values shown in Eqs. (3a)–(3d).

$$m_{up1/2} = \left| \frac{(l_{f;x,y-1} + l_{f;x,y})}{2} - l_{f-1;x,y} \right| \quad \ldots(3a)$$

$$m_{down1/2} = \left| \frac{(l_{f;x,y+1} + l_{f;x,y})}{2} - l_{f-1;x,y} \right| \quad \ldots(3b)$$

$$m_{right1/2} = \left| \frac{(l_{f;x-1,y} + l_{f;x,y})}{2} - l_{f-1;x,y} \right| \quad \ldots(3c)$$

$$m_{left1/2} = \left| \frac{(l_{f;x+1,y} + l_{f;x,y})}{2} - l_{f-1;x,y} \right| \quad \ldots(3d)$$

3. Further processing of motion detection in depth axis

By using the detected 2D motion velocity, the moving direction in the depth axis can be estimated using an outside FPGA. In a depth axis, the shorter distance between an object and a sensor is, the larger the object's size is. In this method, the moving direction is detected by using the change of the object size.

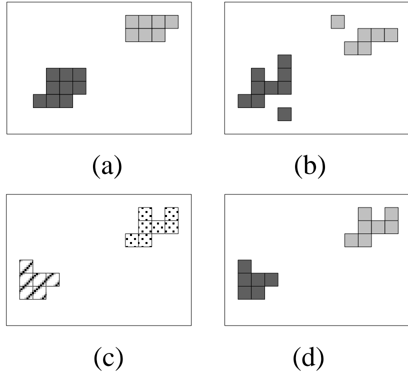


Fig.5 Correspondence of motion regions; (a) detected position in frame *f*, (b) predicted position in frame *f*+*k*, (c) detected position in frame *f*+*k*, (d) result of correspondence.

In order to detect the size change, this method uses the results of the detected moving velocity in the X-Y plane to correspond objects in current frame *f*+*k* with the objects in the previous frame *f*. As shown in Fig 5(a), motion regions are first extracted by grouping the pixels of which the motions are detected in the X-Y plane at frame *f*. The positions at frame *f*+*k* for the pixels in the motion regions are predicted by using the results of moving velocity in X-Y plane as shown in Fig. 5(b). Using the predicted positions, the motion regions extracted at frame *f*+*k*, as shown in Fig. 5(c), can be corresponded with the motion regions at frame *f* (Fig. 5(a)). The results of correspondence are represented by the same colors of the motion regions shown in Figs. 5(a) and 5(d). Then the number of pixels at frame *f* is compared with the number at frame *f*+*k* in each corresponding region. If the number increases or decreases, it is decided that the object is moving forward or backward respectively.

4. Evaluation of the proposed method

We evaluated the proposed method by simulation using some moving images captured at 1000fps by a high speed camera. Fig.6 shows the results of 2D moving direction and speed. In Figs. 6(c) and (d), the darker pixels than a brightness of the background represent moving to right, and the brighter pixels represent moving to left. In addition, the larger the color difference between the detected pixel and background is, the higher the speed is. In these images, two objects were moving to different directions each other as drawing a character “8”. As shown in Figs. 6

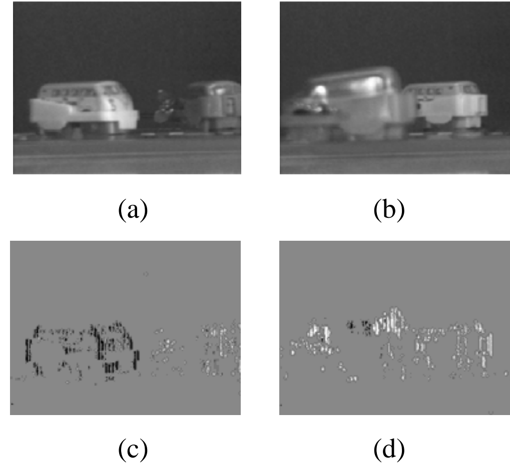
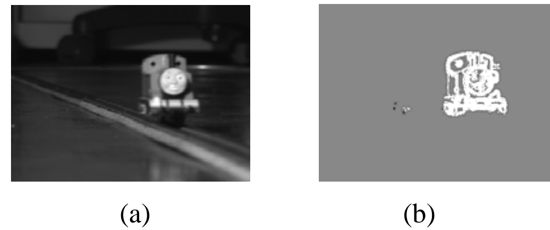


Fig.6 Simulation of the motion detection in the X-Y plane; (a)original image (left object moved to the right, right moved to the left), (b)original image(both objects moved to the left), (c)result of (a), (d)result of (b).



(a) (b)

Fig.7 Simulation of the motion detection in depth axis; (a)original image, (b)result of (a).

(c) and (d), the moving direction and speed for the pixels of the objects were detected reasonably. Fig. 7 shows an example frame of the sequence and the detected moving direction in the depth axis. In this image, an object was moving straight from left backward to right forward. In Fig.7(b), the darker pixels represent moving to backward, and the brighter pixels represent moving to forward. The moving direction of the object was detected correctly.

5. Design and fabrication of new image sensor

We have designed new image sensor on which the 2D motion detection function is implemented. The prototype chip was fabricated using a 2-poly 4-metal 0.35um CMOS process. This chip consists of eight parts as shown in Fig.8. They are APS array,

temporary memories for 3 lines, detecting edge pixels, detecting motion, memory array for the positions of the edge pixels, memory array for the pixel values of first basis frame, and counter. Table 1 shows the outline of the prototype chip and Fig.9 shows the photograph of the chip.

The following is the flow of processing on this prototype chip. First, the luminance values of pixels are readout from the APS array and are stored in the memories for 3 lines temporarily. If the current frame is the first frame (basis frame) of the motion detection, the luminance values are also stored in the memory array for the image of basis frame in the same way. Using the luminance values of the central pixel and 4 neighbor pixels located on the left, right, top, and bottom stored in the temporary memories for 3 lines, the edge intensity is calculated in the edge detecting part. By comparing the edge intensity with a threshold inputted from the outside, edge pixels are detected. The result of edge detection is written in the other memory array.

If the current frame is the second or later frame (reference frame), the luminance value of edge pixels of the basis frame and the central and four neighbor pixels of the current frame are used for the motion detection. The direction of motion is determined by comparing the frame difference values. If the motion isn't detected on the frame, the sensor continues with this processing in the next frame.

In this sensor, the number of the pixels for each direction can be obtained by using the counter circuit and calculated for not only whole image but also arbitrary area controlled from the outside. The sensor outputs not only the results of detected motion direction for each pixel but also the number of pixels for each direction.

6. Conclusion

In this paper, we propose 2D motion detection image sensor. In this sensor, moving direction is detected by using the frame difference with shifting the referential pixels under a high speed imaging. Moving speed is also detected by changing a frame rate or a processing interval of the motion detection. Additionally, we explain the method of the moving direction in depth axis by using a change of the object's size.

The image sensor is now under evaluation.

Table 1 Outline of the prototype chip.

process	2poly, 4metal, CMOS 0.35 μm
power[V]	3.3
chip size[mm^2]	1.98×4.48
pixel number[pixels]	64×64
pixel size[μm^2]	16×16
fill factor[%]	52.8
Num. of trans. (transducer)[Tr./pixel]	3
Num. of trans. (digital memory) [Tr./pixel, 2bit]	8
Num. of trans. (analog memory) [Tr./pixel]	4

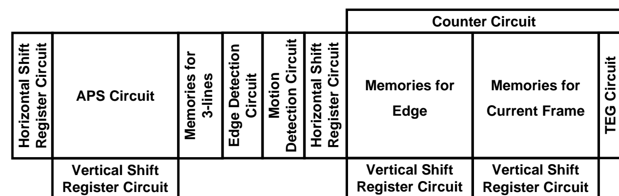


Fig.8 Layout of the prototype chip.

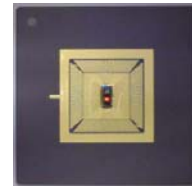


Fig.9 Photograph of the prototype chip.

References

[1] Jie-Bin Xu, Lai-Man Po and Chok-Kwan Cheung, "Adaptive Motion Tracking Block Matching Algorithms for Video Coding", IEEE Transactions on Circuits and Systems for Video Technology, Vol. 9, No. 7, pp. 1025-1029, Oct. 1999.

[2] Yi Sun, "Tracking and detection of moving point targets in noise image sequences by local maximum likelihood", International Conference on Image Processing, Vol. 3, pp. 799-802, Sep. 1996.

[3] J.P. Berns and T.G. Noll, "A Flexible Processor for Object Based HDTV Motion Estimation", IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 1209-1212, Jun 1997.

[4] F.J. Ferri, J. Malo, J. Albert and J. Soret, "Variable-size Block Matching Algorithm for Motion Estimation using a Perceptual-based Splitting Criterion", Fourteenth International Conference on Pattern Recognition, Vol. 1, pp. 286-288, Aug. 1998

Towards smarter ranging pixels with high dynamic range : sensitivity-tuning of current assisted photonic demodulators

Ward van der Tempel, Daniel Van Nieuwenhove, Riemer Grootjans and Maarten Kuijk
Lab for Micro- and Photonelectronics (LAMI)
Department of Electronics and Informatics (ETRO)
Vrije Universiteit Brussel
Pleinlaan 2, 1050 Brussel, Belgium
Email: wvdtemp@etro.vub.ac.be

***Abstract*— The peculiarities of Time-of-Flight ranging with CMOS sensors - with respect to conventional CMOS imaging - allow new ways to enhance dynamic range of these CMOS ranging sensors. This paper discusses how a current-assisted photonic demodulator can be modified to provide enhanced dynamic range. An extra node provides tunable sensitivity to the detector without interfering with the photonic demodulation properties of the device. It can be used to construct smart ranging pixels with extended dynamic range.**

I. Introduction

In CMOS imagers dynamic range is a critical figure of merit. A scene composed of both bright and dark regions is often difficult to capture due to limited dynamic range. A lot of research has already been conducted to improve the dynamic range of today's passive CMOS imagers: sensors with a limited variability of detector capacitance have been proposed [1], multi-sampling imagers taking different frames at distinct exposure times combining them into one image [2], Digital Pixel Sensors [3], combined linear-logarithmic response [4]. While these techniques can also be applied to active CMOS Time-of-Flight (TOF) ranging sensors, due the nature of the measurements obtained in TOF systems, new approaches can be explored, tailored specifically for these TOF sensors.

A typical Modulated Wave Time-of-Flight (MTOF) ranging system is depicted in figure 1. Modulated light is sent to a scene, the reflections are captured by a photonic demodulating sensor which correlates the captured signal with reference signals. These correlations can then be used to extract phase-shift and hence distance information. Since reflection intensities fall with the squared distance, scenes with high dynamic range are inherent to active systems. To be able to measure both close-by and far-away objects the dynamic range of these imaging systems should be very large. Initial solutions, such as multi-sampling, can of course be borrowed from the passive CMOS imager techniques. However, the active MTOF system based on photonic demodulators is actually very different from a passive imager. Sensors in passive imagers measure absolute illumination levels to construct the contrast of the image.

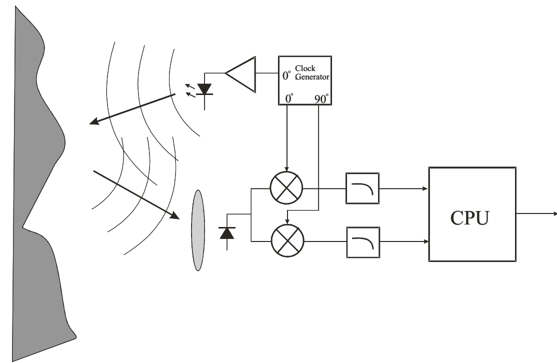


Fig. 1. A typical Modulated Wave Time-of-Flight (MTOF) ranging system.

This means that integration time and conversion gain must be known in order to relate the measurements of the pixels to one-another. MTOF ranging systems measure phase information instead. This implies that each pixel in such a system can be optimized independently, as long as the phase-information is retained. In this paper we will discuss how the current assisted photonic demodulator [5] can be modified to show tunable behavior, making per-pixel optimization possible.

II. the Current-Assisted Photonic Demodulator

The current assisted photonic demodulator (CAPD) was first proposed in [5]. It is a CMOS device based on configurable electric fields. Figure 2 shows the cross-section of a current-assisted photonic demodulator. A majority current is sustained in the substrate by a potential ΔV applied between substrate contacts $Mix2$ and $Mix1$. The electric field determines to which detection junction the electrons, created by captured light, are transferred. With $V_{mix1} > V_{mix2}$ (ΔV>0), the electrons will be transferred to the detecting junction Det1. Likewise, ΔV<0 will send the electrons towards junction Det2. By alternating ΔV we have constructed a photonic demodulator.

This CAPD detector can be integrated in an Active Pixel architecture [6]. Using a 3T architecture a reset, an output

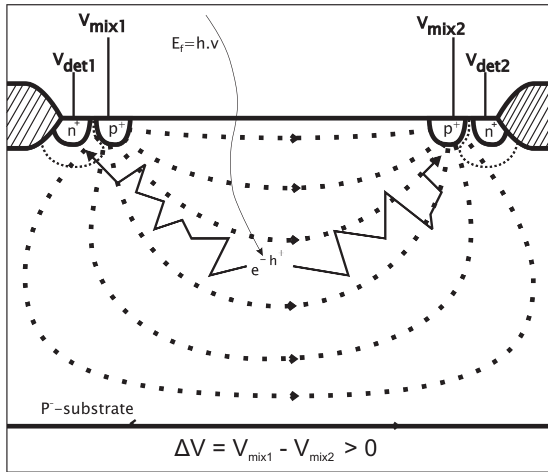


Fig. 2. Cross-section of a CAPD detector. A potential ΔV>0 = $V_{mix1} - > V_{mix2}$is applied, creating an electric field in the substrate. The electrons are transferred by drift to the selected detection junction. For ΔV>0 the electrons will be detected at Det1, ΔV<0 at Det 2.

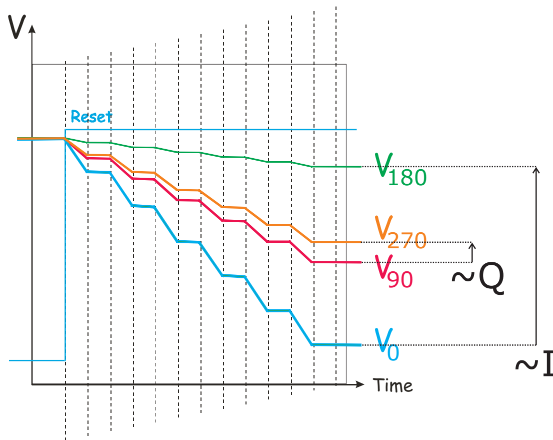


Fig. 3. Cycles.

and a select transistor are added for each detection node. The device is operated much like a conventional active pixel sensor (APS). The detection node is reset and integration is started. Note that here the detector is not a simple n-well, but must be operated by applying the right signals to the Mix substrate contacts. Hence, the charge collected after integration at the detection junction Det1 represents a correlation of the received photonic signal and the signal applied to $Mix1$. To obtain the phase-shift information of the photonic signal, multiple correlations must be performed and compared. As described in [6] several correlations are needed to remove back-ground illumination, reflection intensity and other imperfections from the equations. These values can be obtained time-sequentially (in the case of 1-tap and 2-tap CAPD's) or simultaneously (4-tap CAPD). Typically the received optical signal is correlated with the original modulation signal, its inverse, its quadrature and its inverse quadrature signal, yielding V_0, V_{180}, V_{90} and V_{270} respectively, as shown in figure 3. For sine-wave modulated TOF the phase is calculated using the equation 1 with $I = V_{180} - V_0$ and $I = V_{270} - V_{90}$.

$$\phi_{sine} = \arctan \frac{Q}{I} \tag{1}$$

It is clear that the *difference* between correlations holds the wanted phase information - in other words the photonic demodulator measures *relative* instead of absolute levels to obtain phase-shift and hence depth information. This fundamental difference implies that every pixel can autonomously optimize its sensitivity, conversion gain or integration time. The setting of each pixel does not need to be known to calculate the phase-information from the measured correlations, as long as these correlations are obtained with the same setting.

III. Dynamic Range in MTOF CMOS Ranging Sensors

A reason why increased dynamic range in TOF systems is highly desirable was mentioned in the introduction. Active imaging is inherently confronted with big differences in reflection intensities. If the CAPD pixel saturates when measuring the correlations, the calculated phase will be distorted and lost. However, a very short integration time to prevent saturation of these pixels yields bad SNR for correlations obtained in pixels focused on far-away regions. Saturation can be caused by the active signal itself, for example when the pixel is focused on a close-by object, or by background light illumination. Saturation caused by background light is worse because it does not contribute to the relative information and introduces extra noise. The background light illumination in MTOF has the same effect as the dark current in conventional imaging: decreased of the dynamic range. Figure 4 shows a plot of the different situations in active TOF imaging. The vertical axis represents the active reflected signal while on the horizontal axis the sum of the background light signal and the dark current is plotted. Our hypothetical sensor has a saturation level of about 30000 electrons, which is shown by the saturation boundary, and a total sensor noise (reset and readout noise) of about 40 electrons. A region can be identified where the measurements are limited by the active signal shot noise. Below this curve the limit is due to the total sensor noise and the shot noise of the dark and background current. At low background light levels (neglecting the dark current) the sensor has a large dynamic range DR1. With increasing background light levels the dynamic range drops steeply as less signal swing is available for the active signal and the shot noise of the background light increases (dynamic range DR2). A possible situation is depicted in figure 5 with the dashed lines representing a saturated signal. The integration time is too long and all relative information between the two dashed lines is lost at the end of the integration. A straightforward solution is to control the sensitivity of the pixels capturing high intensities on a per-pixel basis. A first possibility, depicted by the solid lines, is to let the pixel autonomously decide when to stop integrating by abruptly cutting the sensitivity of the detector when saturation is near. In this way, the relative information is held until the end of the global integration time.

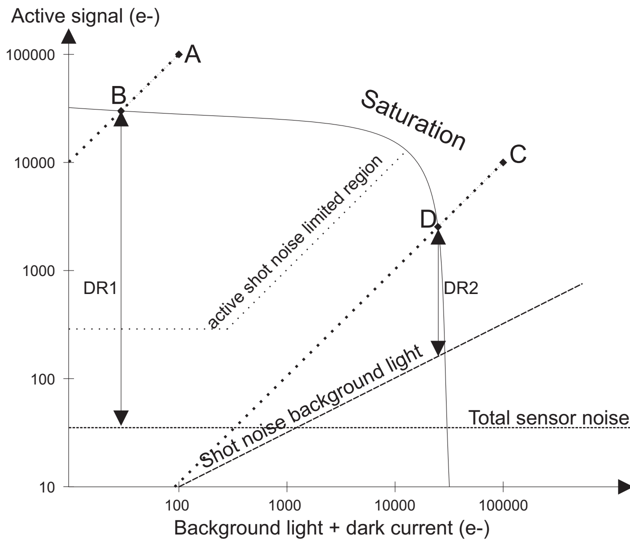


Fig. 4. Different situations in active imaging given a fixed integration time. The total sensor noise includes the reset and read-out noise. For convenience the dark current and background light current are considered one. The information in A and C is lost after saturation. Smart pixels can clip them to B and D respectively and hold the information.

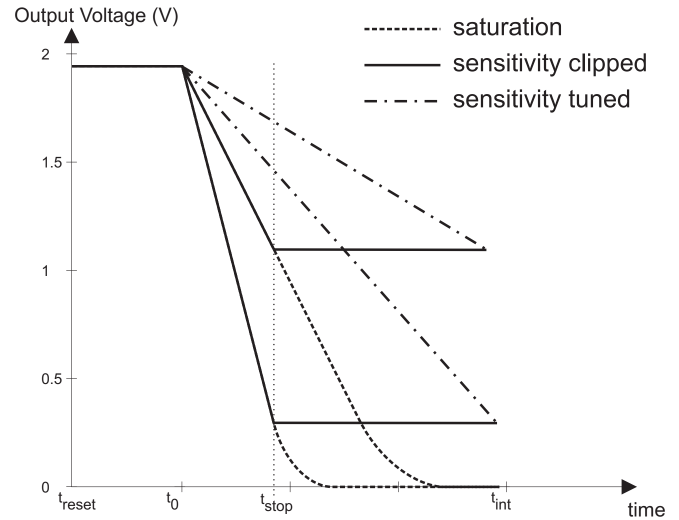


Fig. 5. The dashed lines represent the saturated signals without smart integration. A CAPD sensor with sensitivity tuning operated as an in-pixel electronic shutter can hold the information until read-out (solid lines). Continuous control of the sensitivity can create the signals depicted with the dash-dotted lines.

An array of these pixels can be operated synchronously at a low frame-rate needed for low-intensity reflections of far-away objects, without saturation of the pixels corresponding to near-by objects, extending the dynamic range of the sensor. Applying this method to figure 4, the signals corresponding to point A can be clipped to B, the signals in point C clipped to D. Note that the dynamic range at the output has not increased, but due to the non-linear behavior (clipping) a bigger range of illumination levels can be processed without saturation and without loss of relative information. A similar result can be obtained by reducing the sensitivity during the integration. Instead of clipping the integration time, the sensitivity is tuned. While these approaches require different control circuits, the results are similar. Both approaches rely on controlling the sensitivity in-pixel in a digital or analogue way.

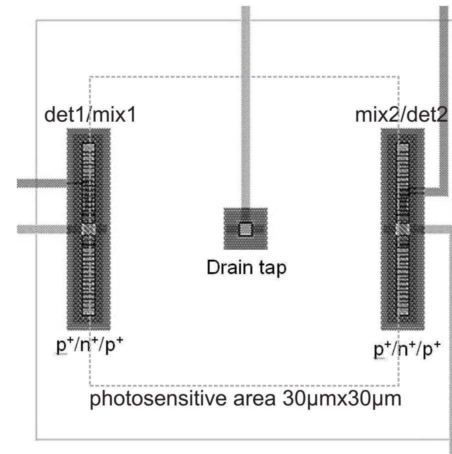


Fig. 6. Top view of a prototype CAPD detector with drain tap for sensitivity tuning. A potential V_{drain} is applied to the drain tap sensitivity tuning contact. If V_{drain} rises, a fraction of the photogenerated electrons is drawn to the drain contact, tuning the overall sensitivity of det1 and det2.

IV. A TUNABLE CURRENT-ASSISTED PHOTONIC DEMODULATOR

To implement tunable sensitivity of the current assisted photonic demodulator an extra drain region was added in the photosensitive area [7], as shown in Figure 6. This region consists of a substrate contact and a detection junction, connected both at the same potential V_{drain}. When a positive potential V_{drain} is applied to this node, a fraction of the photo-generated electrons available in the substrate is attracted to the drain tap and collected using the detection junction. This influences the amount of electrons involved in the demodulation, reducing the overall sensitivity of the detector, while the photonic demodulation continues unhindered.

V. MEASUREMENTS

Figure 7 shows a measurement of the sensitivity of the device when different drain tap voltages are applied. The voltage over the channel was incremented from 0.4V - Mix contacts switched between -0.2V and 0.2V - to 2V - Mix contacts switched between -1V and 1V. Since the Mix potentials are balanced around 0V and the drain tap is located in the center of the device, applying V_{drain} = 0V does not change anything to the performance of the device and relative sensitivity is 100%. Increasing the voltage of the drain tap decreases the overall sensitivity as shown in figure 7. With low channel voltage increasing the drain tap voltage creates a steep drop of the sensitivity. This can be used as an electronic shutter, enabling the first option to enhance dynamic range mentioned in §3. As

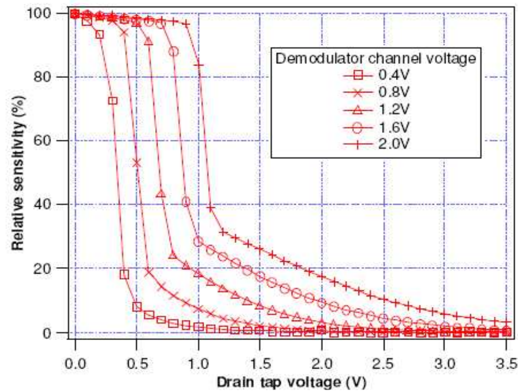


Fig. 7. Measurement of relative sensitivity versus drain voltage at different demodulator channel voltage ΔV.

the demodulator channel voltage is increased, the drain voltage necessary for the initial sensitivity drop increases. Also, the drain tap gradually loses the power to fully quench the sensitivity, showing a more gradual control of the sensitivity. This allows the continuous in-pixel sensitivity tuning. Work on ranging pixels based on the CAPD with tunable sensitivity is on-going.

VI. Conclusion

We presented a current-assisted photonic demodulator with tunable sensitivity. We discussed how this device can be used to construct smart MTOF ranging pixels. While the dynamic range at the output remains unchanged, the non-linear behavior allows an increased dynamic range of the input light intensities.

References

[1] S. Decker et al., "A 256x256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output", ISSCC Digest of Technical Papers, Feb. 1998, pp. 176–177.

[2] M. Sasaki et al, "A Wide-Dynamic-Range CMOS Image Sensor Based on Multiple Short Exposure-Time Readout With Multiple-Resolution Column-Parallel ADC", IEEE Sensors Journal, vol. 7, no. 1, Jan 2007, pp. 151

[3] A. Kitchen et al., "A Digital Pixel Sensor Array With Programmable Dynamic Range", IEEE Transactions on Electron Devices, vol. 52, no. 12, Dec 2005, pp. 2591

[4] G. Storm et al, "Extended Dynamic Range From a Combined Linear-Logarithmic CMOS Image Sensor", IEEE Journal of Solid-State Circuits, vol. 41, no. 9, Sep. 2006, pp. 2095

[5] D. Van Nieuwenhove et al., "A Novel Standard CMOS Detector using Majority Current for guiding Photo-Generated Electrons towards Detecting Junctions", Proceedings Symposium IEEE/LEOS Benelux Chapter, 2005, pp. 229–232.

[6] W. van der Tempel et al., "Lock-in Pixel Using a Current-Assisted Photonic Demodulator Implemented in 0.6 μm Standard Complementary Metal-Oxide-Semiconductor", Japanese Journal of Applied Physics, Vol. 46, No. 4B, 2007, pp. 2377–2380.

[7] D. Van Nieuwenhove et al. "Photonic demodulator with sensitivity control", IEEE Sensors Journal, vol. 7, no. 3, pp. 317–318, Mar. 2007.

<u>Trends in CMOS Imager Technology for Low Power and Low Cost Applications</u>

Don Scansen and Jochonia Nxumalo
Semiconductor Insights Inc.
3000 Solandt Road, Kanata, Ontario Canada K2K 2X2
dons@semiconductor.com

Image sensor design faces an ever-increasing challenge due to the scaling down of the pixel area in an effort to reduce chip production costs while increasing device spatial resolution. Although many circuit design techniques have been developed and many more will be required as the pixels are scaled down, the fundamental limits of performance are related to the design and structure of the unit pixel itself.

New and improved methods of packing photodiodes closer together while maintaining sensitivity and without increasing noise are beginning to emerge as the industry moves to active pixel sensor sizes below 2µm [1]. One of the most important aspects of pixel scaling is engineering of the photodiode and related active areas in the silicon substrate. Other groups have studied photodiode design through careful simulation work [2], [3]. Through our consulting work benchmarking CMOS image sensors, we have found that Scanning Capacitance Microscopy (SCM) is an absolutely indispensable tool for providing a complete understanding of production samples.

Traditional SEM imaging techniques provide the best overall view of the various materials and processes used in modern CIS fabrication. This can be seen in a topographical view of one manufacturer's APS design and cross-section in Figure 1. However, SEM cannot extract details of the photodiode and other aspects of substrate design. The SCM views of one manufacturer's recent (2.7µm pixel generation) APS design and structure are shown in Figures 2 through 4.

Other scanned probe techniques are also very valuable in the study of CIS fabrication. Atomic Force Microscopy (AFM) can be used to evaluate the important back end processes of color filter and microlens arrays. SEM imaging may not provide sufficient detail about the final structure. There are several recent articles describing techniques for denser packing of the microlens such as dead zone free [4] or zero gap [5]. Figures 5 through 8 show examples of AFM providing insight into lens and filter height, shape and uniformity.

As APS dimensions shrink, signal-to-noise ratio is reduced. In our work, we have begun to see production devices that employ structures to avoid structures that contribute to the total device noise. One of these is shallow trench isolation (STI). There has been a migration toward more junction isolation (Figure 3) and field oxide above the substrate rather than in the usual STI approach. We predict that there will be increased emphasis on keeping the substrate design interface free whenever possible.

In conclusion, we have used AFM and SCM to examine the current state-of-the-art in commercial CMOS image sensors from the leading manufacturers. These analytical techniques reveal a great deal about the final photodiode and associated substrate design. We believe that our benchmarking and predictive trends studies suggest the use of AFM and SCM more extensively in the development of the next generation of CMOS image sensors.

[1] K. Itonaga, H. Abe, I. Yoshihara, and T. Hirayama, "A High-Performance and Low-Noise CMOS Image Sensor with an Expanding Photodiode under the Isolation Oxide," 33.1, Technical Digest of the 2005 IEEE International Electron Devices Meeting
[2] Igor Shcherback, Tatiana Danov, and Orly Yadid-Pecht, "A Comprehensive CMOS APS CTK Study: Photoresponse Model, Technology, And Design Trends," IEEE Transactions on Electron Devices, Vol. 51, No. 12, December 2004
[3] Igor Shcherback, Tatiana Danov, and Orly Yadid-Pecht, Study of CMOS APS Responsivity Enhancement: Ring-Shaped Photodiode, IEEE Transactions On Electron Devices, Vol. 52, No. 1, January 2005
[4] Young Chan Kim et al, "1/inch 7.2 mega-pixel CMOS Image Sensor with 2.25um Pixel Using 4-shared Pixel Structure for Pixel-level Charge Summation," Proceedings of the 2006 IEEE International Solid-State Circuits Conference
[5] M. Cohen et al, "Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensors," 5.4, Technical Digest of the 2006 IEEE International Electron Devices Meeting

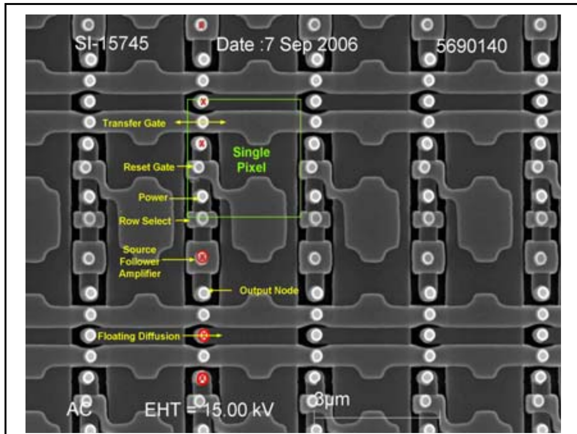


Figure 1: SEM micrograph of APS design at polysilicon level (manufacturer A, 2.7µm APS)

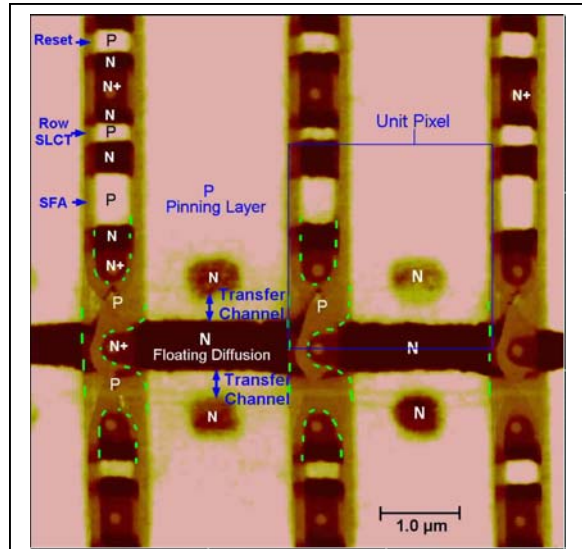


Figure 2: SCM 2D map of APS design at diffusion level (manufacturer A)

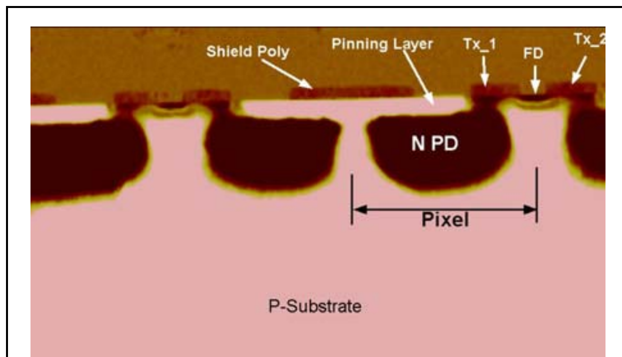


Figure 3: 2D cross-section SCM map of photodiode structure (manufacturer A)

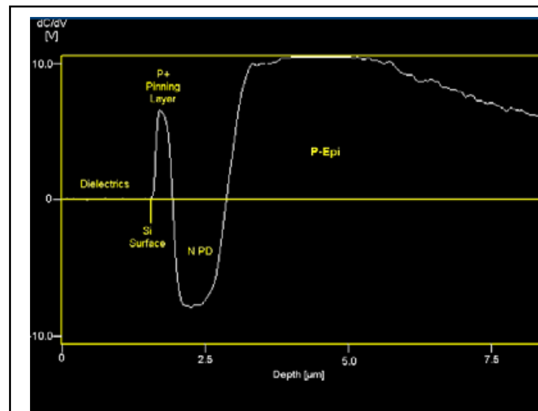


Figure 4: 1D SCM linescan of junction depths in photodiode region (manufacturer A)

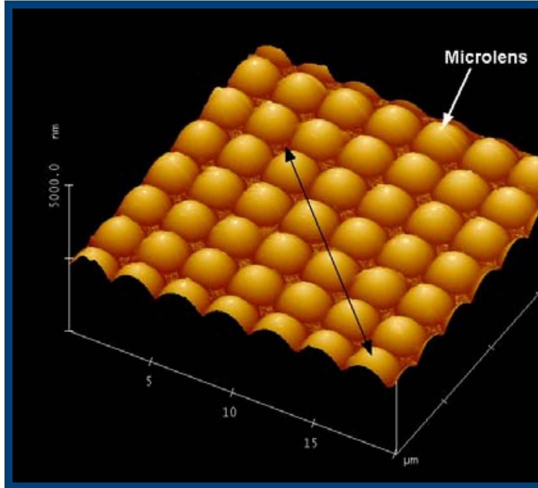


Figure 5: AFM image of microlenses (angle view) (manufacturer B)

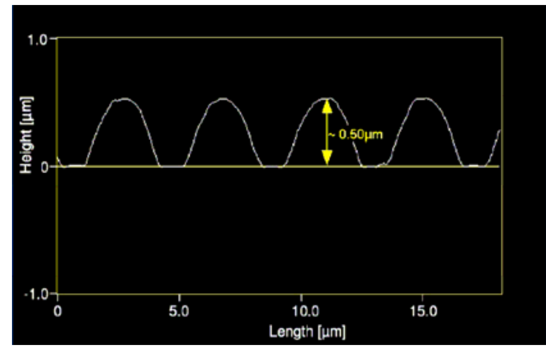


Figure 6: AFM line profile of microlenses (manufacturer B)

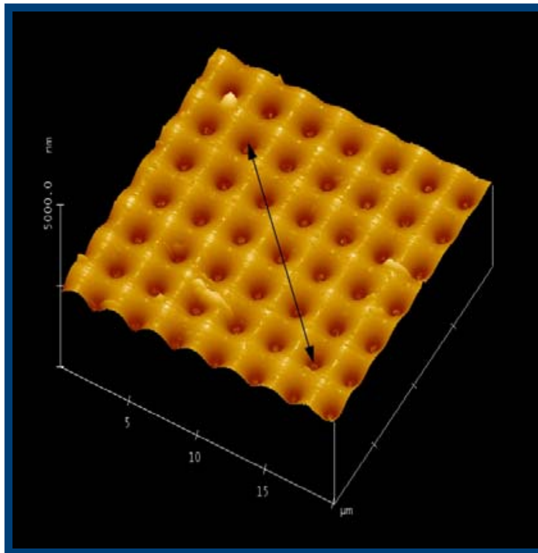


Figure 7: AFM image of blue filter covering periphery (angle view) (manufacturer B)

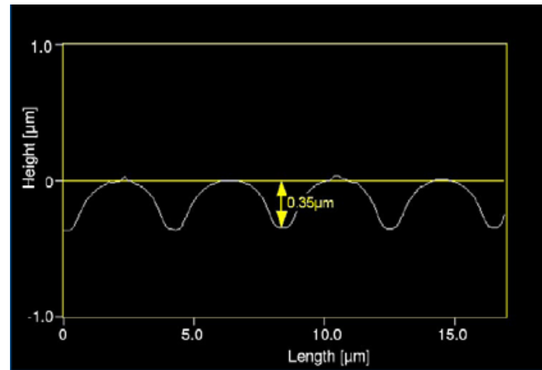


Figure 8: AFM line profile of blue filter covering control circuits (manufacturer B)

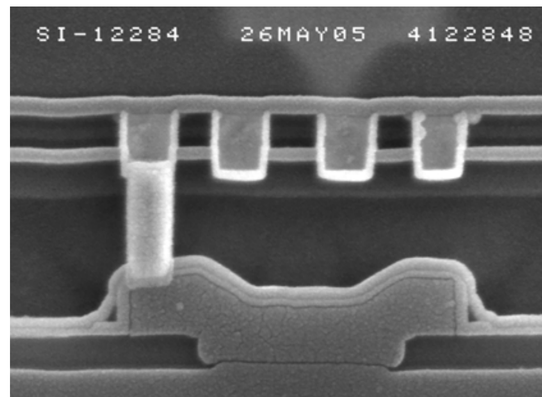


Figure 9: Deposited field oxide isolation (manufacturer C, 2.5µm APS)

Applied Mathematics to Simplify Imager and Camera Analyses

Peter Centen, R&D Cameras, Grass Valley,
Kapittelweg 10, 4800RP, Breda, The Netherlands, tel: +31 76 5721564;
Peter.centen@thomson.net

Abstract. *Discussed in this paper are 3, extremely helpful, techniques in the analyses of imager and camera performance. The first topic is an extension to the well known photon shot noise curve. It is a straight forward method to determine any arbitrary transfer function f(N) from pixel-to-camera output. Next, the design of a μ-lens is usually executed as a function of Chief Ray Angle (CRA). But performance is practically measured with a lens and a given f-number range. The method offered converts the f-numbers into a set of CRA numbers with which the μ-lens efficiency η(CRA) can be determined as a function of CRA. The third topic entails the application of a 2-dimensional histogram to investigate dependence of all pixels in an imager on one parameter. Like temperature, supply voltage or time.*

1.0 An extension to the photon shot noise transfer curve

The noise at the output of a camera consists of two basic parts. One is the system noise often referred to as the read noise and the other is the shot noise. The shot noise is governed by the laws of physics and as such predictable. The system noise can be rather complex depending on whether anomalies in the system occur. Examples of anomalies are: LVDS transmission failures, missing bits in the ADC, periodic ADC noise due to ground bounce. The method and its practical implementation discussed in this paper is applicable in the situation with and without anomalies.

In the linear approach for the shot noise transfer curve the output signal reads

(1.1) $V_{out} = K * N$,

with K the gain from pixel-to-output and N the number of electrons generated in the pixel. The noise is written as the quadratic sum of the shot noise and the read noise,

(1.2) $U_n = K * \sqrt{N + N_d^{\,2}}$.

For large charge packets (N) the ratio between the noise squared and the output signal approaches K. Measuring the noise U_n as a function of the output signal V_{out} allows to calculate the unknown gain K, [1,2]. Knowing K one can convert the output signals in the number of electrons without a priory knowledge of the μV/e and the gain of the camera chain. For instance one can determine the read noise in electrons, the maximum charge handling capacity and other pixel related parameters like FPN and sensitivity all in electrons.

Graphing the noise on the Y-axis and the output signal on the X-axis on a log-log scale shows two asymptotic lines. One for small N values with the noise approaching the read noise N_d and for large N values approaching $\sqrt{N}$ which on a log log scale shows as a straight-line with coefficient ½.

In the general case the output signal V_{out} is written as:

(1.3) $V_{out} = f(N)$

and the corresponding noise, or root of variance, U_n

(1.4) $U_n = \left|\dfrac{df(N)}{dN}\right| * \sqrt{N + N_d^{\,2}}$

With f() the transfer function from pixel-(electrons) to-camera-output, N the number of electrons generated in the pixel and N_d the read noise. Under the reasonable assumption of monoticity for f() the absolute-signs can be dropped.

Taking the derivative from the output signal, equation (1.3), with respect to the number of electrons N, substituting the result in the noise equation (1.4), applying separation of variables and finally integrating left and right sides, the result reads

(1.5) $$\boxed{\int_0^N \frac{dN}{\sqrt{N + N_d^{\,2}}} = \int_0^{Vout} \frac{dV_{out}}{U_n}}$$

The left side can be written in closed form and the right side is known through measurement,

(1.6) $$\sqrt{N + N_d^{\,2}} - N_d = \frac{1}{2} * \int_0^{Vout} \frac{dV_{out}}{U_n}$$

Hence the arbitrary transfer function f(), from pixel-to-output, can be determined and the output signal V_{out} as a function of the number of electrons (N) generated is known and can be graphed,

(1.7) $$\boxed{N = \left(\frac{1}{2} * \int_0^{Vout} \frac{dV_{out}}{U_n} + N_d\right)^2 - N_d^{\,2}}$$

Nowadays width the advent of digitized images the method is fairly simple to implement. Use is made of the fact that output levels are represented as digital words with a given bit depth. Hence can be used as in index of a one dimensional array too.

The implementation requires 3 grabbed images, Figure 1.1, as follows:

-take **shortly** after each other two snapshots, **ImageG1** and **ImageG2**, of any scene containing all the gray levels from black to white, eg a defocused grey chart. The difference between these two images on a pixel-by-pixel basis is only shot noise and read noise times $\sqrt{2}$.

-take shortly here after a snapshot of the black, **ImageB**, eg with capped lens. The difference between ImageG1 and ImageB is the output level on a pixel-by-pixel basis. The graph of the noise versus output level, is then calculated following:

For i,j = 1,1 to Nrows, Ncolumns do
Vout= ImageG1[i,j]-ImageB[i,j]);
Histo(Vout)= Histo(Vout)+1;
Variance(Vout) = Variance(Vout) +
+{(ImageG2[i,j]-ImageG1[i,j])²/2-Variance(Vout)}
/Histo(Vout);
End

NOTE: The Variance is written as a moving average in recursive form!

For all output levels, V_{out}, now calculate the noise

(1.8) $U_n(V_{out}) = \sqrt{Variance(V_{out})}$

and so the right-hand side of equation (1.6) is known.

Figure 1.2 shows the noise as a function of output level for a camera with gamma switched on (power law) and a camera in linear mode.

The discretized form of equation (1.7) reads:

(1.9)

$$N_k = \left(\frac{1}{2} \sum_{i=1}^{i=k} \frac{Vout(i) - Vout(i-1)}{U_n(i)} + N_d \right)^2 - N_d^{\ 2}$$

Application of eq. (1.9) to the data depicted in Figure 1.2 results in the second graph, Figure 1.3, where the transfer-function of the pixel-to-camera output is calculated. Clearly the linear and the gamma transfer characteristics are visible.

2.0 Conversion from f-number to chief ray angle

A nice theoretical approach to the optical efficiency is given in [3]. In this chapter a practical approach is described for the class of lenses with object at infinity.

Given a camera, an imager and a lens with aperture f. Than a cone of light with Chief Ray Angles ranging from 0 to CRA_x is projected on the pixels , Figure 2.1, with the following relation between maximum CRA_x and f-number

(2.1) $$CRA_x = ATAN\left(\frac{1}{2*F}\right)$$

In general the output level V_{out} is proportional with the inverse of the f-number squared, F^{-2}

After applying geometry one arrives at the following relation between output level and CRA_x

(2.2) $$V_{out} = g * \int_0^{CRA_x} \eta(\theta) * \frac{\tan(\theta)}{\cos(\theta)^2} d\theta$$

Where the μ-lens efficiency, as a function of CRA, is defined as $\eta(CRA)$ and g a constant is.

In the case of a perfect μ-lens, $\eta(CRA) = 1$ and after performing the integration of equation (2.2) the output level is proportional with $\tan(CRA_x)^2$ or after substitution of equation (2.1) with the inverse of the f-number squared as one would expect.

Table 1, shows the CRA values for several f-numbers

F	CRA
1.2	22.62
1.4	19.65
2	14.04
2.8	10.12
4	7.13
5.6	5.10
8	3.58
11	2.60
16	1.79

Table 1: CRA expressed in degree

Using the mean-value theorem of integration, defining $\overline{CRA}$ as an element of the interval $[CRA_1, CRA_2]$ eq. (2.2) is than evaluated as

(2.3)

$$V_{out}(CRA_2) - V_{out}(CRA_1) =$$

$$\eta(\overline{CRA}) * g * \int_{CRA_1}^{CRA_{2x}} \frac{\tan(\theta)}{\cos(\theta)^2} d\theta =$$

$$\eta(\overline{CRA}) * \frac{g}{2} * \left(\frac{1}{\cos(CRA_2)^2} - \frac{1}{\cos(CRA_1)^2} \right)$$

Therefore given two f-numbers for which the output level V_{out} is measured, the related CRA can

be calculated and an estimation of the μ-lens efficiency on the interval [CRA_1,CRA_2] is determined through equation (2.3)

A more refined approach is by defining the μ-lens efficiency as a smooth function:

$$(2.4) \quad \eta(CRA) = \frac{1}{1 + b * CRA^3} + a * CRA^2 .$$

Substituting into eq. (2.2) and applying a least-mean-square-fit to the measured V_{out}, as a function of CRA_x, the parameters a and b are determined. Hence the *μ-lens* efficiency is known as a function of CRA by substituting a and b back into eq. (2.4).
This theory now is applied to experimental results [4] which are graphed for a straight forward μ-lens and a double μ-lens. The μ-lens efficiency as a function of CRA is depicted in figure 2.2. The effect of the embedded lens now clearly shows for CRA larger than 12 degree.
The error between the measured and the estimated V_{out} is within 1% for the new μ-lens and 2% for the old μ-lens.

3.0 On the use of a 2-dimensional-histogram.

The application of a 2-dimensional histogram is in determining activation energies of large population of pixels. Or the dependence on a parameter like pixel supply voltage or change in pixels as a function of time. Its purpose is that after application of the method one can see at a glance if a large amount of pixels, on an individual basis, behave the same or if the relation to the parameter under investigation is uncorrelated.

The 2-dimensional histogram is an image, 3D-plot, where X and Y-axis are amplitude values and the Z value is the histogram (count) part.
Use is made of the fact that the pixel amplitude in a digitized image can be used as an index of an array.
The 2-dimensional histogram is generated through transformation of the amplitude into X or Y position. The intensity as the number of pixels having that joint X,Y amplitude. One needs 2 grabbed images, and only parameter changed in value. Example: **Image1** and **Image2** are 1920x1080x10bit images and temperature is 70C for the first and 50C for the second image.
A normal histogram can be generated through
For i:=1 to Nrows
For j:=1 to Ncolumns
HISTO2D[IMAGE1[i,j] ; IMAGE2[i,j]]:= HISTO2D[IMAGE1[i,j] ; IMAGE2[i,j]]+1

This normal 2d-histogram shows more or less where and how the point of gravity of all the pixels values changes and is located.
A specialized 2-dimensional histogram is the binarized one [5]:
For i:=1 to Nrows
For j:=1 to Ncolumns
HISTO2DBIN[IMAGE1i,j] ; IMAGE2[i,j]]:=1

When there is a combination of amplitudes that only one pixel exhibits it will show up clearly in the binarized 2-dimensional histogram. As such a very powerful tool to investigate FPN and its excursions, the leaking pixels

Figure 3.1 shows an example of such binarized histogram. Almost all the pixels in the imager have about the same growth factor or activation energy. It looks like a comet tail at an angle to the dotted reference line. There are a few exceptional pixels that go astray. The dotted reference line depicts 'X=Y'. Pixels that do not change in amplitude show up on and close to this line .

Figure 3.2 shows an example of a normal 2-dimensional histogram where the parameter changed is the pixel supply voltage. There are 3 regions to be discriminated:
1: is where pixels have the same amplitude for both pixel supply voltages, (on the dotted line);
2: where the bulk of the pixels change in amplitude with the same growth factor (on an angle different from the dotted reference line)
3: where pixels vanish at low voltage and
4: where pixels vanish at high voltage.

Literature

1] J. Janesick, K. Klaassen, T. Elliott, *Charge-coupled-device charge-collection efficiency and the photon transfer technique*, Optical engineering, October 1987, Vol. 26, No.10, pp 972-980.
[2] J. Mullikin, et. al., *Methods for CCD Camera Characterization*, SPIE 2173, "Image Acquisition and Scientific Imaging Systems", 1994, pp 73-84.
[3] P. Catrysse, B. Wandell, *Optical efficiency of image sensor pixels*, J. Opt. Soc. Am. A, Vol. 19, No. 8, August 2002, pp1610-1620.
[4] H. Takahashi et. al., *A 1/2.7' inch Low-Noise CMOS Image Sensor for Full HD Camcorders* , Visuals Supplement ISSCC 2007, February 2007, pp 745
[5] P. Centen et. al., *A 2/3 inch CMOS Image Sensor for HDTV Applications with Multiple High-DR Modes and Flexible Scanning*, Visuals Supplement ISSCC 2007, February 2007, pp 421.

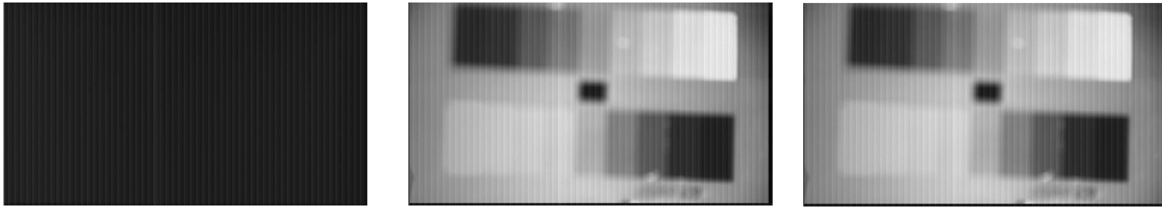


Figure 1.1: Example of a set of 3 images to determine the Shot Noise Transfer Curve

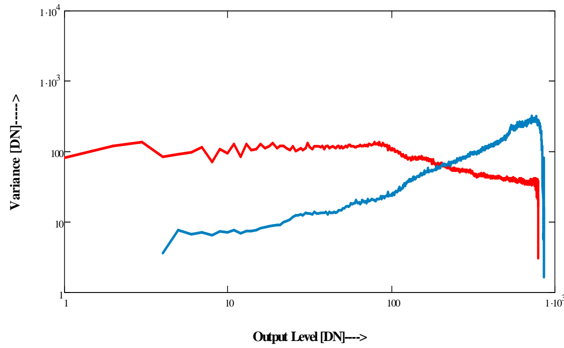


Figure 1.2: Noise (Variance) as a function of output level

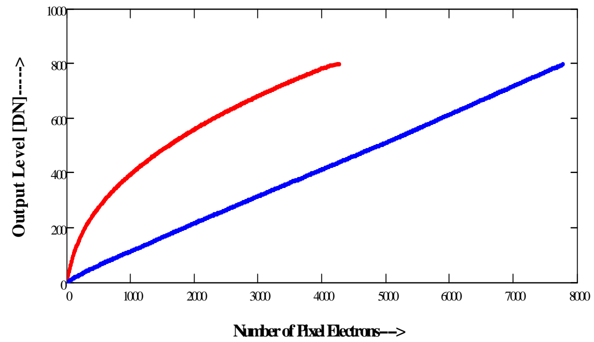


Figure 1.3: Camera Transfer Curve calculated from the shotnoise curves in Figure 1.2.

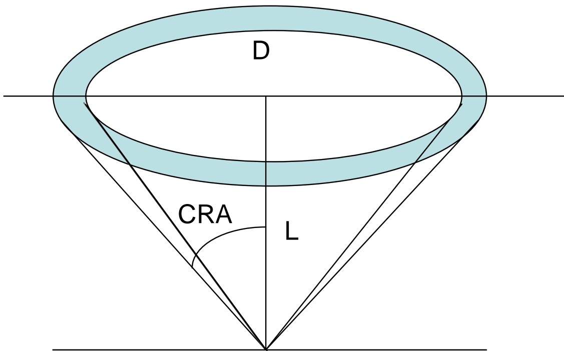


Figure 2.1: F-number and cone angle which is the maximum CRA. All light rays have angles in an interval of [0,CRA].

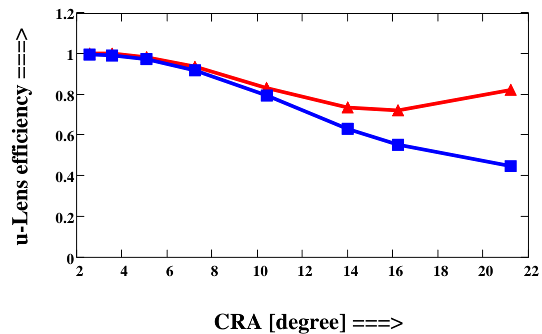


Figure 2.3: Estimated µ-lens efficiency as a function of Chief Ray Angle. Solid squares depict the old µ-lens and solid triangles the new double µ -lens.

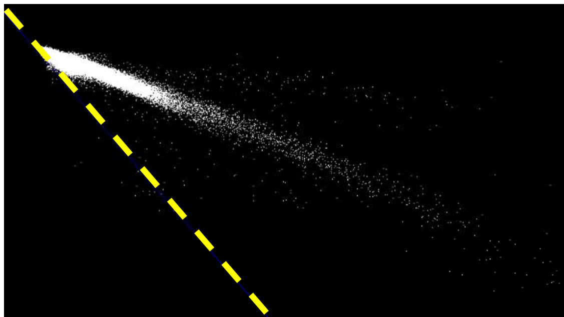


Figure 3.1: Two dimensional binerized histogram for images taken at 70C (X-axis) and 50C (Y-axis). Dotted line for "X=Y"

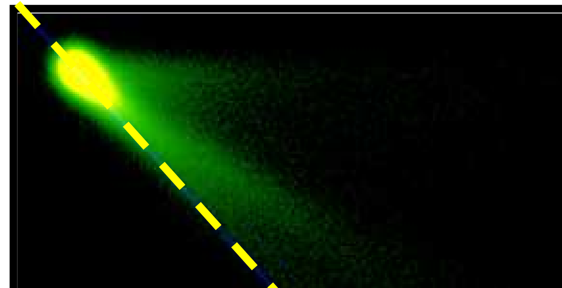


Figure 3.2 A 2-dimensional histogram for an imager with changed pixel voltage. Yellow a linear and green a logarithmic representation. Dotted line for "X=Y".

A custom CMOS imager for wavelength-multiplexed indoor optical LANs

Tomoya Miyawaki, Keiichiro Kagawa, Itsuki Nagahata, Masahiro Nunoshita, and Jun Ohta

Graduate School of Materials Science, Nara Institute of Science and Technology,
8916-5 Takayama, Ikoma, Nara 630-0101 JAPAN

Phone: +81-743-72-6054, Fax: +81-743-72-6052, E-mail: kagawa@ms.naist.jp

ABSTRACT

We are developing a custom CMOS imager to realize a compact and high-data-rate indoor optical wireless LAN module. The CMOS imager has a function of fast optical data acquisition, and we can obtain the positions of the communication nodes from the imager. The function of concurrent multi-point data acquisition of the imager enables us to utilize a wavelength-division-multiplexing (WDM) technique to increase the data rate of the downlink. We have fabricated a 64x64-pixel custom CMOS imager prototype with capability of 4-channel concurrent data acquisition, and constructed a prototype system of WDM indoor optical wireless LAN for proof-of-concept. Image acquisition and the experiments of wavelength-multiplexed free-space optical data transmission by use of the prototype imager are shown.

I. INTRODUCTION

Free-space optical communications (FSOC) including indoor optical wireless local area networks (LANs) [1,2] are an promising technology to realize ultra-fast wireless communications. CMOS imagers can be a candidate of the photoreceiver for the FSOC due to its high functionalities. For example, a custom CMOS imager for the application of communication between unmanned tiny airplanes has been developed[3]. In this paper, we present a custom CMOS imager to realize a compact, high-speed, and intelligent wavelength-division-multiplexing (WDM) indoor optical wireless LAN system. We have already reported custom CMOS imagers for indoor optical wireless LANs [3,4]. We have introduced a WDM function to our imager to increase the total communication bandwidth in proportion to the number of the multiplexed wavelengths. The features of our imager are concurrent data acquisition and crosstalk reduction of the demultiplxed light spots as well as position detection of the communication nodes and the hub from the captured images. Figure 1 depicts our WDM indoor optical wireless LAN system. The functional mode is determined at each pixel among an image capture mode for position detection of the communication counterparts with high photo-sensitivity and a photoreceiver mode for receiving the high-speed optical communication data. The custom CMOS imagers are used at both hub and nodes. The sensor can receive multiple optical data up to four in our prototype imager. With the function, the hub concurrently receives the data from the multiple nodes, and the nodes receive a bundle of the wavelength-multiplexed optical data from the hub at the same time. The wavelength band will be 850 nm. Figure 2 shows a configuration of our system, in which gratings are utilized as a multiplexer and a demultiplexer, and movable MEMS (micro-electro-mechanical systems) mirrors coupled with scan lenses are used for steering the communication light beams.

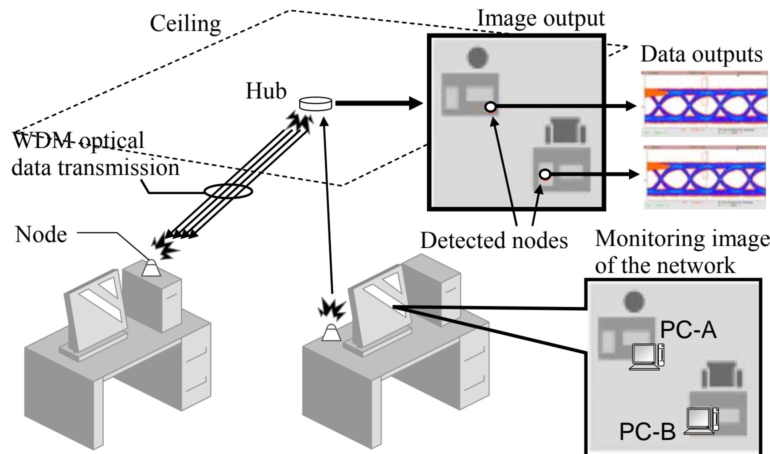


Fig. 1. Wavelength-division-multiplexed indoor optical wireless LAN.

II. SENSOR ARCHITECTURE

Figures 3 and 4 show a block diagram and a pixel schematic of our imager. The features of the pixel structure are simple configuration without in-pixel amplifier, and a function of photo-currents summation of optical communication data among the neighboring pixels to fully utilize the incident optical power. The pixel has vertical signal lines, Vsig<i-1> and Vsig<i>, in its both sides. They are shared among the neighboring columns. In the communication mode, the photocurrent is put out to one of the Vsig lines, which is controlled by the in-pixel latch memories, toward the transimpendace amplifier (TIA) at each column. When both of the in-pixel memories are LOW, the pixel works in the image capture mode, and the photodiode voltage is read through the PMOS source follower to the Vaps<i> signal line. Figure 5 shows a simplified schematic of the photoreceiver circuit of our imager. To alleviate the common-mode noises, the photocurrents from the pixels surrounding the signal pixels are read out through Vref<i> line to realize differential signaling. At most four pairs of Vsig and Vref are selected by the analog multiplexer, and are amplified by the limiter after the cross-talk reduction circuit. The demultiplxed optical signals at the receiver possibly have inter-channel interferences when the pitch of the resolved spots is as large as or smaller than the pixel size or the pitch of the wavelengths is not same as the designed one. The cross-talk reduction circuit is composed of Gilbert-cells to perform a matrix operation, which calculates a product of a matrix with 4x4 elements and four input signals from the analog multiplexer in an analog domain. The matrix elements are applied from outside the imager.

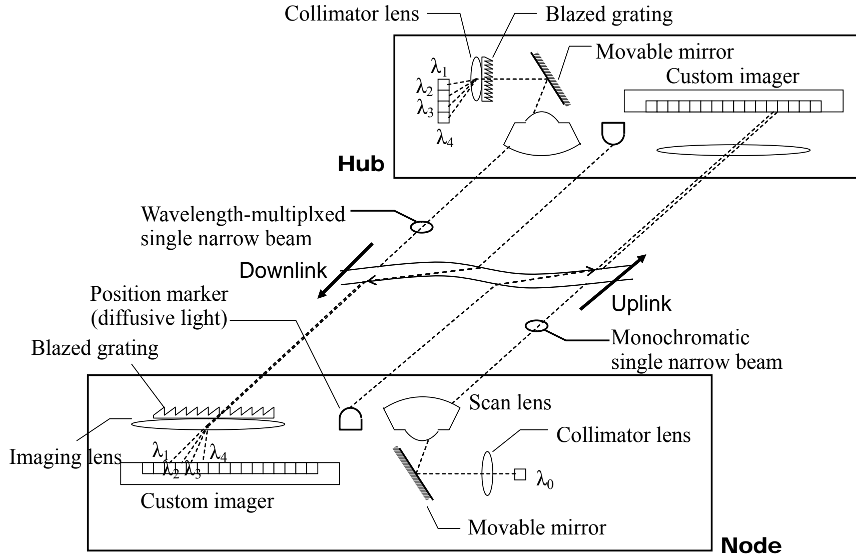


Fig. 2. Configuration of the communication modules.

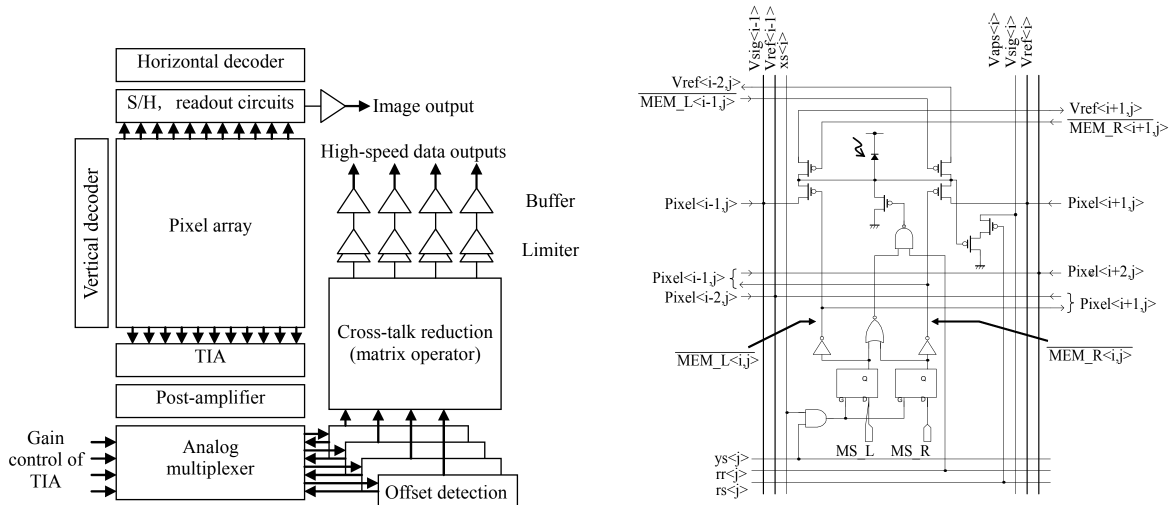


Fig. 3. Block diagram of the imager.

Fig. 4. Pixel schematic.

III. EXPERIMENTAL RESULTS

Figure 6 and Table 1 show the photomircrography and the specifications of our prototype sensor to demonstrate WDM free-space optical data transmission. Figure 7 shows the experimental setup. Three light beams with wavelengths of 676, 785, and 897 nm were multiplexed into a single beam by dichroic mirrors, and deflected by a motorized mirror toward the receiver. After free-space propagation over distance of 1.65 m, the beam is demultiplexed to the multiple spots aligned with 400 μm interval by use of the grating and a visible-infrared video lens at the receiver. Figure 8(a) shows a captured image of a scene of our laboratory to verify the functionality of image acquisition. After the positions of the demultiplexed light spots were detected from the captured images as shown in Fig. 8(b), the output waveforms from our custom CMOS imager were successfully acquired. Fig. 9 shows an eye diagram of a single channel and results of concurrent data acquisition. The waveform for wavelength of 898 nm was not obtained due to low sensitivity of the photodiode for that wavelength. Although the aimed data rate was 100 Mbps for non return to zero signals, the measured data rate was about 20 Mbps. That is why the parasitic capacitances of the bus line in the pixel array and the analog multiplexer were not considered properly in design.

IV. CONCLUSIONS

We have presented a custom CMOS imager for WDM indoor optical wireless LANs, and demonstrated the preliminary WDM optical data transmission and concurrent data acquisition by use of the prototype imager. The data rate will be improved by use of a finer CMOS technology and with proper circuit modeling.

REFERENCES

1. J. R. Barry: *Wireless Infrared Communication* (Kluwer Academic Publishers, 1994).
2. D. C. O'Brien *et al.*: IEEE J. Selected Topics in Quantum Electron. **11** (2005) 173.
3. B. S. Leibowitz, IEEE J. Solid-State Circuits **40**, 9 (2005) 1948.
4. K. Kagawa *et al.*: IEICE Trans. Comm. **E86-B** (2003) 1498.
5. K.Kagawa *et al.*: in Proceedings of 2003 Workshop on CCD&AIS (2003).

Table 1 Specifications of the fabricated imager.

Technology	0.35-μm CMOS (silicide process) 2-poly, 3-metal
Chip size	9.8 mm sq.
Pixel count	64 x 64
Pixel size	100 μm sq.
Photodiode structure	Nwell/ Pdiff
Fill factor without μ-lens	16%
Photoamplifier	RGC (TIA)/ Cherry-Hooper amp. (post amp and gain stage)
Total transimpedance gain	2.5 kΩ – 2.5 MΩ (simulation)
Data rate	20 Mbps NRZ/ ch
Number of channels	4

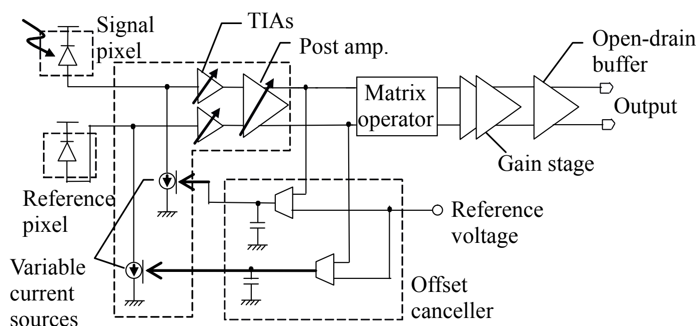


Fig. 5. Simplified schematic of the photoreceiver circuits.

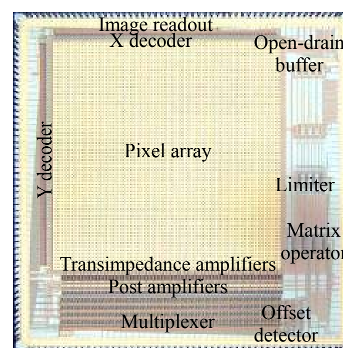


Fig. 6. Photomicrography of the fabricated imager.

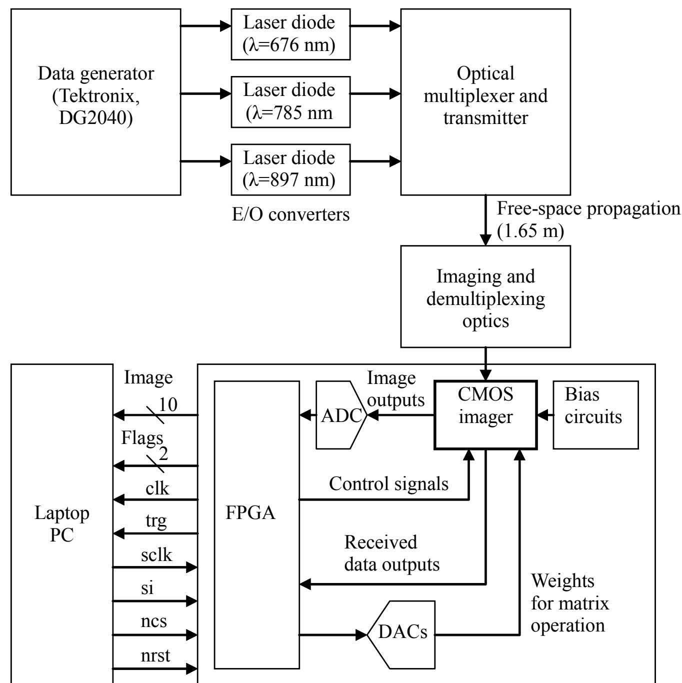


Fig. 7. Block diagram of the demonstration system.

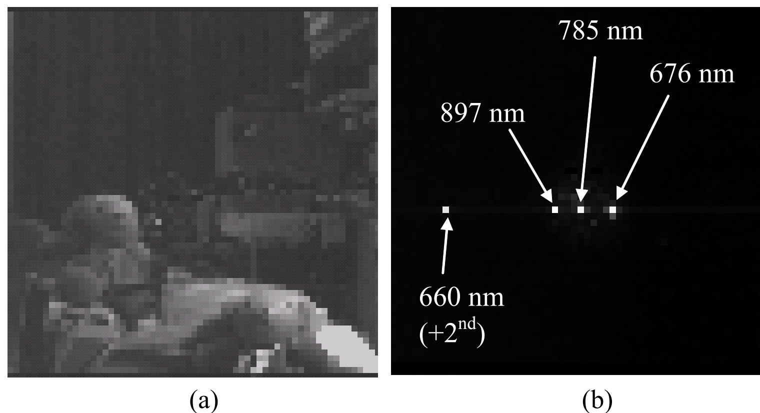


Fig. 8. Captured images of (a) a scene of our laboratory and (b) the demultiplexed light spots.

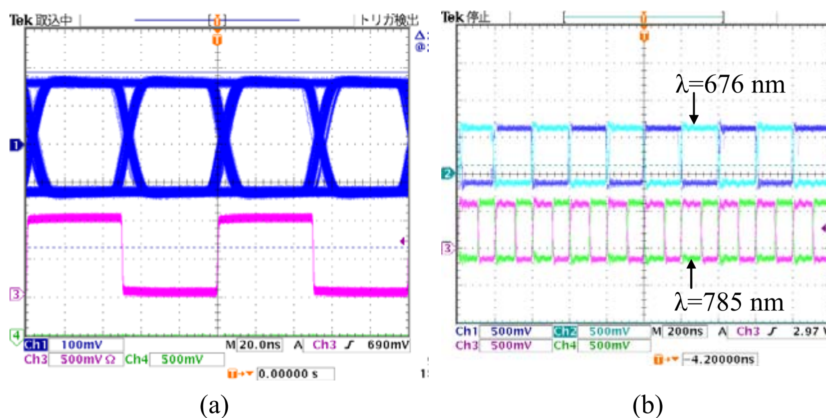


Fig. 9. Received waveforms after limiting: (a) eye pattern of a single channel for 20-Mbps NRZ pseudo-random sequence and (b) concurrent acquisition of two channels

An optical / potential / voltammetric multifunctional CMOS image sensor for on-chip biomolecular / neural analytical applications

T. Tokuda, S. Sato, K. Kagawa, M. Nunoshita, and J. Ohta
Graduate School of Materials Science, Nara Institute of Science and Technology
Takayama 8916-5, Ikoma, Nara, 630-0101 JAPAN.
TEL: +81-743-72-6054, FAX: +81-743-72-6052, E-mail: tokuda@ms.naist.jp

Abstract

We have developed an on-chip image sensor with target applications of on-chip biomolecular and neural imaging. The sensor pixel can sense not only intensity of incident light, but also on-chip electric potential. The light shield structure on the pixel circuit was used as a sensing electrode. Once the passivation layer on the sensing electrode was removed, one can perform on-chip voltammetric measurement, which will be a powerful solution for on-chip biosensing applications. To realise the on-chip voltammetric measurement, we used a column reset line as a current path. Basic characteristics of the sensor was characterized in either optical / potential image sensor operation or optical / voltammetric image sensor operation.

1. Introduction

In the last decade, on-chip bio-sensing and bio-assay technologies using LSI-based intelligent sensors have been attracting a lot of interests and expectations. Measuring bioscientific targets (DNAs, proteins, neural cells, etc.) with on-chip configurations, there are three major approaches to take. One is optical sensing (imaging) [1], another is potential sensing with capacitively coupled electrodes [2], and the other is voltammetric analysis with conductive electrodes [3]. In the present work, we designed a novel image sensor with all the three sensing functions. We designed an optical/electric multifunctional-sensing pixel and columnar circuitry to achieve the optical / potential / voltammetric triple imaging functions.

2. Sensor design

Fig. 1 shows concept of the two kinds (potential and voltammetric) of on-chip electric imaging implemented on the present CMOS image sensor. Fig. 2 shows micrographs and Table 1 shows specifications of the fabricated sensor. Fig. 3 shows schematic and layout of the optical / electric multifunctional-sensing pixel designed for the multifunctional CMOS image sensor. The pixel consists of two sets of reset / readout circuits of 3-Tr APS. For optical sensing, conventional 3-Tr APS is implemented. On the other hand, in the electric sensing part of the pixel, the sensing node (cathode) of the PD in APS was replaced with a sensing electrode. The sensing electrode was formed with the top metal layer. As fabricated, the sensing electrode is covered with passivation layers of the standard LSI structure. The sensor is used as a capacitively-coupled on-chip potential image sensor. Since the pixel was designed with parallel output configuration, the optical and electric sensing functions can be simultaneously operated.

The sensing electrode has a reset transistor (M_4). Without the reset transistor for the electrode, the potential sensing function suffers from residual charge in the electrodes as large offset in pixel characteristic [4]. The reset line for the electrode is also used to establish a current path in voltammetric imaging function.

Fig. 4 shows schematic of columnar circuitry of the sensor. The columnar circuitry consists of two sets of a columnar load unit and a pmos source follower for optical and electric columnar signal lines, respectively. Each load unit has both nmos and pmos loads. Switching the applied voltage on pixel (**Vdd_Pixel** in Fig. 3(a)), and biasing pmos and nmos loads appropriately, the pixel amplifier transistor (M_2, M_5) can be operated in both source follower and common source mode.

To implement the voltammetric function on the sensor, not only voltage sensing path, but also a current supply path and current sensing circuitry are required. As noticed previously, the current path between the columnar circuitry and pixel is established with the reset line. In order to use the sensing electrode for voltammetric measurement, a voltage follower with resistance feedback is configured in each column. The current injected through the sensing electrode into measured object is estimated from a difference between input and output voltages of the sensing amplifier.

As shown in Fig.4, the sensor has four output channels for (1) PD level, (2) electrode potential, (3) input monitor for the amplifier, and (4) output of the amplifier. The 4-channel configuration enables to simultaneously operate the optical and electric imaging function. Furthermore, in voltammetric imaging operation, the potential of the electrode can be monitored via the output channel (3). The voltage difference between columnar circuit and sensing electrode due to the parasitic resistances in columnar **V1** line and transistors can be compensated owing to this feature.

3. Characteristics of the fabricated multifunctional imager

Imaging functions with the optical and electrical multifunctional pixel was demonstrated. The sensor and wires in a ceramic package were molded with epoxy resin. A water droplet was placed on the sensor surface and two tungsten electrodes were placed in the water. The tips of the tungsten electrodes are placed on the sensor surface. Fig. 5 shows (a) experimental setup, (b) optical image, and (c) potential image taken with the present sensor. Potentials of the two

electrodes were set as 0V (left), and 3V(right). The potential images were taken without removing the passivation layer. Thus, the image is taken under capacitively-coupled potential sensing mode. In Fig. 5 (a), two electrodes with shadows on the sensor were observed. In the optical image (Fig. 5 (b)), two shadows of the electrodes were observed. In the potential image (Fig. 5 (c)), potential distribution in water evoked by the electrodes were imaged.

In order to extend the sensor functionality and enable the voltammetric imaging mode, the passivation layer of the sensor should be removed. Reactive ion etching process can be used for the removal of the passivation layers. However, using the potential imaging function, the removal of the passivation layers can be performed more correctly and safely. At first, the top passivation layer (silicon nitride) was removed with RIE process. Then the silicon oxide layer on the sensing electrodes was etched with diluted HF (or buffered HF) solution. During the etching process, the sensor is operated in potential sensing mode, and potential of the HF solution is pulled up at 3.0V.

Fig. 6 shows *in situ* observation of the removal process of the passivation layer. At first, the potential sensing function is in capacitive coupling mode, and it turns conductive coupling mode as the passivation layer is etched away. The removal of the passivation layer on the sensing electrode can be observed as a drastic change of the pixel value. At the last stage of the Fig. 6, all the pixels exposed to the etching solution turns into conductive coupling mode.

Fig. 7 shows a typical current measurement characteristic of the column operational amplifier for voltammetric measurements. The feedback resistance was 10kOhm. The measurement was performed using a current source which was directly connected to the V1 line. We confirmed that the column amplifier is correctly working and current injected through V1 line can be measured with an acceptable linearity for voltammetric measurements used in electrochemical applications.

Acknowledgements

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References

[1] F. Mallard, G. Marchand, F. Ginot, and R. Campagnolo, "Opto-electronic DNA chip: high performance chip reading with an all-electric interface," Biosensors and Bioelectronics, **20** (2005), 1813-1820.

[2] B. Eversmann, M. Jenkner, F. Hofmann, C. Paulus, R. Brederlow, B. Holzapfl, P. Fromherz, M. Merz, M. Brenner, M. Schreiter, R. Gabl, K. Plehnert, M. Steinhauser, G. Eckstein, D. S.-Landsiedel, and R. Thewes: IEEE J. Solid-State Circuits **38** (2003) 2306-2317.

[3] K. Dill, D. D. Montgomery, A. L. Ghindilis, and K. R. Schwarzkopf, "Immunoassays and sequence-specific DNA detection on a microchip using enzyme amplified electrochemical detection," J. Biochem. Biophys. Methods, **59** (2004) 181-187.

[4] T. Tokuda, A. Yamamoto, K. Kagawa, M. Nunoshita and J. Ohta: Sens. Actuators A **125** (2006) 273-280.

Table 1: Specifications of the multifunctional sensor

Technology	0.35 μm 2-poly, 4-metals standard CMOS
Functions	Optical imaging Potential imaging (capacitive / conductive coupling) Voltammetric imaging (conductive coupling)
Chip size	3980 μm x 4080 μm
Array size	320 x 240
Pixel size	7.5 μm x 7.5 μm
PD area (Fill factor)	10.8 μm^2 (19.2 %)
Electrode area	38 μm^2
Readout	Analog voltage

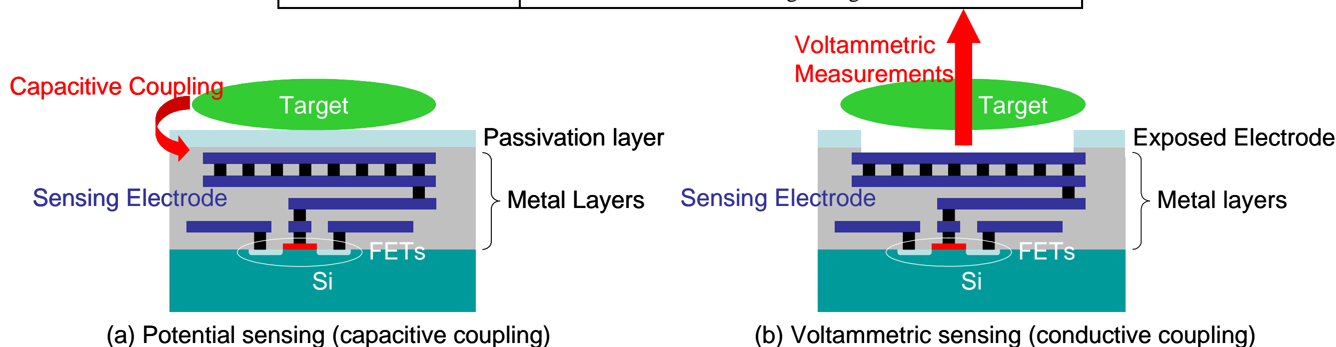

Fig. 1: Two kinds of on-chip electric sensing: potential (capacitive coupling) and voltammetric imaging.

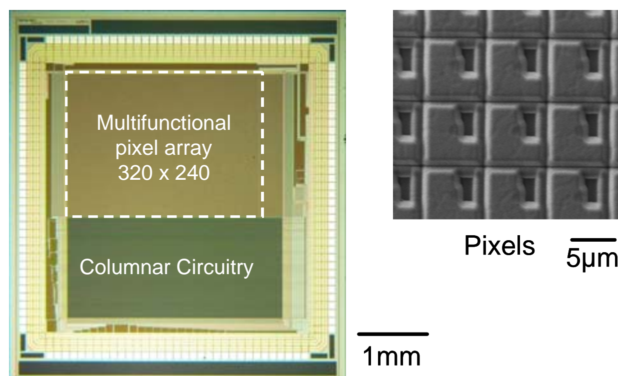

Fig. 2: Micrographs of the fabricated multifuncional image sensor.

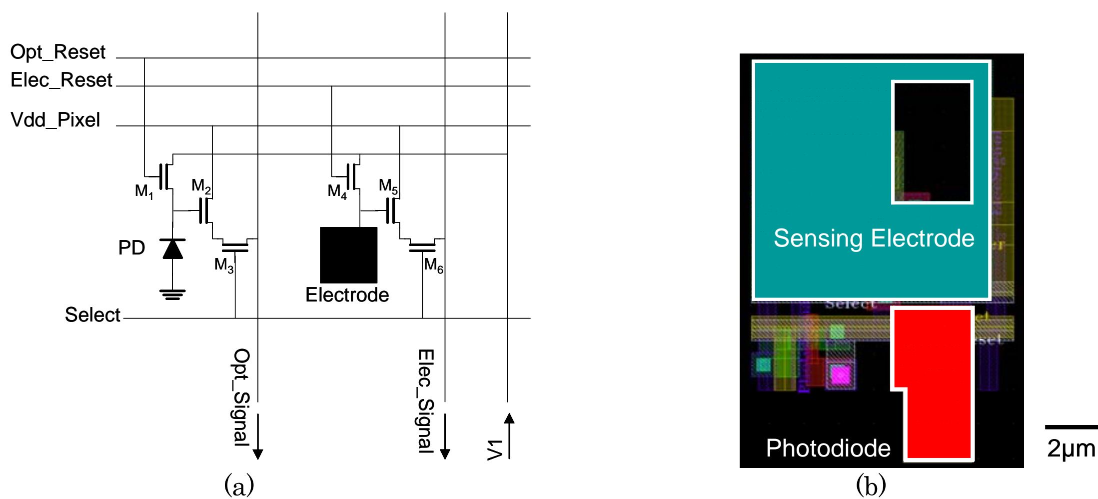

Fig. 3 (a) Schematic and (b) layout of the optical / electric multifunctional pixel.

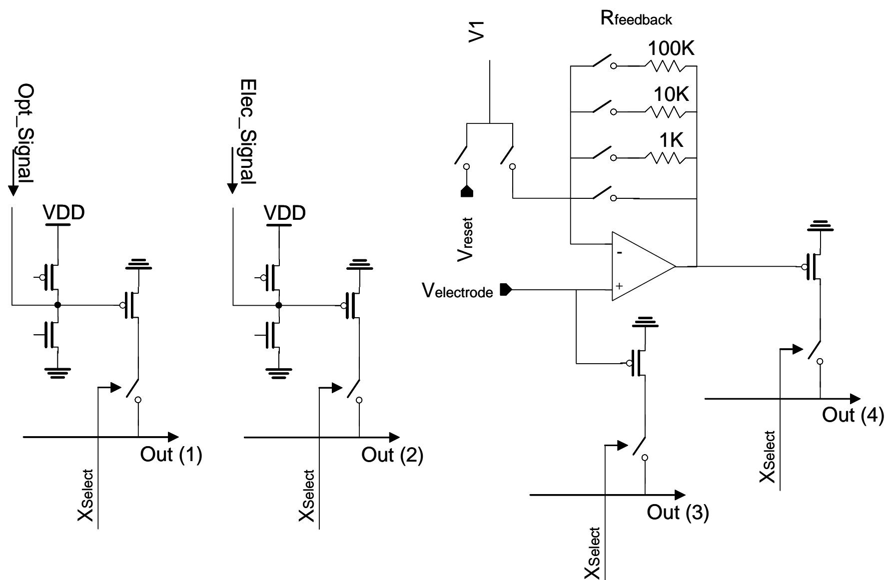

Fig. 4: Schematic of columnar circuitry of the optical / potential / voltammetric image sensor

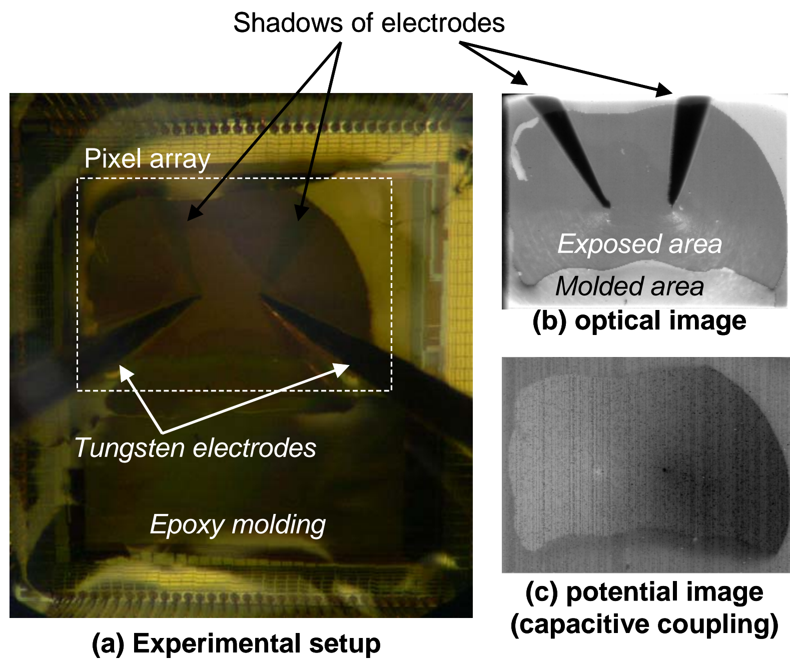

Fig. 5: (a) Experimental setup (b) optical image, and (c) on-chip potential (capacitive coupling) image of two electrodes in water. Potentials of the two electrodes are 0V(left) and 3V(right).

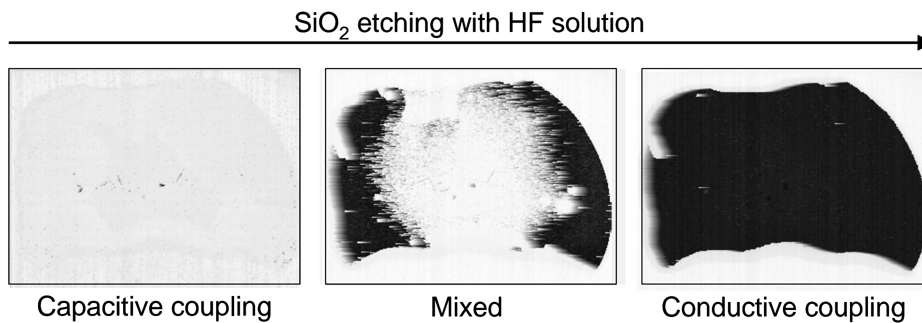

Fig. 6: Transition of the potential measurement mode from capacitive coupling to conductive coupling in etching process of SiO_2 passivation layer. Potential of the HF solution was kept at 3.0 V.

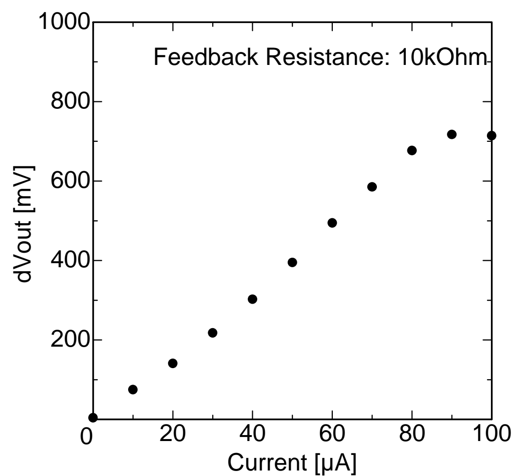

Fig. 7: Current measurement characteristic of the column operational amplifier for voltammetric measurements. The feedback resistance was 10kOhm

Design and Packaging of an Implantable CMOS Neural Imaging and Interface Device

D. C. Ng[1], T. Nakagawa[1], T. Mizuno[1], T. Tokuda[1], M. Nunoshita[1],H. Tamura[2], Y. Ishikawa[2], S. Shiosaka[2], and J. Ohta[1]

[1]Graduate School of Materials Science
[2]Graduate School of Biological Sciences
Nara Institute of Science and Technology, Nara, JAPAN
Tel: +81 743 72 6054, Fax: +81 743 72 6052, email: n-david@ms.naist.jp

Abstract

We present a CMOS image sensor device for neural imaging and interfacing. The sensor device is post-processed using MEMS microfabrication technique to enable backlit illumination. Pt electrodes are formed on the device for electrical stimulation of neurons. A specially developed packaging technique, which includes a color filter that increases the signal-to-noise ratio for on-chip fluorescence imaging, was used. In vivo experiments inside the mouse hippocampus verifies the use of the device for simultaneous imaging and electrical stimulation.

I. Introduction

Microfabrication techniques combining MEMS and CMOS technologies have recently been demonstrated to be an attractive platform for the development of many bioimaging and biosensing devices [1], [2]. While devices fabricated using CMOS technology have been shown to be capable of a host of sensing parameters like photons, pH, temperature, ion, and force, postprocessing with MEMS micromachining technologies enable these devices to be deployed to its intended application. Examples of these devices for medical and scientific research include, brain recording chips, camera pills, smart microdialysis chips, and artificial retinal prosthesis [3] – [6].

We have been working on a new neural imaging approach based on CMOS image sensors. In the past, we have demonstrated capability of contact imaging in vivo for discerning the time course of serine protease activity inside the mouse hippocampus [7]. The advantage of using a CMOS imaging device is high imaging resolution offered by this technology. Apart from imaging, the capability for electrical stimulus and recording is another advantage. A device that is capable of imaging and also electrical interface will enable simultaneous physiological and imaging experiments to be performed, promising new approaches for the study of the brain.

In this work, we developed a new CMOS image sensor device with embedded Pt electrodes. This new device is realized by a combination of sensor design and microfabrication techniques. We have also incorporated illumination light sources and chemical delivery onto the device thus realizing a single minimally invasive neural imaging and interface device.

II. CMOS Sensor Chip

The CMOS chip is specially designed for imaging the mouse brain (Fig. 1). The imaging element consists of an array of 3-transistor active pixel sensors. The sensor circuit schematic is shown in Fig. 2. To reduce the number of input-output pads, row and column scanners, instead of decoders were utilized. Also, the output signal is read-out serially from a single output pad. Four independent electrodes are strategically located within the imaging array to provide electrical stimulus and recording inside the mouse hippocampus. To minimize injury during insertion into the brain, the contact area in front of the chip is hyperbolically curved. Next, we designed backlit vias onto the sensor to enable backlit illumination from a LED light source. This will enable a more uniform light distribution on the image sensor, and also eliminate the use of excitation light filters. The chip was fabricated using standard 0.35 μm CMOS process.

III. MEMS Postprocessing and Packaging

In order to use the device for in vivo imaging, a special postprocessing and packaging process has been developed. The process flow is shown in Fig. 3. First, an Al etch mask for etching the backlit vias was patterned onto the backside of the chip. The backlit vias were etched using the DRIE Bosch process. The chip was etched until the passivation layer was reached. This layer is transparent to the illumination light from the LED (wavelength 365

nm). Next, the LED was attached to a flexible preprinted polyimide substrate by means of flip-chip bonding. The post-processed chip was then attached on top of the LED. A filter which has cut-off wavelength below 400 nm was spin coated onto sensor surface. This special filter is used to block off the LED light but allow higher wavelengths to pass through hence increasing the signal-to-noise ratio of fluorescence light. A YAG laser was used to ablate the sites coated with filter for subsequent wire bonding. The input-output pads were wire-bonded to the polyimide substrate, followed by formation of a platinum (Pt) bump electrodes onto the embedded Al electrode. Finally, the device was sealed in a transparent epoxy and a needle was attached for injection of chemical inside the brain.

IV. Device Characteristics

Fig. 4 (a) shows the packaged device without filter coating. When a single LED under the device was turned on, illumination light was observed from the backlit vias. This was captured by the image sensor device as shown in Fig. 4 (b). Also, the difference between images in free space and inside a brain phantom, prepared with 6.6% skim milk mixed uniformly inside 1% wt agarose gel, was observed. AMC fluorophore (absorbance peak: 380 nm, fluorescence peak: 460 nm) was mixed into the phantom and fluoresce when illuminated with light from the LED.

The device was used for fluorometric measurement of AMC inside the brain phantom. From the measurement result shown in Fig. 5 (a), a minimum AMC concentration of 10 μM was successfully detected. The characteristics of the Pt electrodes were determined by impedance measurement inside phosphate-buffered solution. Fig. 5 (b) shows the measured result as compared to conventional stainless steel (SS) 100 µm diameter electrodes commonly used for electrical stimulation inside the mouse brain. The result shows that the Pt electrodes perform comparably to that of conventional SS electrodes.

V. In vivo Verification

Preliminary experiments in vivo have been performed inside the mouse brain. The device was inserted into the Schaffer collateral region of the hippocampus and pulse stimulus currents of various intensities were applied. A separate recording electrode placed at the CA1 region was used to record the postsynaptic neural potential. The recorded signals are shown in Fig. 6. From this experiment, it is concluded that the device can be used for on-chip electrical stimulation of the neuron cells.

Acknowledgement

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References

[1] A.C.R. Grayson, R.S. Shawgo, A.M. Johnson, N.T. Flynn, Li Yawen, M.J. Cima, Langer, R, "A BioMEMS Review: MEMS technology for physiologically integrated devices," *Proc. IEEE*, vol. 92, pp. 6-21, 2004.

[2] O. Brand, "Microsensor integration into systems-on-chip," *Proc. IEEE*, vol. 94, pp. 1160-1176, 2006.

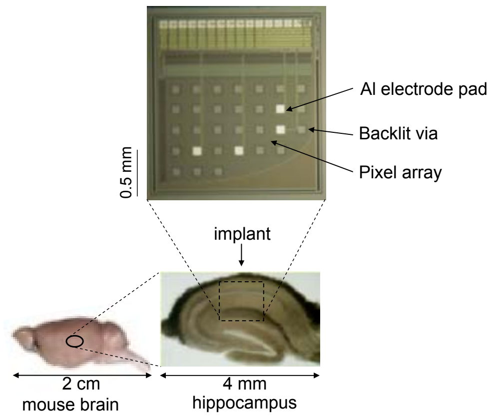
[3] L. R. Hochberg, M. D. Serruya, G. M. Friehs, J. A. Mukand, M. Saleh, A. H. Caplan, A. Branner, D. Chen, R. D. Penn, J. P. Donoghue, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, pp. 164-171, Jul. 2006.

[4] G. Iddan, G. Meron, A. Glukhovsky, P. Swain, "Wireless capsule endoscopy," *Nature*, vol. 405, pp. 417, May 2000.

[5] D. R.Walt, "Miniature analytical methods for medical diagnostics," *Science*, vol. 308, pp. 217-219, Apr. 2005.

[6] W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. Granacki, J. Lacoss, J. Wills, "Implantable biomimetic microelectronic systems design," *IEEE Eng. Med. Biol. Mag.*, vol. 24, pp. 66-74, Sep. 2005.

[7] D. C. Ng, H. Tamura, T. Tokuda, A. Yamamoto, M. Matsuo, M. Nunoshita, Y. Ishikawa, S. Shiosaka, J. Ohta, "Real time in vivo imaging and measurement of serine protease activity in the mouse hippocampus using a dedicated complementary metal-oxide semiconductor imaging device", *J. Neurosc. Methods*, vol. 156, pp. 23-30, 2006.



Technology		0.35 μm std. CMOS 4M2P
Operating voltage		3.3 V
Chip size		2 mm x 2.2 mm
Image pixel	type	3-transistor APS
	number	224 x 164
	size	7.5 x 7.5 μm^2
Photodiode	type	Nwell-Psub
	size	19.75 μm^2
Backlit via	size	85 x 85 μm^2
	number	26
Electrode	size	90 x 90 μm^2
	number	4
Image sensor output		Serial analog voltage

Fig. 1 CMOS image sensor device compared to the mouse hippocampus. The chip specification is tabulated on the right

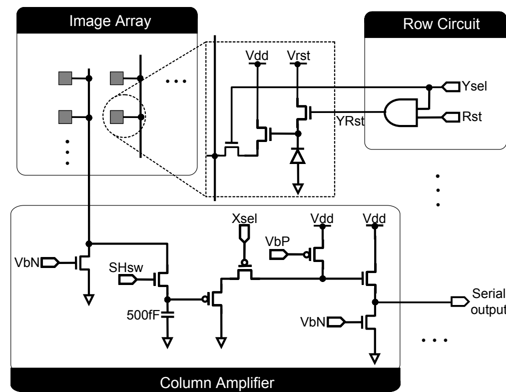


Fig. 2 Schematic of the sensor circuit showing the imaging array, and column and row circuits.

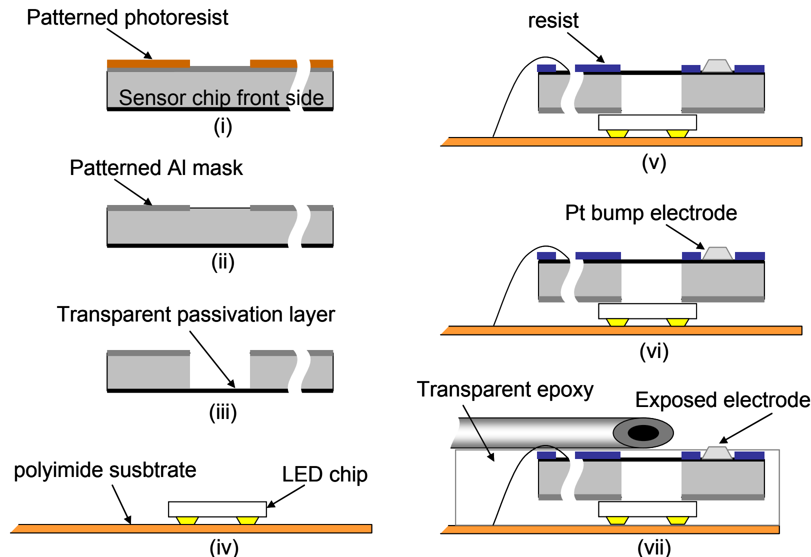


Fig. 3 Post-process and packaging flow of the CMOS device. (i) Sputter Al and pattern photoresist on backside of chip, (ii) wet-etch Al as mask for DRIE, (iii) deep reactive ion etch backlit via and sensor outline (Bosch process), (iv) flip-chip bond LED onto polyimide substrate, (v) attach sensor chip on top of LED and spin coat filter resist, (vi) laser-assisted ablation of resist at bond sites followed by wire bonding of input output pads and forming Pt bump onto Al electrodes, (vii) seal with transparent epoxy and precision laser cut out final shape. An injection needle is attached onto the device for chemical delivery.

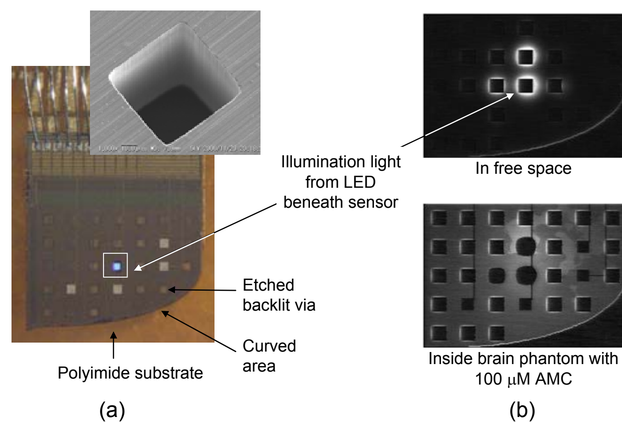


Fig. 4 (a) Photograph of fully post-processed and packaged sensor chip showing illumination from the LED underneath the chip. Inset shows a backside etched via. (b) Captured image from the image sensor chip in free space (upper) and inside a brain phantom (lower).

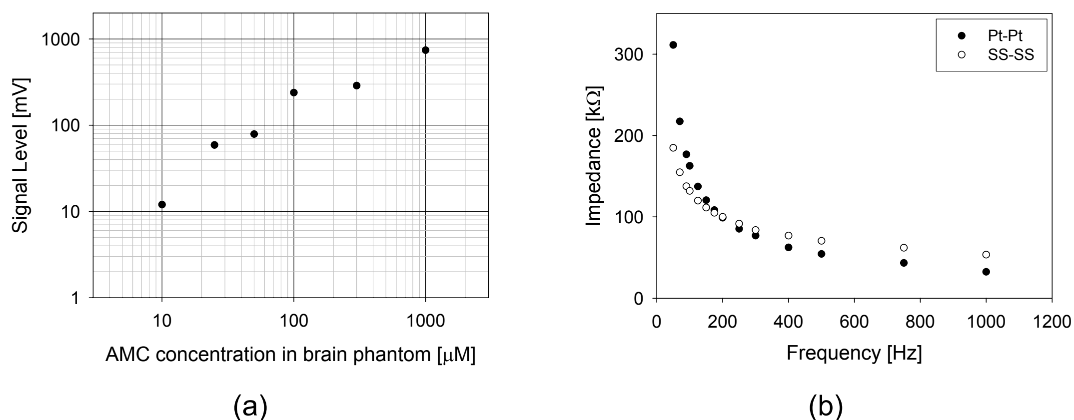


Fig. 5 (a) Fluorometric measurement at various AMC concentration levels inside a brain phantom. (b) Impedance spectrum of the Pt electrodes compared to standard SS electrodes.

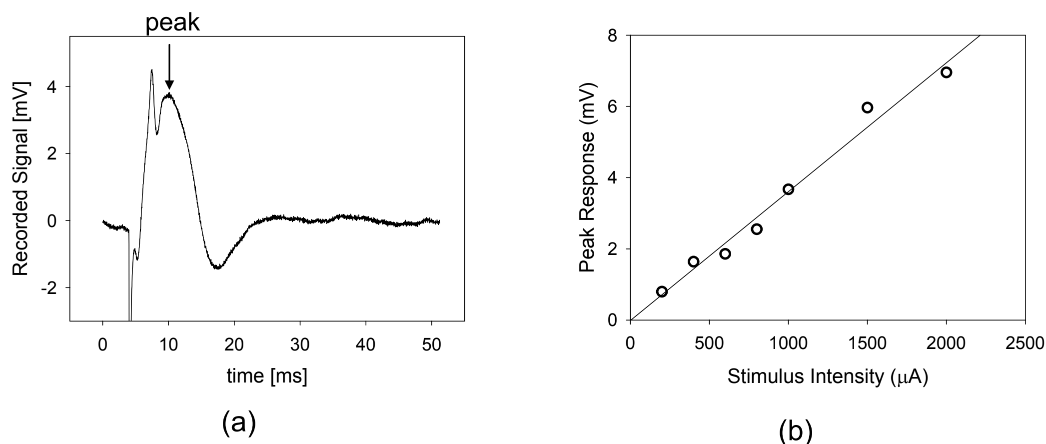


Fig. 6 (a) Typical recorded signal from single pulse stimulation. (b) Recorded peak amplitude is a linear function of input stimulus current intensity.

An Efficient Capacity and Image Lag Simulation Method of CMOS Image Sensor

Kee-Hyun Paik, Jongcheol Shin*, Seok-Ha Lee*, Chang-Rok Moon*, Chang-Hyo Koo, Keun-Ho Lee, Duckhyung Lee*, Young-Kwan Park, and Moon-Hyun Yoo
CAE Team, Technology Development Team*, Memory Division, Samsung Electronics Co., Ltd.
San #16 Banwol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Korea, Tel: +82-31-208-0714, Email: keehyun.paik@samsung.com

Abstract

In this work, we present an accurate, fast, semi-transient, three-dimensional CMOS image sensor cell simulation flow. Capacity, residual electrons and image lag are simulated with 95% accuracy. The simulation has been used successfully in development of CIS cells to provide inexpensive analysis and optimization.

Introduction

Development of CMOS image sensor (CIS) involves dealing with a non-traditional, fully three dimensional device that show strong time dependence. Utilization of TCAD analysis to boost understanding of CIS operation reduces development time.

In CIS, the need for high fill factor, the ratio between photodiode (***PD***) area and unit cell area, demands a complex geometric shape and a fabrication process of which is highly asymmetrical. More traditional simulation analysis based on congregates of two dimensional slices require engineers to expect a priori potential trouble spots and design the simulation domain accordingly. A 3D analysis which avoids the need for such a priori knowledge is worth the additional effort.

It has been shown that three dimensional transient simulation analysis of CMOS image sensor cell operation is very accurate [1]. However, the complexities involving multiple devices residing in one virtual silicon result in high computational burden, requiring several weeks of engineer's effort. This diminishes the transient simulation approach's value as a technology development tool.

A quick running semi-transient simulation method is developed based on analysis of the transient simulation. It is shown to have true predictive capabilities. It successfully predicts saturation signal level preventing early design error and enables engineers to perform detailed optimization process well ahead of costly mask and process commitments.

Transient Analysis

Performing transient simulation on a fully replicated CIS cell can give a comprehensive view of its internal operation. However, having to simulate multiple active devices with a physically large photodiode makes the simulation prohibitively large, the simulation domain is shown in figure 1. Solving such a large problem one must carefully optimize system resource allocation, using sparse mesh on physically large ***PD*** and placing fine mesh over important transfer transistor (***Tx***) channel region.

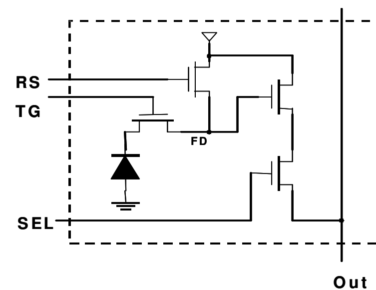


Fig. 1. Transient simulation domain (dotted box), include the entire active pixel sensor circuit.

The resource allocation takes a majority of effort; however, the result is a very accurate replication of CIS cell operation, with much insight into internal state variables.

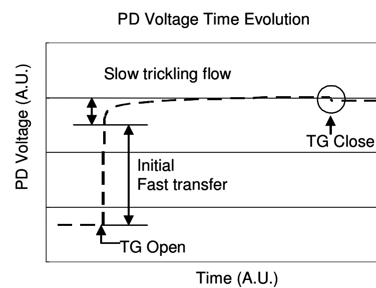


Fig. 2. Above shows the time evolution of the ***PD*** potentials during charge transfer, output of transient simulation. Notice a very fast initial transfer when ***Tx*** opens the potential barrier between ***PD*** and ***FD*** and a much slower electron transfer that follows.

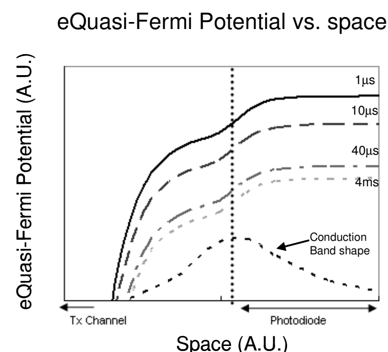


Fig. 3. Electron quasi-Fermi potential during main charge transfer.

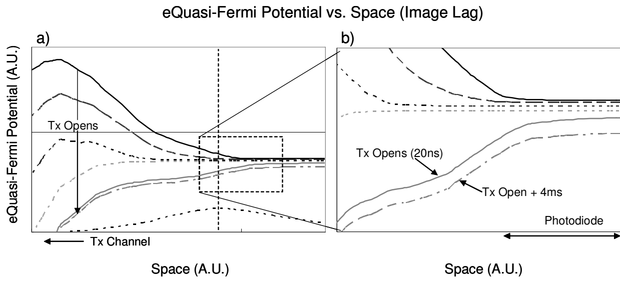


Fig. 4. a) Electron quasi-Fermi potential of image lag, that is during a secondary charge transfer w/o any additional electrons supplied (photonic or otherwise) to the photodiode.

Figures 2 - 4 demonstrate the capability of the transient analysis. Figure 2 shows time evolution of photodiode potential, figure 3 shows the driving force of electron current, electron quasi-Fermi potential, spatially at the edge of ***Tx/PD*** barrier, and figure 4 shows the same when image lag occurs.

As powerful as this method may be, turn around time for result given a novel CIS structure is comparable to actual fabrication, making it difficult to be used in product optimization. However, using the transient simulation, CIS operation is analyzed in detail and a more suitable simulation method is devised.

Construction of Methodology

One can note that capacity, ***C***, is a static quantity. The maximum amount of electrons that ***PD*** will hold should not depend on time. Transfer of the electrons in ***PD*** to floating diffusion (***FD***) is a transient process. Thus, the number of electrons that didn't escape (residual electrons ***R***) is a transient quantity. However simulation based study show that it is only weakly transient, see figures 2 and 3 for time evolution of ***PD*** potential during initial transfer determining saturation and figure 4 for the secondary transfer determining image lag. Further, often ***C*** is larger than ***R*** by orders of magnitude, maximum saturation signal, ***S = C - R***, can be assumed to be time independent. Visual representation of ***C*** and ***R*** are shown in figure 5.

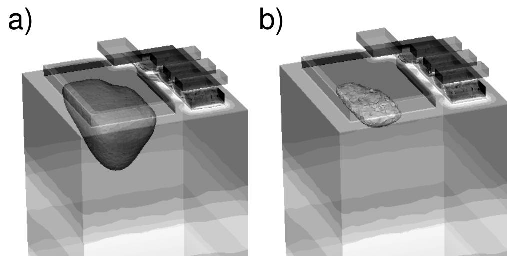


Fig. 5. Visualization of electrons in ***PD*** a) when it is full, and b) when ***Tx*** opens to allow electrons to drain to ***FD***.

The time independence allows decoupled simulation of ***PD*** and the transfer transistor, ***Tx***, reducing overall simulation complexity. ***PD*** and ***Tx*** are simulated separately negating mesh conflict that plagued the transient simulation. Abandoning transient device simulation in favor of static DC simulation also reduces simulation time. The potential barrier between ***PD*** and ***FD*** is the boundary condition that links the two simulations, see figure 6 for the split domain. Simulation results of ***C*** and ***S*** depend very sensitively on the barrier height. Accuracy of simulated capacity in previous works supports that barrier heights being used internally are accurate, see figures 7 and 8.

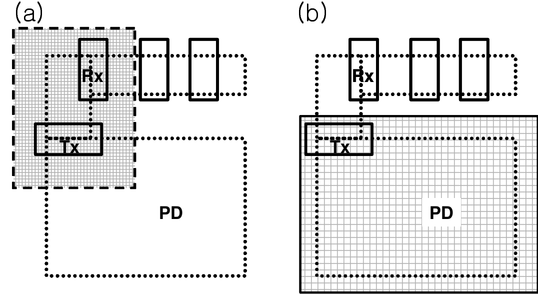


Fig. 6. a) ***Tx*** simulation requires fine mesh over a small spatial domain to capture details of ***Tx*** transistor operation, whereas b) ***PD*** simulation has a more loose mesh requirement over a large spatial domain. Setup of each simulation project is easier than that of full transient simulation with mixed mesh requirements and both can be run in parallel to reduce simulation time.

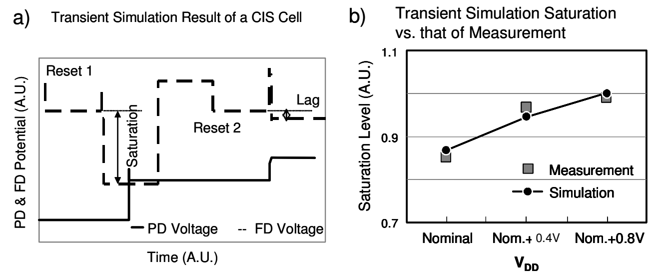


Fig. 7. a) Above shows the time evolution of the ***FD*** and ***PD*** potentials during one full operation of CIS cell, output of transient simulation. b) Change of the saturation level for various V_{DD}. Significant additional output suggests incomplete transfer of PD electrons. The transient simulation of full virtual CIS replicates saturation, ***S***, results very accurately.

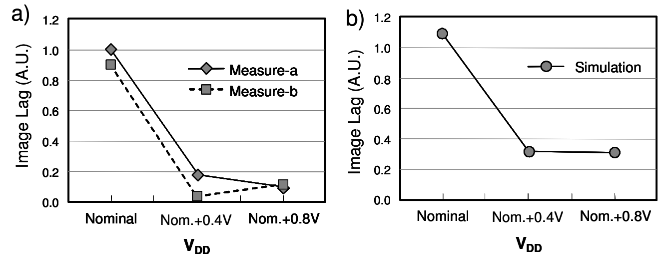


Fig. 8. Comparison between (a) measured and (b) simulated image lags. Simulations and experiments are done by operating CIS twice without supplying addition electrons to PD between the two operations, i.e. 2nd operation done under no illumination.

Based on the observations of transient simulations, a conversion table is compiled for translating the maximum conduction band height under ***Tx***, the potential barrier of interest between ***FD*** and ***PD***, and electron quasi-Fermi level in ***PD*** for various temperatures on *table 1.* Distance to electron quasi-Fermi level is around 11 kT/q.

Table 1. Distance from highest conduction band edge (CB) under ***Tx*** to electron quasi-Fermi level of ***PD*** for various temperatures

Temp. (K)	Dist. to CB (V)	Dist. To CB (kT/q)
353	0.343	11.20
333	0.322	11.15
313	0.299	11.05
293	0.281	11.06

The electron quasi-Fermi level is biased into ***PD***, filling it with electrons to proper energy level. This entirely static approach yields accurate simulation of ***S***, and yields simulation of ***R*** that provides reasonable but somewhat lacking indication of image lag, see figure 9.

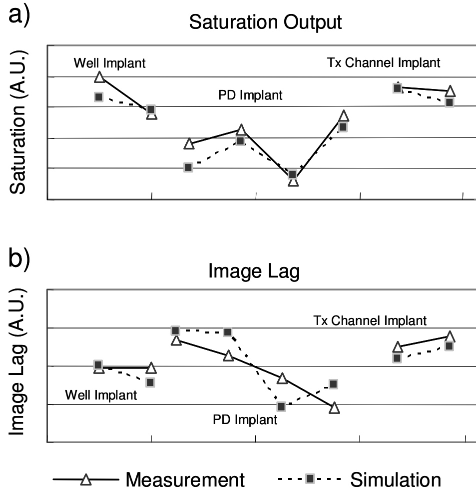


Fig. 9. Comparison of partitioned CIS simulation result vs. experimental data of saturation output and image lag. Saturation shows a very nice fit, all trends are replicated and absolute value are within 10% of experimental data. Image lag and residual electrons show a less smooth matching, for its modeling is less robust. The discrepancy is handled by addition of equivalent circuit SPICE simulation.

Obtaining a more accurate image lag simulation result, as indicated earlier, is more difficult since the quantity is transient in nature.

It would be desirable to keep device simulation static and capture the transient image lag at the same time. To do this, the following equivalent circuit model of ***PD-Tx-FD*** is proposed, see figure 10.

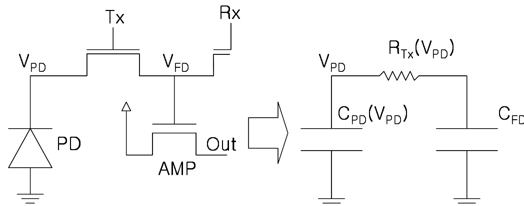


Fig. 10. Equivalent circuit diagram of CIS Cell for more accurate image lag simulation.

R_{Tx} is the ***Tx*** channel resistance when V_g is high. It is a rapidly varying function of V_{PD}. It is extracted by differentiating V_{PD} over I_{Tx} while V_g is high.

$$R_{Tx} = \left.\frac{\partial V_{PD}}{\partial I_{Tx}}\right|_{V_{g_Tx}=high} \qquad (1)$$

Imaginary component of the ***Tx*** channel impedance is non-negligible at certain places, but only weakly affects the resulting saturation and image lag simulation results since during those non-negligible instances CIS behavior is dominated by R_{Tx}.

C_{PD} is the ***PD*** capacitance and is function of V_{PD} and V_{FD}. However, the dependence on V_{FD} is deemed small enough after performing full AC analysis with the relevant variable; thus it is reduced to a mere function of V_{PD}. C_{PD} is obtained by solving Poisson's equation for the ***PD*** and differentiating accumulated charge in ***PD***.

$$C_{PD} = \left.\frac{\partial Q_{PD}}{\partial V_{PD}}\right|_{V_{FD}=high} \qquad (2)$$

C_{FD} is the ***FD*** capacitance. It is simplified to be a constant for it varies little in the CIS cell's operating range. Change of C_{FD} is simulated to be about 4% during CIS operation. This capacitance must also include those contributions by interconnects and amplifier. Or the measured value of C_{FD} near operation condition could be substituted.

Notice that, extracting parameters R_{Tx}, C_{PD}, C_{FD} can be done entirely via static DC simulations.

Above equivalent circuit model was implemented in SPICE and the voltage dependent quantities were described as follows:

$$R_{Tx} = \exp\left(\sum_{i=0}^{6} r_i V_{PD}{}^{i}\right) \qquad (3)$$

$$C_{PD} = \sum_{i=0}^{4} c_i V_{PD}{}^{i} \qquad (4)$$

Describing C_{PD} as a 4th order polynomial was sufficient. It is a relatively slowly varying function of V_{PD}. However, R_{Tx} rapidly falls at a point. This occurs when ***Tx*** channel potential is no longer controlled by its gate bias. Since it was more important to capture R_{Tx} behavior during this rapid exponential fall off, polynomial interpolation in log space was chosen. Figures 11 and 12 show the fitted results.

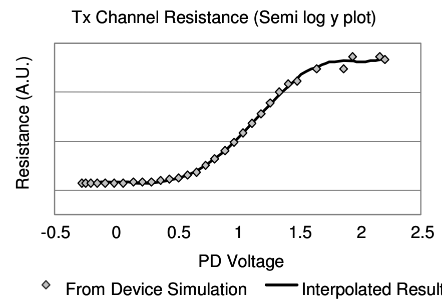


Fig. 11. ***Tx*** channel resistance computed by device simulation and interpolated function fitted to represent R_{Tx}.

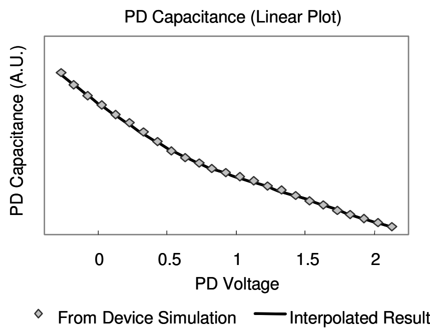


Fig. 12. ***PD*** capacitance computed by device simulation and interpolated function fitted to represent C_{PD}.

Initial value of V_{PD} and V_{FD} can be obtained from static simulations and using Table I. With initial conditions known, SPICE simulation for the equivalent CIS circuit can be performed in a very short time, in order of minutes. Figure 13 shows the simulated result and figures 14 a) and 14 b) show the simulated saturation signal and image lag and the subsequent experimental result.

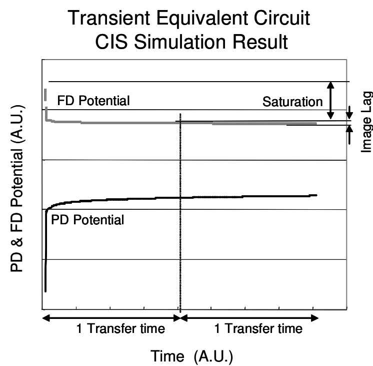


Fig. 13. Above shows the output of equivalent circuit CIS cell image lag simulation. Time evolution of ***PD*** and ***FD*** are shown with saturation and image lag marked.

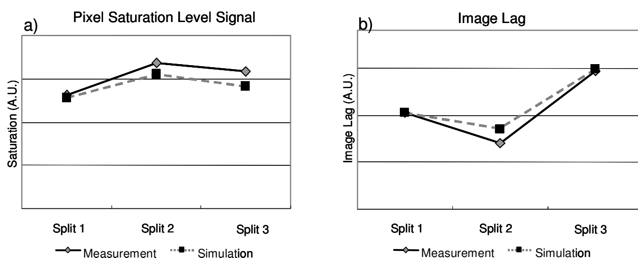


Fig. 14. Above shows the predicted saturation level output of 1.7um pixel pitch CIS cell. Having done process calibration with previous generation device, saturations of each split were predicted a month ahead of actual experiments.

Application

During development of 1.7x1.7um^2 and 1.75x1.75um^2 pixel CIS this simulation was used extensively [3][4]. Moving from 1.9x1.9um^2 pixel CIS [2] the optimal gate length was determined prior to device fabrication and verified in experiment. Shorter gate length would mean larger ***PD*** size and thus potentially larger ***PD*** capacity. However, too short a channel would ruin the ***Tx***' ability to form an effective barrier between ***PD*** and ***FD*** and result in lowered ***PD*** capacity. Simulated prediction of this analysis is shown in figure 15.

The portion labeled short channel effect (SCE) notes the loss in capacity due to shorter ***Tx***' inability to form effective barrier between ***PD*** and ***FD***. Based on the simulation a more focused experimental mask split was designed to optimize ***Tx*** gate length more efficiently, see figure 16.

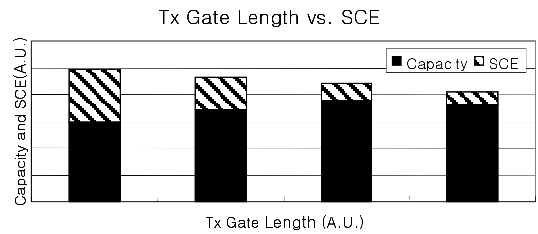


Fig. 15. For 1.7um CIS, above is the comparison of net capacity (the capacity when ***Tx*** barrier is as high as that of 1.9um CIS ***Tx***), and effective capacity (the capacity defined in section 2 of this work). The difference is defined as SCE of CIS.

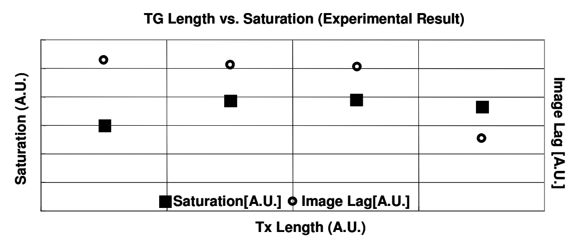


Fig. 16. Optimization performed on 1.7um CIS ***Tx*** gate length. Countering SCE by larger gate a point where decreasing net capacity conceptualized in figure 15 and effective capacity defined.

Conclusions

A fast and accurate electrical characteristic simulation methodology for CMOS image sensor cell that is fully three dimensional and avoid time consuming device level transient analysis, was conceived during development of 1.9um pixel pitch CIS cell, and applied in all stages of 1.7um and 1.75um pixel pitch CIS development with great success.

Simulation methodology described in this work reduced analysis time by allowing detailed look inside a CIS cell, enabling fast problem correction head of costly fabrication commitments. Early stage layout evaluation ruled out design errors reducing engineering iteration of costly mask correction.

References

[1] K.-H. Paik, *et al.*, SISPAD, p. 103, 2005.
[2] C.-R. Moon, *et al.*, IEDM Tech. Dig., p. 813, 2005.
[3] S.-H. Lee, *et al.*, Symp. On VLSI Tech., p. 178, 2006.
[4] J. Kim, *et al.*, IEDM Tech. Dig., p. 123, 2006.

3-D Wave Optical Simulation of Light Wave-guide Structures by Localized Boundary Element Method

Hideki Mutoh and Shigetoshi Sugawa*
Link Research Corporation
*Graduate School of Engineering, Tohoku University

1-18-5, Kojima, Taito-Ku, Tokyo, 111-0056 Japan
*6-6-11, Aza-Aoba, Aramaki, Aoba-ku, Sendai, 980-8579 Japan
Phone: +81-3-3851-9871, E-mail: hideki.mutoh@nifty.com
*Phone: +81-22-795-4835, *E-mail: sugawa@fff.niche.tohoku.ac.jp

Abstract

The analysis of the light gathering power and cross-talk in the light wave-guide structures by 3-D wave optical simulation is reported using Localized Boundary Element Method. Air is better isolation material than SiO2, aluminum, or tungsten to improve the light gathering power. If SiO2 is adopted as the isolation material, light absorbent or reflective material would be needed in the isolation region to improve cross-talk characteristics.

I. Introduction

The pixel size of image sensors has been reduced continuously. With reducing the pixel size of CMOS image sensors, their lower sensitivity than CCD image sensors becomes serious problem. Although CCD image sensors can use the low level micro-lens or inner lens structure [4], CMOS image sensors cannot adopt it, because of the multi-level metal wiring. Therefore, wave-guide structures have been proposed to improve the sensitivity of CMOS image sensors [1], [2]. In order to realize 3D wave optical analysis for image sensors, we have developed a 3D wave optical simulator by Localized Boundary Element Method (LBEM) [3], [5]. This method can execute 3D simulation much faster than conventional boundary element or FDTD method. The wave optical analysis of the light gathering power and cross-talk in wave-guide structures by LBEM is reported.

II. Light gathering power of single micro-lens

Fig. 1 shows the structure for the micro-lens light gathering power analysis consisting of sphere micro-lens made of material with refractive index of 1.7 and silicon substrate, where “w”, “h”, and “d” denote the cell size, micro-lens height, and the distance between the bottom of the micro-lens and the silicon surface, respectively.

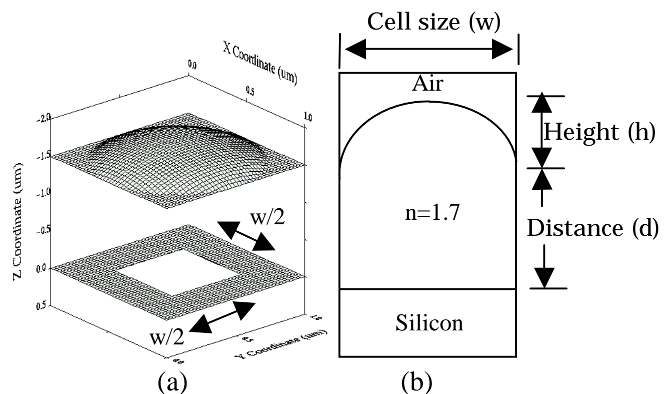


Fig. 1. Structure for wave optical simulation of light gathering power dependence on cell size, lens height, and distance. (a) Bird’s eye graph where center of the plane of Z=0 is the photo-sensitive region. (b) vertical cross-sectional view in XZ plane of y=w/2.

Fig. 2 shows the light gathering power dependence on d, h, and w, calculated by LBEM with 550 nm vertical incident light. The unit of the horizontal axis is cell size. The similar result has been obtained by FDTD method.

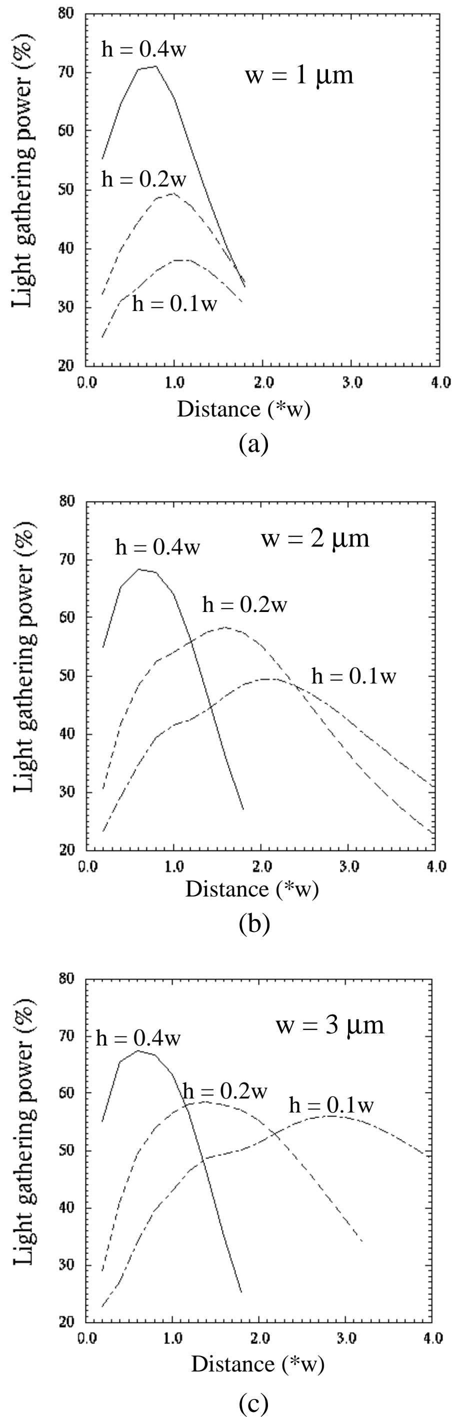


Fig. 2. Light gathering power dependence on cell size, lens height, and distance by 550 nm vertical incident light. (a) w = 1 µm, (b) w = 2 µm, (c) w = 3 µm.

It is found that the larger micro-lens height gives the larger peak of light gathering power. In the case of small micro-lens height, the distance for the largest light gathering power decreases with reduction of the cell size. Therefore, large distance micro-lens cannot obtain the large light gathering power in the small cell size case.

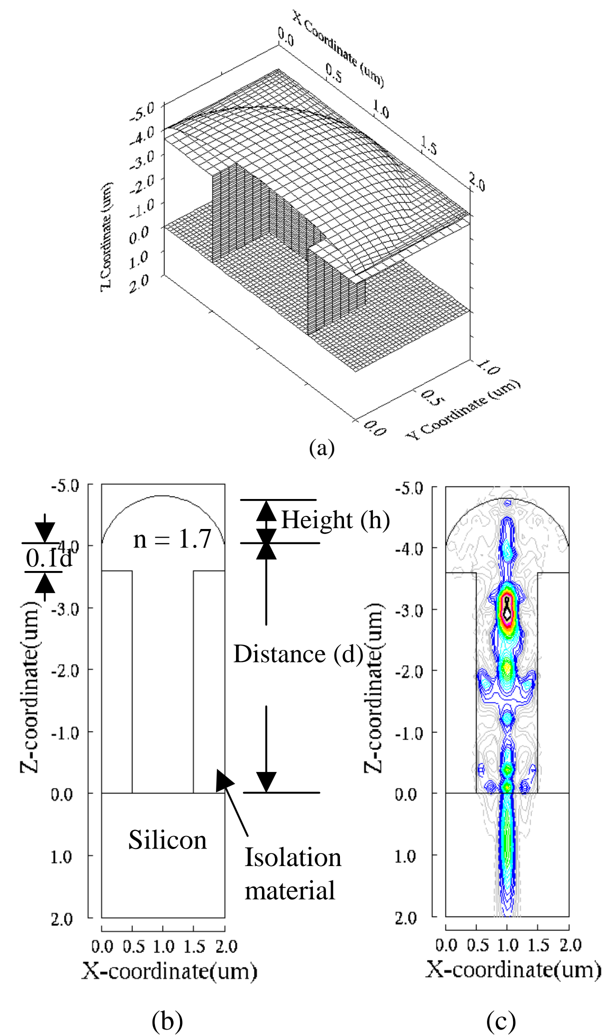


Fig. 3. Structure for analysis of Llight gathering power dependence on cell size, lens height, and distance. (a) Bird's eye view, (b) vertical cross-sectional view in XZ plane of y=0, (c) Light intensity distribution by 550 nm vertical incident light.

III. Light gathering power of wave-guide structures

Fig. 3 shows a wave-guide structure for this analysis, where h and d denotes the micro-lens height and the distance of wave-guide from entrance to exit, respectively. The inside material of the wave-guide has as same refractive index of

1.7 as the micro-lens, and the outside (isolation) material is assumed to be air (n=1), oxide (n=1.5), aluminum (n=0.5+3.9i), or tungsten (n=4+2.2i).

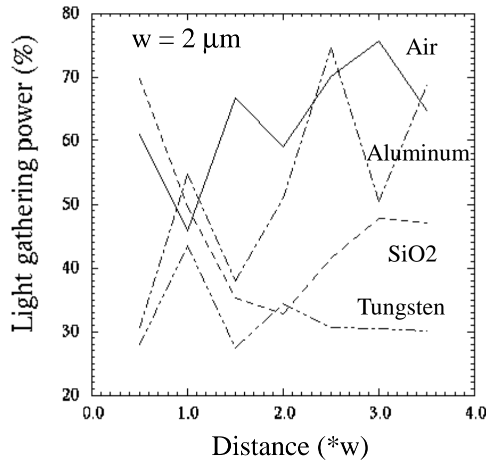


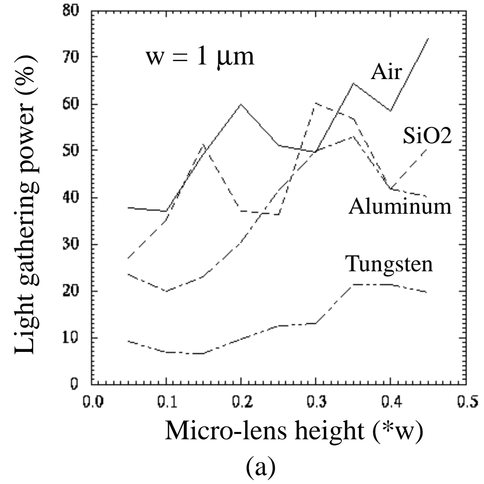
Fig. 4. Light gathering power dependence on the distance and isolation material by 550 nm vertical incident light.

A. Light gathering power dependence on distance

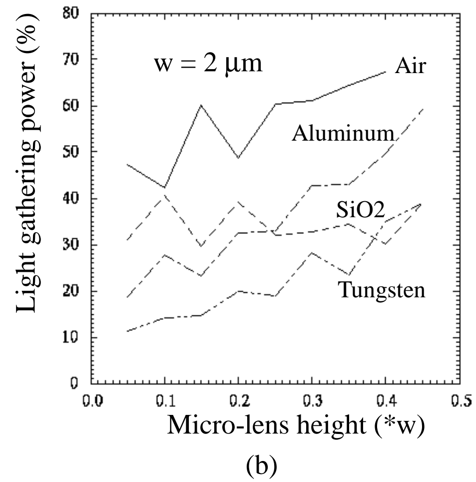
Fig. 4 shows the light gathering power dependence on the distance and isolation material in the case of w = 2 and h = 0.4 w. Although large interference exists, it is found that the light gathering power does not decrease with the increase of the distance d, except the tungsten case. In the tungsten case, the longer tungsten wall absorbs the lager part of incident light, because of its low reflectance and large absorption coefficient.

B. Light gathering power dependence on height

Fig. 5 shows the light gathering power dependence on the micro-lens height and isolation material in the cases of w = 1 and 2, where micro-lens distance d is 2 w. It is found that the light gathering power increases with increase of the micro-lens height as similarly shown in Fig. 2 and air is better isolation material than aluminum, SiO2, or tungsten to obtain large light gathering power. Because air isolation gives the largest total reflectance at the side-wall of the wave-guide in consideration of the angle range of the light through the micro-lens to the side-wall.



(a)



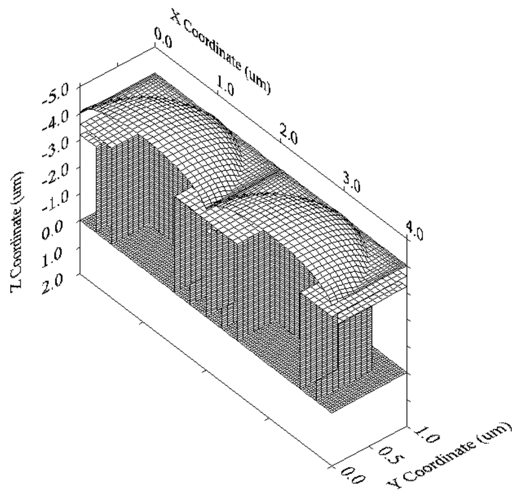
(b)

Fig. 5. Light gathering power dependence on the micro-lens height and isolation material by 550 nm vertical incident light. (a) w = 1 μm, (b) w = 2 μm.

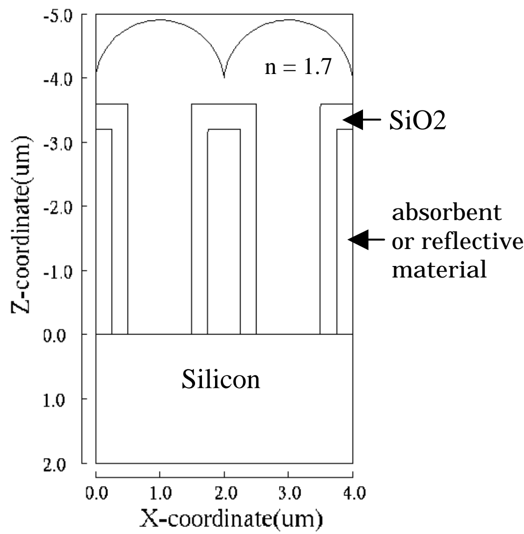
IV. Cross-talk of wave-guide structures

Fig. 6 shows the structure for the cross-talk analysis consisting of two cells of the wave-guide structure with the micro-lens height of 0.45 w and distance of 2 w, where only left micro-lens is illuminated. The isolation region is made of SiO2 and light absorbent or reflective material. Fig. 7 shows the cross-talk dependence on the incident light angle. The cross-talk value is defined as the light gathering power ratio between the right and left cell. The structure of SiO2 isolation without absorbent nor reflective material has large cross-talk, which increases with increase of the incident light angle. The absorbent or reflective

material in SiO2 isolation region can effectively reduce cross-talk.



(a)



(b)

Fig. 6. Structure for analysis of cross-talk dependence on incident light angle. (a) Bird's eye view, (b) vertical cross-sectional view in XZ plane of y=0.

V. Conclusion

The wave-guide structure can efficiently improve the sensitivity and cross-talk of CMOS image sensors. It was found that air is better isolation material than SiO2, aluminum, or tungsten for the structures to improve light gathering power. If SiO2 is adopted as the isolation material to avoid unfamiliar process or reliability problems, light absorbent or reflective material would be needed in the isolation region to improve cross-talk characteristics.

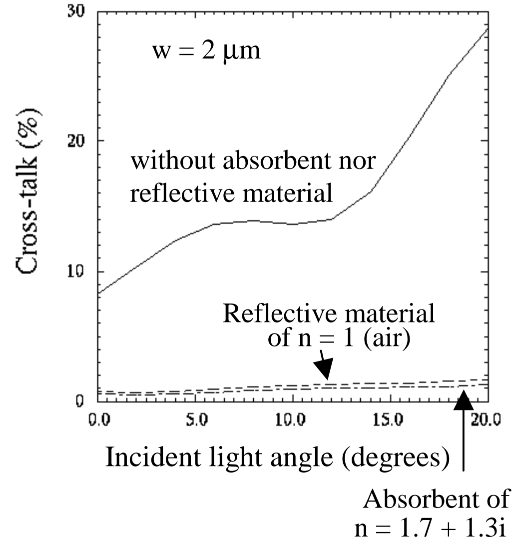


Fig. 7. Cross-talk dependence on the incident light angle in 2 μm cell by 550 nm incident light.

References

[1] D. N. Yaung et al, "Air-gap guard ring for pixel sensitivity and crosstalk improvement in deep sub-micron CMOS image sensor," IEDM Tech. Dig., pp. 401-404, Dec. 2003.

[2] T. H. Hsu et al, "High-Efficiency Dielectric Structure for Advanced CMOS Imagers," Proceeding of 2005 IEEE Workshop on CCD and AIS, June 2005.

[3] H. Mutoh, "Optical simulation for image sensors by wave analysis," Proceeding of 1997 IEEE Workshop on CCD and AIS, June 1997.

[4] H. Mutoh, "3-D wave optical simulation of inner-layer lens structures," Proceeding of 1999 IEEE Workshop on CCD and AIS, June 1999.

[5] H. Mutoh, "High Speed 3-D Wave optical Simulation for Image SensorsProceeding of 2005 IEEE Workshop on CCD and AIS, June 2005.

What Camera Manufacturers Want

Sunita A. Mathur, Michael A. Okincha, Michael D. Walters
VistaPoint Technologies, 2241 Lundy, San Jose CA 95131

Abstract—**Rapid advances in CMOS image sensors and SOCs, (which include image processing) are currently taking place. To date these advances have enabled the rapid proliferation of cameras in mobile phones and other consumer electronic devices. This paper takes the viewpoint of the camera manufacturer and describes what further advances are most needed to reduce the cost, size and to further improve the quality, performance, and yield of camera modules.**

I. Introduction

Camera module annual shipments grew from ~20Mu in 2002 to >550Mu in 2006 and is one of the fastest growing products in digital imaging. Module production is pushing many technical and process boundaries. This article briefly discusses the market for camera modules, and focuses on the cutting edge technical issues and developments in module construction and assembly, imager die layout, pixels trends, image processing, calibration, test, singulation, sawing and transport.

II. Camera Markets

What camera module manufacturers want is fundamentally driven by end-market and end-user requirements. A fixed focus camera module must be able to take a sharp self-portrait at 20-30cm while also having acceptable sharpness of distant objects, for example.

The primary requirements for mobile phone cameras are acceptable image quality, low-price and small physical size. The mobile handset market can be divided into four segments as shown in Figure 1. In order to access the volumes in each mobile phone market segment the required price points must first be met. The best solution that meets the price point tends to obtain the highest volume. Substantial technology developments are required to increase performance and drive down costs at a compound rate >15%/yr as shown in Figure 1. From 2002 – 2007 increased resolution and lower camera prices were driven primarily by pixel geometry shrinks from 5μm to 1.75μm. Additional technologies like chip-scale packaging and innovative new, low-cost optics are required to be high-volume production ready in the next year to sustain these cost reductions and further expand the camera module market.

III. Camera Module Construction and Assembly

Market demand for ever-smaller camera modules requires that manufacturers utilize the latest in packing and assembly technologies. A block diagram of a typical camera module is shown in Figure 2. VGA resolution camera modules today can be smaller than 5mm x 5mm x 3mm.

Figure 3 shows a sampling of difference camera module designs.

Camera modules use a wide range of assembly technologies. Imager die can be mounted using COB, flip-chip, or chip-scale packages. Die may be mounted on fiberglass or ceramic substrates, or serve as the substrate itself. The lens and IR filter are typically assembled as a subassembly and mounted to the substrate with a plastic housing. During assembly, components may be passively or actively optically aligned. The module can be attached to the handset using either a flexible PCB or board-to-board connector, or the module may be mounted in a socket.

Figure 4 shows the cross-section of a common module design. The bare die imager is epoxied and wire bonded to a fiberglass PCB substrate. The lens/IR filter barrel is mounted to the substrate by a plastic housing. This type of design is rapidly being replaced by more streamlined designs, involving fewer components and assembly steps.

IV. Imager Die Layout Considerations

With few exceptions, camera modules (1) are square in footprint, and (2) have the optical center coincident with the mechanical center. Customers and yield management also prefer everything fit within the housing; protrusions where parts can break off are unwelcome. These requirements place important constraints on the imager die layout.

While the center of the die may intuitively seem like the best place for the center of the pixel array, that is only true when the die is the only component on the substrate top surface. In most real-world applications, the module design includes a variety of passive components. To fit wire bonding pads and these passive components under the housing, the imager die must be shifted from the mechanical center, shifting the pixel array center as well. The ideal amount and direction of shift depends greatly on the module design and assembly processes. Imager vendors must work closely with camera manufacturers to ensure the die layouts permit designs that meet customer requirements.

Figure 5 shows how die layout affects module size. A poorly placed pixel area forces the module to be much larger necessary. By intelligently offsetting the pixel array the module can be much smaller. There is even room for passives without affecting module size.

V. PIXELS

Smaller pixels make for smaller, more cost-effective die, with 1.75µm pixels currently representing the state of the art. As pixel sizes decrease, optical design challenges increase and lens yields decrease. Because the sensor die still represents the majority of the cost of most modules, shrinking the sensor die by reducing the pixel size reduces the overall module cost. At some threshold, however, smaller pixels will increase, rather than decrease, module cost. Figure 6 shows how as pixels shrink, the cost of building a module is dominated by lens cost and manufacturing processes rather than die cost. Smaller pixels are also less sensitive to light and noisier, degrading image quality. Smaller pixels are definitely possible, but it's not clear that they're desirable.

Smaller pixels also complicates the guiding of light to the photodiode, requiring the lens system and die-level optics be better matched. Lens/sensor mismatch can cause pixel noise and chroma nonuniformity in the image corners due to excessive shading correction and sharpness, and focus failures in the center. Since changing the die's optics is faster than changing a lens design, sensor vendors must be willing to tune their optics to match a given lens, rather than the other way round. This may create some inventory management issues, but the alternative is a poorly matched optical system and inferior image quality.

VI. IMAGE PROCESSING

Image processing in camera modules for cell phone applications has been primarily used to correct for lens shading issues and to enhance color performance. The sensor manufacturers have also leveraged it to obscure defective pixels and fixed pattern noise in their products for yield enhancement in the wafer fab. While auto-correction features like auto-white balancing and auto-gain correction ensure that the camera modules are user friendly. However, still the amount of image post processing in cell phone applications has been quite minimal compared to the digital still camera and digital video camera market.

A key area for improvement is compensation for the performance of smaller pixels. Better noise reduction, smarter demosaicking, and improved sharpening algorithms are crucial to reducing color crosstalk, temporal noise, and fixed pattern noise. If the noise of smaller pixels can be managed, low light performance can be maintained without other image quality tradeoffs, like desaturating color or increasing lens f-number.

Bad pixel correction must be able to correct for cluster defects, not just single pixel failures. As will be discussed later, contamination of the imager surface is the largest cause of module defects. Pixel sizes decrease through the use of new manufacturing processes, but dust and other particles stay the same size. The ability to correct bad pixel clusters will reduce module costs both through increased yields and reducing the need to build more expensive or larger clean room facilities.

Better lens shading correction algorithms are needed as well. Lens vignetting correction is called on to undo lens vignetting, lens alignment error, and pixel array nonuniformities in color and photoresponse. Common assumptions like uniform response across color channels, perfect alignment of the lens to the pixel array, and polynomial lens shading functions all need rethinking. New algorithms must correct each channel individually using arbitrary sized grids of control points. Lens correction also must vary with illuminant, since color shading varies with illuminant (daylight, tungsten, fluorescent). Go away, pink centers and blue corners.

Support for the many forms of optoelectromechanical systems, like auto-focus and optical zoom, is also critical. Image processing must offer both custom algorithms and provide a complete, robust solution. Even better, any image processing that eliminates the need for moving parts. Moving parts are expensive to assemble, create particles through friction, and are unreliable. Innovations like extended-depth-of-focus, nontraditional optics, and sophisticated post-processing have the potential to enhance the appeal of fixed focus modules and to allow for more

compact auto-focus and zoom solutions.

Digital still camera features like image stabilization, automatic image judgment, and multiple image capture will migrate over to camera modules.

VII. Camera Calibration

No two camera modules are the same; even within the same production run there will be variations in color response, lens alignment, etc. The industry made significant progress in variation-reducing methods (process control, screening through test), yet typical module performance still falls short of industry demands. The only remaining option is to measure each module's characteristics, and later correct for them, a process generally called calibration.

Calibration has three phases: (1) measuring the performance of each camera module in production, (2) transferring that information to the each handset, and (3) using the information to tune the image processing for optimal image quality. To date, the greatest barrier has been transferring the calibration data to the right handset. The only viable solution is to store calibration data within the camera module itself.

Recently, image sensor suppliers have begun adding nonvolatile memory to their devices. Some include a few bytes, some several kilobytes. An exciting advance, nonvolatile storage will lead to better image quality. But first the industry must decide how to use it. What kind of data is needed for calibration? A good place to start is with the current register set provided to optimize image processing. Module serial number, lens identification, alignment data, color response data (color matrices, or tables), lens shading and sensitivity or linearity data. Calibration data could require a few bytes or many kilobytes, depending on the format and scope.

It's crucial to recognize that having calibration data alone is not enough. The image processing has to be prepared to use it. For example, consider the top view of a camera module shown in Figure 7. The optical center of the camera is represented by a X and is offset from the pixel array center due to lens to SOC misalignment caused by camera assembly. The camera optical center X can be measured during the calibration process and stored in camera memory. To be useful, the camera image processing must use the camera optical center data to adjust the lens shading correction, for example. Another possibility to reduce system costs with shrinking pixels would be to add a few extra rows and columns to systems using 1.4µm pixels. The boundaries of the active pixel array could then be adjusted to compensate for the camera optical center without reduction in resolution.

Very few providers of image processing have clear plans for what calibration data they could use, or in what format. Camera manufacturers can measure many kinds of performance, and record the data in many formats. The industry should openly develop data standards and methods to ease adoption of this key technology.

VIII. Test, Singulation, Sawing and Transport

To optimize yield and quality the camera manufacturers are targeting two areas of improvement of sensor fabrication: surface contamination and test process alignment.

Surface contamination is the single largest source of yield loss in camera manufacturing. Both silicon vendors and camera module assemblers are dedicating enormous effort towards contamination reduction.

The two main sources of contamination are debris from die sawing and clean room processes. Die sawing generates particles, which tend to stick to the organic coatings on the imager surface, as shown in Figure 8. Debris also tends to chip off the edges of the die during handling. Aside from die debris, the surface properties of the die tend to increase contamination.

The organic coatings used for microlenses attract and keep particles through static electricity, van der Waals bonding, and surface tension, reducing the effectiveness of cleaning processes[1]. Glass-on-die technologies aimed to reduce surface contamination, but the loss of economies of scale and unaddressed static charge effects limit the technology's effectiveness. New efforts to reduce static charge generation with conductive coatings are expected to surpass the cost/performance of glass-on-die processes[2]. Sensor vendors are also working to eliminate places for contamination to lodge, through the development of gapless microlenses and non-stick inorganic coatings.

Historically, particles could be acceptably detected by visual inspection under 20x magnification. As pixels shrink to 1.75µm and beyond, visual inspection is impractical due to the throughput and quality requirements. Sensor vendors must use 100% automated inspection to monitor residual contamination after wafer washing.

In addition to surface protection technologies, manufacturing and transportation processes must avoid both surface damage and dust build up in order to minimize the particle-induced yield loss.

Reducing functional die failure rates requires the sensor suppliers to apply existing test equipment more effectively. Wafer level test patterns, algorithms, and test conditions must be aligned with the camera settings used by phone OEM. Camera manufactures and sensor suppliers need to partner to ensure settings on the phone level have been optimized for mass production.

IX. CONCLUSION

Camera modules are a complex system, involving a myriad of disciplines, technologies, and processes. Advancements in die design, pixels, image processing, calibration, test, and handling are all needed to achieve the next level of quality. Performance is limited by the weakest link, and all areas have to develop together. The sheer size of the market opportunity ensures that the required resources will be invested, making camera modules one of the most exiting products in digital imaging.

REFERENCES

[1] Ultraclean Surface Processing of Silicon Wafers: Secrets of VLSI Manufacturing, Chapter 6.3: Adhesion forces between a Wafer and a Particle, Takeshi Hattori, 1998 Springer, ISBN 3540616721

[2] Indium Tin Oxide for transparent EMC shielding and Anti-static applications, J. Eite and A. G. Spencer, Diamond Coatings Ltd., Unit 11, Lodge Forge Trading Estate, Cradley Road, Cradley Heath, West Midlands, B64 7RW, UK. www.diamondcoatings.co.uk. Presented at EMCUK 2004, Newbury, UK, 2004.

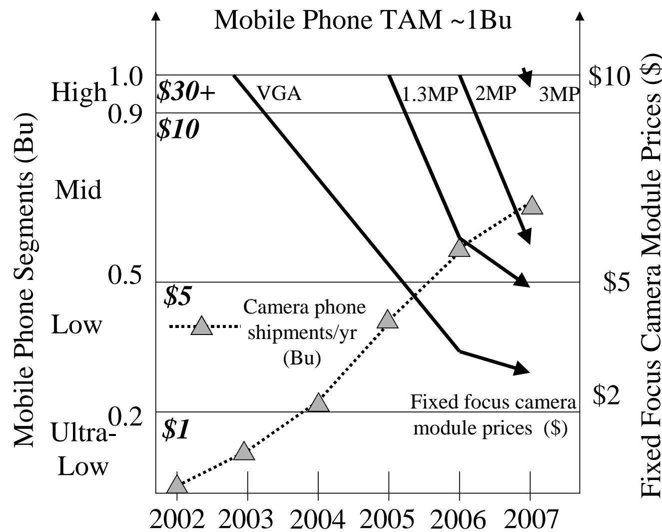


Figure 1. Camera module market size by price and segment.

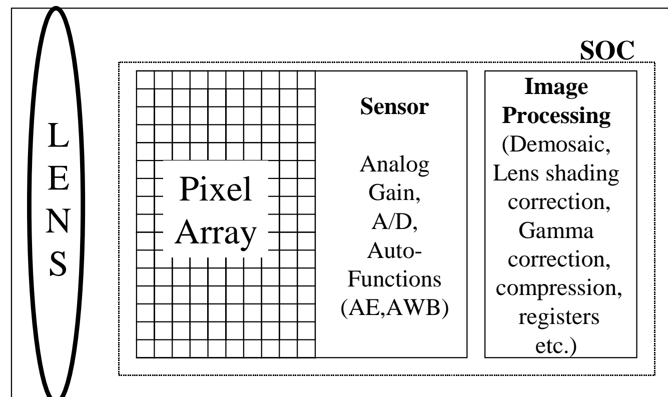


Figure 2. Fixed Focus Camera Module Block Diagram

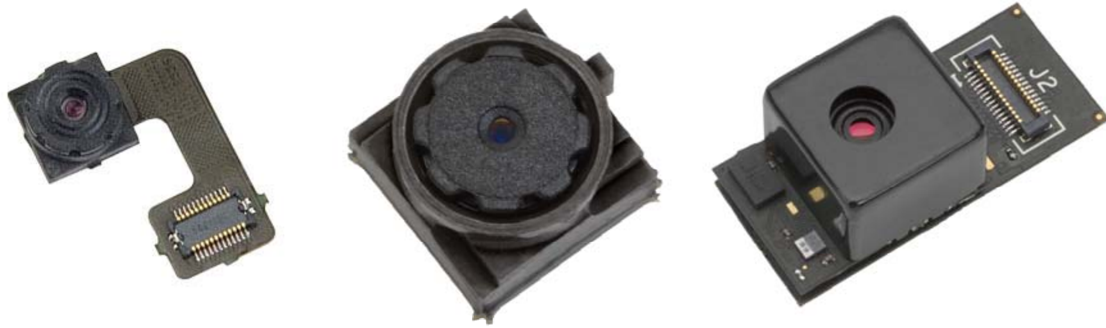


Figure 3. Examples of camera modules. Fixed-focus module with flexible PCB interconnect, left. Fixed focus socketable module, center. Autofocus camera module with calibration memory, right.

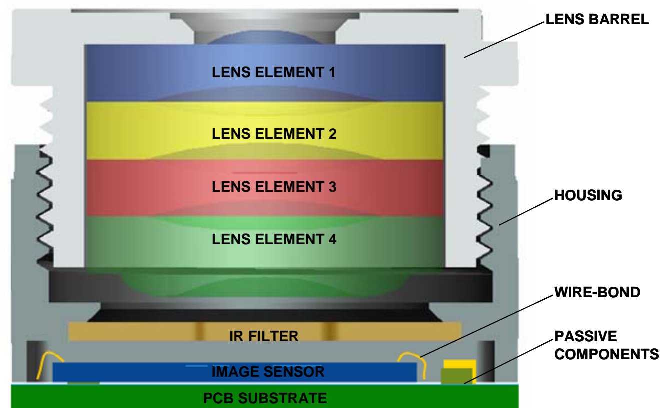


Figure 4. Cross-section of typical camera module.

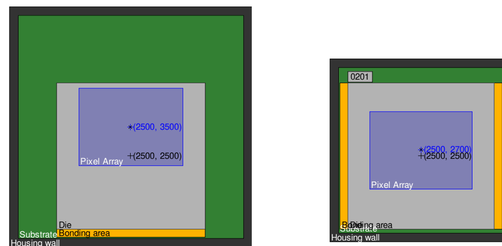


Figure 5. Effect of imager die layout on module size. Poor die layout, left. Good layout on right. Pixel array: blue, die area: gray, bonding area: orange, substrate: green, housing attach area: black. Pixel array is in the mechanical center of the module in both cases.

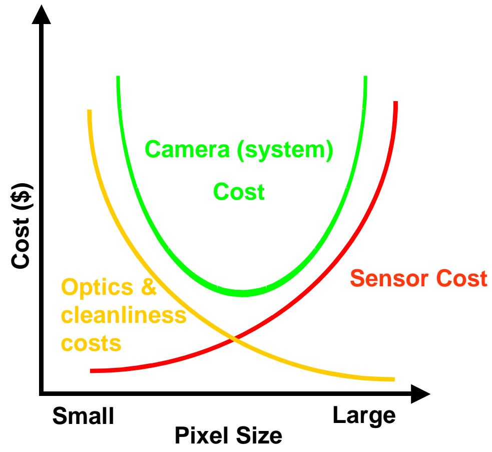


Figure 6. Camera module cost vs. pixel size

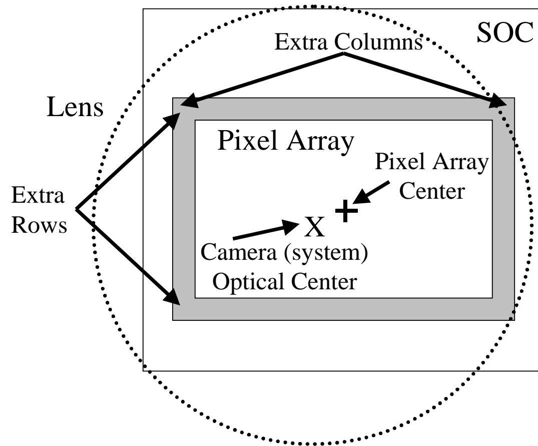


Figure 7. Camera Module (Top View) Illustrating Effect of Lens to SOC Misalignment

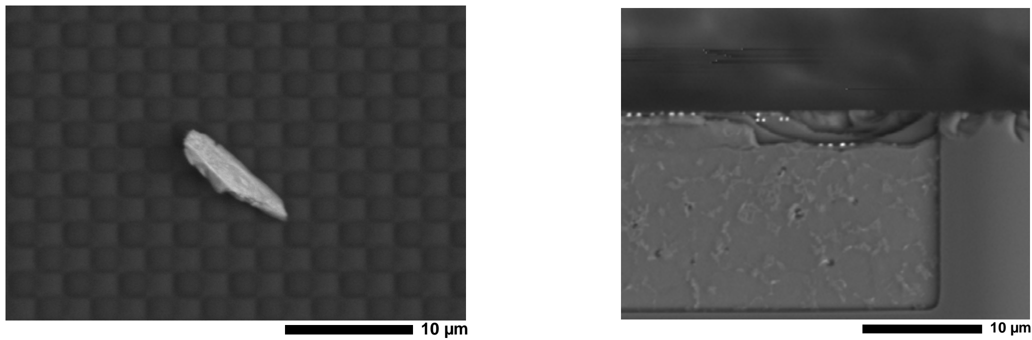


Figure 8. SEM image of particle on active pixel array after wafer washing, left. Image of saw street of die with particle, right.

Radiometric Performance Enhancement of Hybrid and Monolithic Backside Illuminated CMOS APS for Space-borne Imaging

J. Bogaerts[(1)], K. De Munck [(1)], P. De Moor [(1)], D. Sabuncuoglu Tezcan [(1)], I. Ficai Veltroni[(2)], G. Lepage[(3)], C. Van Hoof[(1)]

(1) Imec, Kapeldreef 75, 3001 Heverlee, Belgium, jan.bogaerts@imec.be
(2) Galileo Avionica, via A. Einstein 35, 50013 Campi Bisenzio (Firenze), Italy, iacopo.ficaiveltroni@galileoavionica.it
(3) Cypress Belgium, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium, fle@cypress.com

Abstract

In this paper we discuss the development of high-end CMOS detectors whose radiometric performance has been optimized for space-borne imaging. This ESA development program [1] aims to demonstrate the advantages of CMOS APS in terms of system complexity, associated size and cost, added functionality and radiation tolerance, while offering the radiometric performance of scientific CCD based instruments. The design of the detectors has been discussed at the previous edition of this workshop [2]. This paper will focus on the measured results of the most important specifications and on the newly developed technology steps for the handling and processing of the thin device wafers.

1. Introduction

The aim of this ESA program is to improve the performance of CMOS APS to achieve CCD-like performance required for hyperspectral earth and planetary observation while adding well-known CMOS advantages like on-chip functionality, low power operation, high speed and radiation tolerance. The goal of such space missions is to observe parameters encompassing agriculture, forestry, soil/geological environ-ments and coastal zones/inland waters. These data can be used to improve our understanding of geospheric processes.

Important requirements for the sensor are snapshot operation to avoid image distortion due to the satellite's movement and high frame rates, combined with large dynamic range and high quantum efficiency. Therefore, the detectors combine some newly developed technologies to achieve the radiometric and functional performance that is required for the envisaged space applications. The pixel architecture allows for correlated double sampling combined with pipelined snapshot shutter for low noise and large full well operation. This is of particular interest for hyperspectral detectors or instruments operating in "step & stare" mode which would be compatible with high resolution and large dynamic range imaging systems, even in the case of microsatellites with low performance attitude and orbit control subsystem. High resolution earth observation instruments use preferably CCD TDI devices in pushbroom mode, requiring high satellite pointing stability. The use of 2D high resolution CCD arrays would require a mechanical shutter to stop integration during frame read out. This function is implemented at the device level with CMOS APS, simplifying the system design and eliminating shutter failure risk.

2. Sensor description

The detector architecture is shown in Figure 1. The pixel pitch is 22.5 µm in both X and Y direction. The readout sensor is processed in 0.35 µm Xfab technology, the diode arrays for hybridization were processed at Imec (0.13 µm technology).

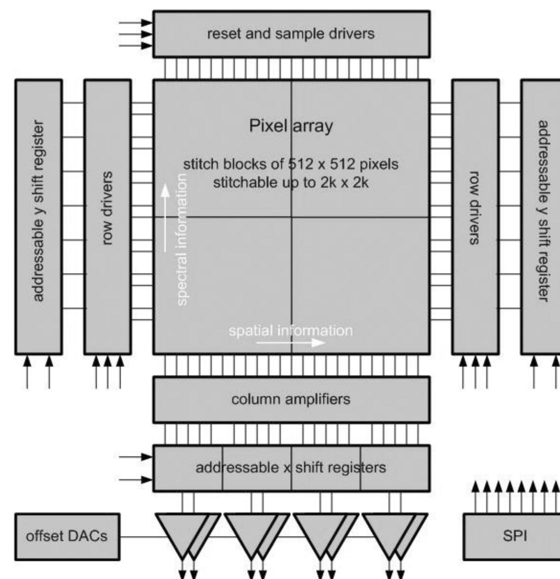


Figure 1. Sensor architecture.

Both required the stitching technique in which smaller blocks are repeated on the wafer. The pixel array consists of stitch blocks of 512 by 512 pixels and is stitchable up to 2048 by 2048 pixels. Columns are multiplexed in groups of 256 to a pseudo differential output (signal and reference output). Each output runs at a maximum readout frequency of 20 Mpixels/s.
Two types of backside-illuminated detectors are realized: either entirely monolithic or hybridized devices (Figure 2).

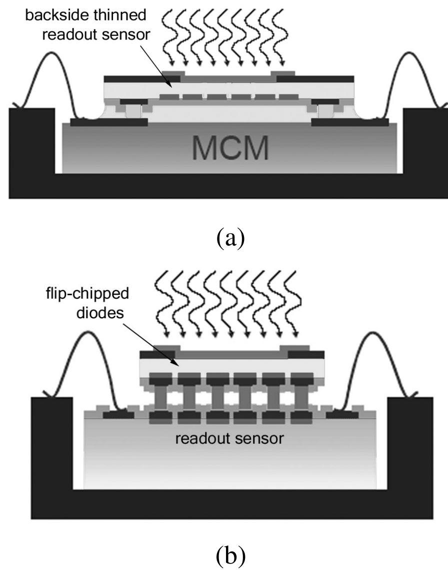


Figure 2. Monolithic backside illuminated approach (a) or hybrid sensor (b).

The pixel consists out of two stages: a light detecting stage and a sample and hold stage with three storage capacitors. This architecture, as explained in [1], allows for a true pipelined synchronous shutter with on-chip correlated double sampling (CDS), i.e. all pixels start and stop integration at the same moment while the previous frame is still read out.

The main pixel characteristics are given in Table 1. The pixel readout noise is determined by the size of the storage capacitors. The three capacitors, made by poly on diffusion, occupy about 70 % of the pixel area and equal each 350 fF. The photodiode capacitance is about 15 fF in case of the monolithic sensor and can vary from 25 fF to more than 1 pF in the hybrid approach.

Table 1. Measured sensor characteristics.

	monolithic	hybrid
in-pixel storage capacitance (fF)	350	350
full well charge (x 1000 electrons) (FWC)	> 200	> 950
conversion gain (uV/e)	6.93	1.45
dynamic range (FWC/dark noise) (dB)	75	75
maximum SNR (dB)	53	60

Both approaches have their advantages. The monolithic device requires less post-processing, leading eventually to the highest possible yield. Since its photodiode capacitance is as low as possible, it yields the best signal to noise ratio at low light levels. On the other hand, the hybrid approach allows for the highest flexibility in detector design (e.g. full well capacitance, cross talk reduction (see further)) and optimal shielding of the readout to avoid parasitic light sensitivity during readout.
Besides the normal operation mode with synchronous shutter and on-chip CDS, the sensor can also be programmed to read out the pixels non-destructively or to operate in a high dynamic range mode using a row dependent integration time [2].

3. Sensor processing

Innovative processing techniques on eight inch wafer scale have been developed and mastered which completely avoid the need for direct handling and processing of very thin (< 50 µm) wafers. All processing of thin device wafers (Figure 3) – including thinning – is performed on a temporary carrier, glued together with a temporary adhesive. The important advantage of this approach is that it allows the use of standard processing tools. Backgrinding, damage removal by dry and wet etching, implantation, laser annealing, deposition and resist patterning are all done on carrier wafer. Switching between backside and frontside processing of the thin wafers is made possible by a thin wafer transfer technique between carriers.
By means of a second adhesive, the initial wafer stack is glued to a second temporary carrier with the thin wafer facing towards the second carrier. Subsequently, the first carrier is removed, based on the different release properties of the adhesives. As a carrier, both Si and CTE matched SD2 glass have been used. Glass is used in case backside alignment with respect to the thin wafer frontside is required. CTE matching is needed to avoid thin wafer breakage on carrier while performing process steps at elevated temperature.

Fully processed thinned monolithic imagers are flip-chip bonded by means of large Au stud bumps on a redistributing MCM substrate (Figure 2). For hybridized imagers, in which the photodiode array is flip-chip integrated on the Read-Out IC, a single 10 µm diameter Indium bump per pixel is used. Both flip-chip operations have been done with and without carrier, although flip-chip without carrier is found to be more prone to die breakage. The bump interconnect yield was first assessed through daisy chain measurements and was found to be better than 99.98 %. In the final 1k x 1k hybrid demonstrators, the pixel functional yield of 99.93 % confirms these measurements.

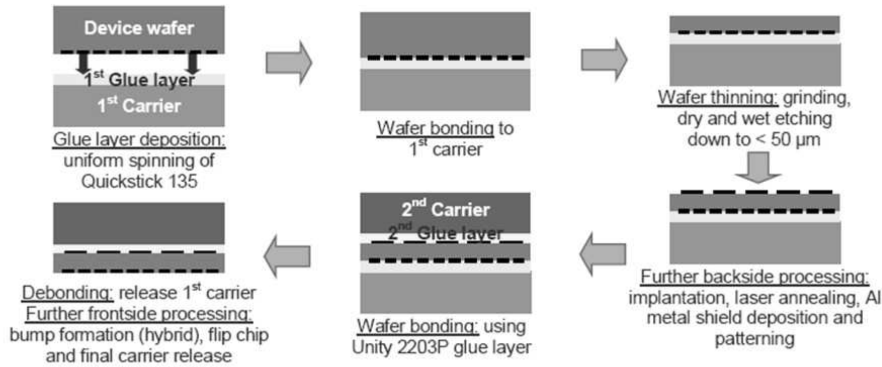


Figure 3. New thin eight inch wafer handling process flow for the fabrication of the thin imagers.

4. Measurement results

Since the readout time can be large compared to the integration time, the shutter efficiency is a key parameter. It has been measured to be virtually 100 %, certainly for the hybrid detectors where the pixel storage elements are completely shielded due to the bump interconnect.

Also the quantum efficiency is of utmost importance for the envisaged applications. The QE of the detectors has been optimized for the range of 400 to 850 nm, resulting in a final epi thickness of about 22 to 35 µm for the monolithic and hybrid devices respectively. A one-dimensional analytical model was developed to calculate the propagation and absorption of an incoming wave in the layer stack: air, anti-reflective coating (or without), the silicon epi layer and the dielectrics on the frontside. The epi layer includes a shallow boron implanted region for which it is assumed that all charges generated in this region will recombine and be lost for collection (i.e. dead layer). The surface recombination velocity at the border of this layer was empirically determined from the various QE measurements. Furthermore, the highly doped region has a sloped doping profile of about 75 nm. The backside surface field created by this implant profile is taken into account in the model, as well as the internal electric field generated by the varying epi doping profile [2]. Figure 5 shows the measurements of the QE on a 1k x 1k monolithic device without ARC. The measurements are in close agreement with the simulation where a 15 nm dead layer thickness is used (the ideal case of no dead layer is shown as reference). Recently, the following experiment has been carried out. A laser annealed device yielding good quantum efficiency over the full wavelength range, underwent an oxide plasma clean step. This process re-introduced surface damage resulting in large charge carrier recombination. The figure shows that the damage was nearly completely annealed by a single laser pulse (SP), but that a larger number of laser pulses again increases the surface damage, and consequently reduces the quantum efficiency, especially in the short wavelength range.

Reflectivity measurements of an optimized ARC, consisting of a ZnS/MgF_2 stack, have shown less than 3 % light loss in the range of interest (Figure 4). Application of this ARC on the devices as measured in Figure 5 thus gives a global QE well above 80 %.

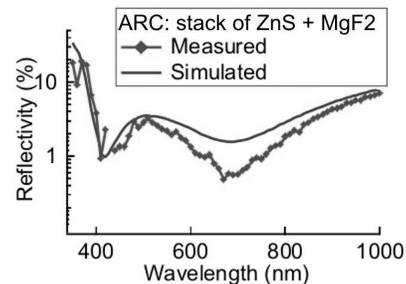


Figure 4. Optimized ARC properties. Global reflective light loss is less than 3 % over the extended optical range of interest (400-850 nm).

Typically, to optimize the epi thickness, there is a trade-off between cross talk on one hand and quantum efficiency and sensitivity (small photodiodes) on the other hand. This can be partially alleviated by using high resistivity substrates and/or large bias voltages. However, large depletion would lead to increased dark current and unwanted susceptibility to proton displacement damage. Therefore, in both the hybrid detectors and the monolithic sensors, a varying epi doping profile results in a built-in electric field that will accelerate the collection of photo-generated charges and improve the cross talk behaviour [2][3]. The dark current of a monolithic device was measured to remain below 3000 electrons/s at room temperature after subsequent irradiation by $5x10^{10}$ protons/cm^2 and 50 krad(Si) from a Co^{60} source.

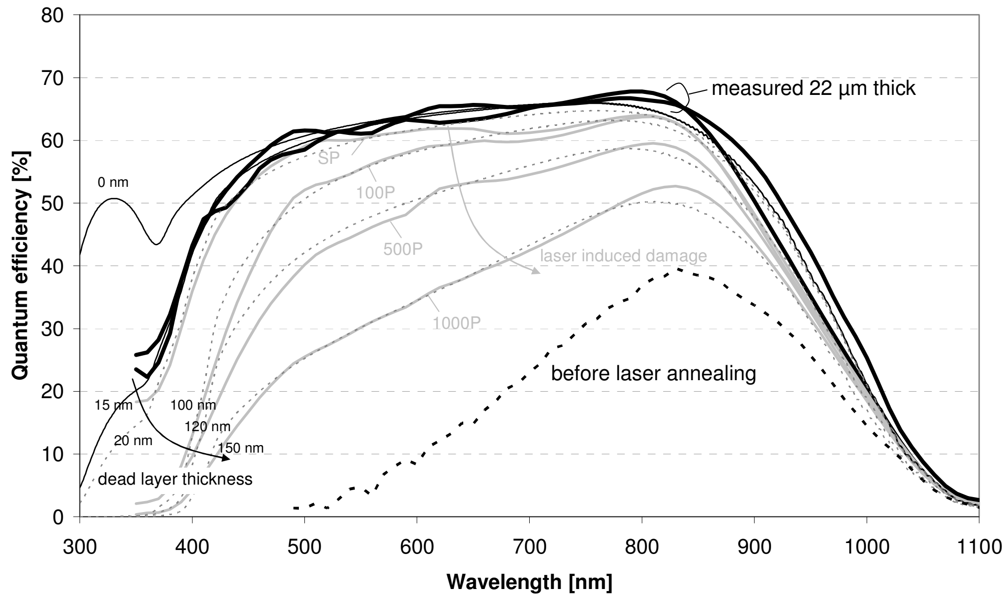


Figure 5. Measured and simulated quantum efficiency curves before and after backside treatment. A non-optimized laser anneal process will also lead to increased surface recombination.

In a hybrid detector, the cross talk due to diffusion has been eliminated completely through highly doped polysilicon filled trenches with high aspect ratio (Figure 6). These 1 µm wide 50 µm deep trenches confine the collection volume to individual pixel and enforce a lateral drift field between pixels. Quantitative measurements of the cross talk in the detectors are currently being carried out.

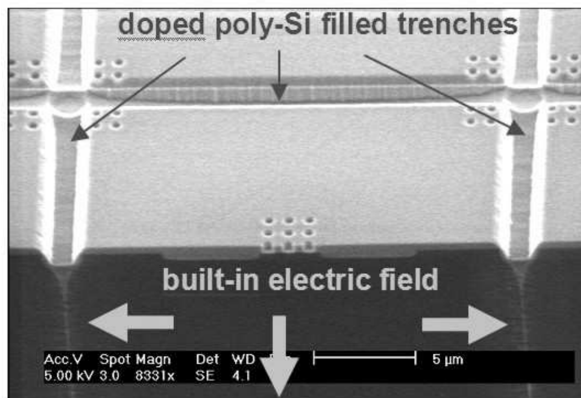


Figure 6. Top view and cross section of a single 22.5 µm pitched pixel surrounded by trenches (diodes for hybridization before metallization step).

5. Conclusions

In this paper we presented the development of a CMOS image sensor that is targeted towards space-borne imaging applications like hyperspectral imaging. The pixel is characterized by the implementation of three storage capacitors, which allow for a synchronous pipelined shutter operation, combined with CDS on-chip. The readout sensor can be used either as readout chip for hybridized diodes or as monolithic backside illuminated device. Innovative processing techniques on eight inch wafer scale have been developed to avoid any direct handling and processing of thin wafers by the use of temporary carrier wafers. This allows us to use only standard process tools. A number of techniques and performance enhancing concepts (like the use of graded epi and pixel isolating trenches) have been combined. To the authors' knowledge, the combination of this graded thick epi and cross talk reducing trenches makes these backside illuminated CMOS detectors unique.

References

[1] Radiometric Performance Enhancement of Active Pixel Sensors, ESA ITT AO/1-3970/02/NL/EC.

[2] "High-end CMOS Active Pixel Sensor for Hyperspectral Imaging", J. Bogaerts, B. Dierickx, P. De Moor, D. S. Tezcan, K. De Munck, C. Van Hoof, IEEE Workshop on CCDs and Advanced Image Sensors 2005, Japan.

[3] B. Dierickx, J. Bogaerts, "NIR-enhanced image sensor using multiple epitaxial layers", Electronic Imaging, San Jose, 21 Jan 2004; SPIE Proceedings vol. 5301, p. 204, 2004.

Back-Illuminated, Three-Dimensionally Integrated CMOS Imager with In-Pixel CDS

V. Suntharalingam†, G. Prigozhin*, R. D'Onofrio, S. Kissel*, M. Bautz*
Lincoln Laboratory, Massachusetts Institute of Technology, 244 Wood Street, Lexington, MA 02420
*Kavli Institute for Astrophysics and Space Research, Massachusetts Institute of Technology

Abstract: We present a three-dimensionally (3D) integrated CMOS photodiode imager pixel array that includes pixel-level correlated double sampling to suppress reset noise. This 256 x 256 active pixel image sensor employs a FDSOI CMOS-based readout tier vertically interconnected to silicon photodiode pixels. A wafer-scale back-illumination process is used to achieve 100% fill factor photodiodes. Device testing is underway with simulations projecting an input referred noise target of 5 electrons.

Introduction

Lincoln Laboratory has developed a wafer-scale process technology that enables the dense vertical interconnection of multiple circuit layers [1]. For image sensor applications the first circuit layer or tier is a silicon or compound semiconductor device and the second and subsequent tiers contain silicon-on-insulator (SOI)-based electronics. As shown in Figure 1, the circuit tiers are vertically interconnected through an oxide-bonded interface, and the detector tier may be thinned for 100% fill factor, back-illuminated operation. For mechanical support, an optional transparent substrate may be present, and openings may be included in the substrate for soft X-ray penetration. The combination of small wafer-to-wafer alignment tolerance (+/- 0.25 μm) and small 3D via size (1-2 μm) permits aggressively small pixels. Earlier we demonstrated a 1k x 1k CMOS visible imager [2] with 8-μm x 8-μm pixels, having a vertical interconnection at each pixel between photodiode and readout transistors. Fig. 2 shows a cross-sectional SEM through two pixels of this functional active pixel imager.

With dense vertical integration of pixel detector to associated transistors comes the significant benefit that greater area in the pixel footprint can be devoted to readout circuitry than could be accomplished in a conventional monolithic architecture. In this work we employ a simple noise suppression circuit to reduce reset noise, which can be the dominant noise source under low illumination.

Pixel Design and Operation

To implement in-pixel reset noise substration, we adapted a per-pixel "clamp" CDS circuit [3] to our 3-D SOI CMOS technology. Fig. 3 and 4 show the pixel structure and the timing diagram, respectively. The pixel consists of two reset switches (MRST1 and MRST2), two source followers (MSF1 and MSF2), a CDS capacitor (C2), and row selection transistors (M_ROW and M_ROWBAR). Reset noise reduction is accomplished by transferring the large kT/Cpd reset noise from the MRST1 reset to the much larger coupling capacitance C2.

The pixel is operated with a two-stage reset. In the first phase both MRST1 and MRST2 are held low (for p-MOS reset transistors). Integration begins when MRST1 is raised. The noise from MRST1 is transferred to C2, where it is subtracted by the capacitor. Since the initial reset noise is subtracted, the operation is a form of correlated double sampling, here occurring internal to the pixel. Finally MRST2 is raised, causing a smaller kT/C2 noise voltage to be sampled onto the capacitor.

Pixel layout for Tier-2 and Tier-1 are shown in Fig. 5 and 6, respectively. We use p-MOS reset transistors to allow complete reset of the photo-diode node, thus avoiding image lag. SOI transistor layout was driven to minimize parasitic leakage mechanisms; thus H-gate geometries and body-ties were employed where possible. A generous 24-μm square was allotted to the pixel so that we could achieve a large in-pixel coupling capacitance (780fF). Much finer pixel sizes could be realized by using conventional (non-H-gate) transistor gate geometries, smaller coupling capacitance, or by elevating the coupling capacitance to an even higher third circuit tier.

Fabrication Technology

Photodiodes and CMOS pixel electronics were fabricated in two separate 150-mm circuit wafer lots and assembled into a 3-D stack. The photodiode tier (Tier-1) consisted of p+n diodes in high-resistivity (>3000 Ω-cm, n-type) float-zone silicon substrates. The diode's lateral doping profile is graded using implant masking and thermal annealing to minimize the surface contribution to dark current. The second tier (Tier-2) is fabricated using our 0.35-μm FDSOI-CMOS process with 7.2-nm gate oxide, cobalt-silicide, and planar three-level-metal interconnect. After 3-D circuit stacking [1,2], the imager is prepared for illumination from the photodiode side; the detector tier silicon is thinned to approximately 50μm, coated with an antireflection layer, and then mounted onto a transparent support in a process sequence similar to that used to make back-illuminated CCDs [4]. Standard semiconductor equipment was used for all processing steps. An in-process view of the pixel transistors in shown in Fig. 7.

Results

Fig. 8 shows a photograph of the completed chip after processing for back illuminated operation. This test array is 256x256 pixels, each 24-μm square, with a chip footprint of roughly 6mm x 6mm. Initial testing confirms photoresponse from the array. Fig. 9 compares SPICE-based noise simulations to hand calculations for pixels with varying C2. SPICE predicts a noise target of 5-electrons rms, further dependent on other sources in the signal chain. We intend to present detailed test characterization results in June.

† vyshi@LL.mit.edu, (781) 981-7885; FAX (781) 981-7889

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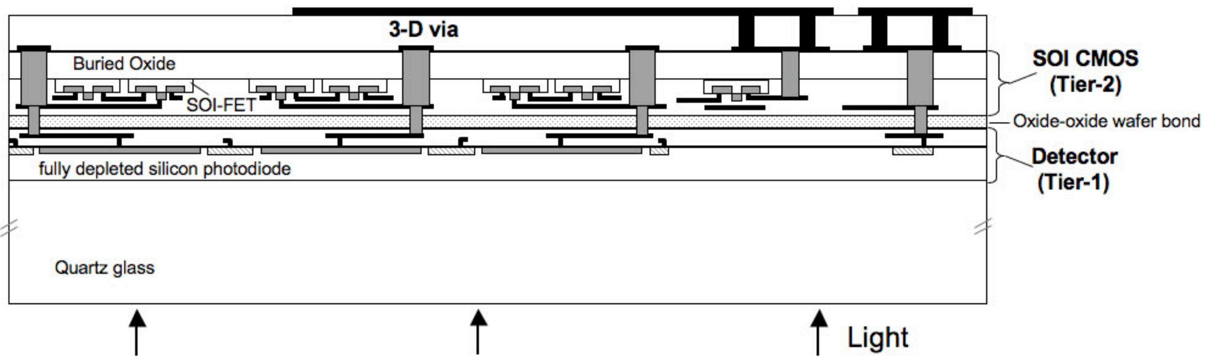

Fig. 1. Schematic diagram of 3-D stacked image sensor circuit. Tier-1 is a silicon photodetector wafer and Tier-2 is an inverted SOI-CMOS wafer.

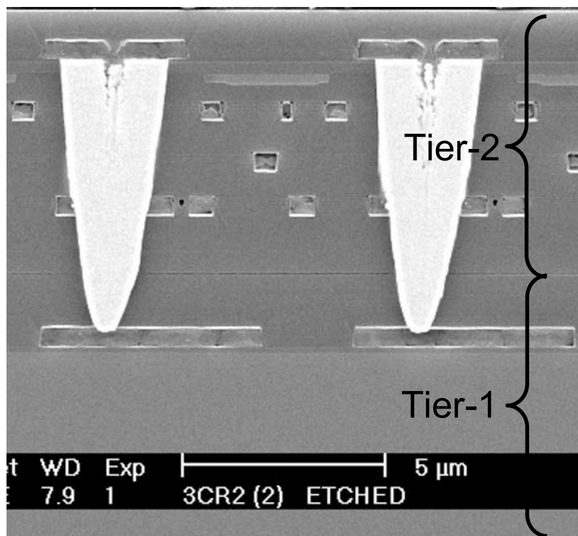

Fig. 2. Cross sectional SEM micrograph through 8-µm pixel, 3-D integrated CMOS image sensor [2]. The oxide-oxide bond between the two tiers has been decoratively etched to highlight its position.

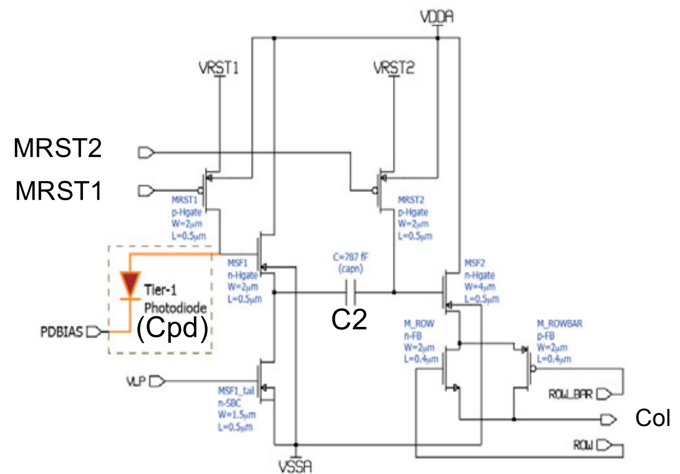

Fig. 3. Three-dimensionally integrated pixel schematic.

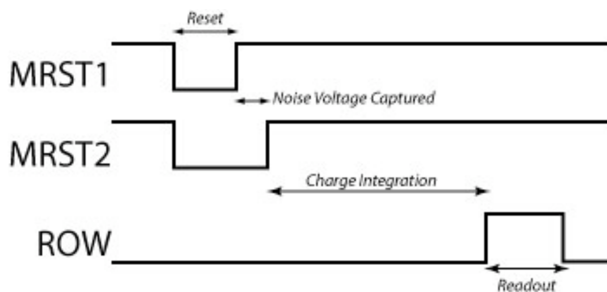

Fig. 4. Pixel timing diagram to implement reset noise reduction. (Based on [3])

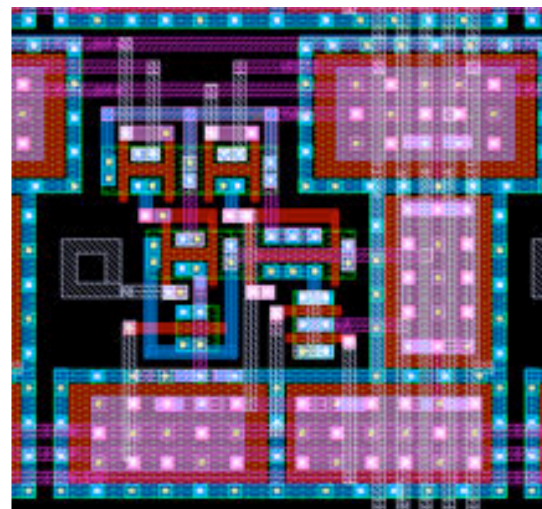

Fig. 5. Pixel Layout in Tier-2 which includes reset gates, CDS capacitor, and readout transistors. (24µm square)

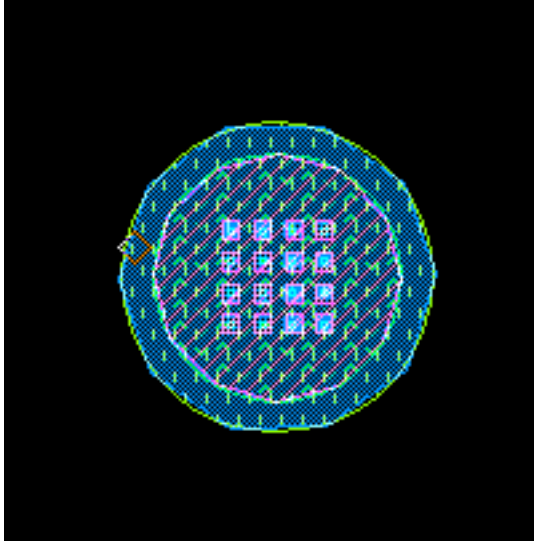
Fig. 6. Photodiode pixel layout in Tier-1 (24μm square).

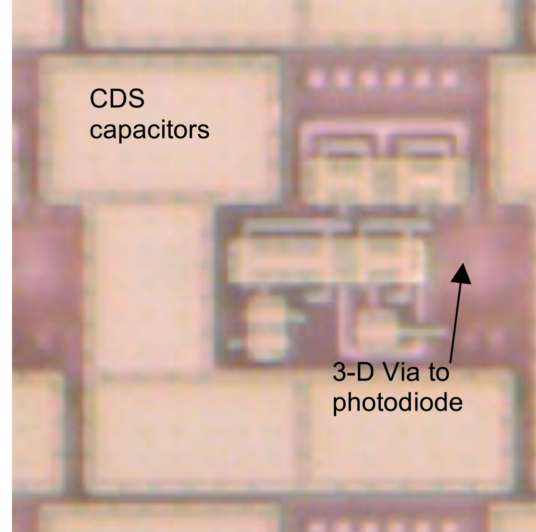

Fig. 7. In-process photomicrograph of pixel after 3-D layer transfer. The SOI-CMOS transistors are seen to be inverted, with active silicon islands now above the polysilicon gates.

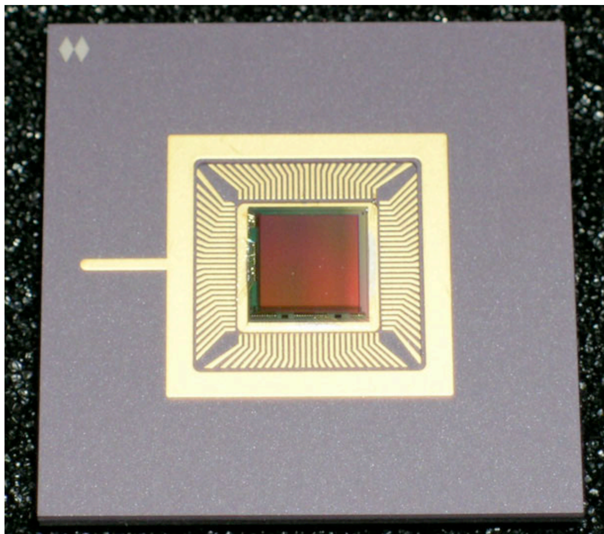
Fig. 8. Completed 256x256 pixel array after processing for back-illuminated operation.

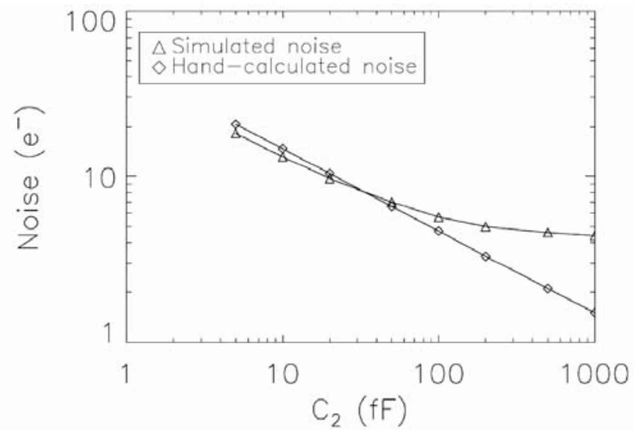

Fig. 9. Projected improvement in input referred noise – comparison between SPICE-simulations and hand calculations, after [3]. For large values of C2, hand calculations fail to capture other noise sources in the circuit.

Acknowledgment

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References

[1] J. A. Burns *et al.*, "A wafer-scale 3-D circuit integration technology," IEEE Trans. Elec. Dev., 53, Oct. 2006, pp. 2507-2516.
[2] V. Suntharalingam *et al.*, "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," 2005 IEEE International Solid-State Circuits Conference Technical Digest 48, 356-357.
[3] S. Kleinfelder *et al.*, "Novel Integrated CMOS Sensor Circuits," IEEE Trans. Nucl. Sci. 51, 2004, p. 2328.
[4] B.E. Burke, *et al.,* "Soft X-ray CCD imagers for AXAF," IEEE Trans. Electron Devices, 44, , Oct. 1997, pp. 1633-1642.

Wafer-Level Thinned Monolithic CMOS Imagers in a Bulk-CMOS Technology

Bedabrata Pain, Chao Sun, Paula Vo, Bruce Hancock, Thomas J. Cunningham,
Chris Wrigley, Risaku Toda, Victor White, Amrita Banerjee*, and Durgmadhab Misra*
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov
* Dept of Electrical & Computer Engineering, New Jersey Institute of Technology
161 Warren St, Newark, NJ 07102

As the pixel pitch of CMOS image sensors continue to shrink, there is a growing recognition of the advantages of back-illuminated image sensors [1,2], such as improved sensitivity, angular response, integration of process electronics in the pixel, and easier process integration with newer back-end-of-the-line. This paper builds on our previous work [1], and describes the design, fabrication, and test results on a monolithic 1024x1024 back-illuminated digital CMOS imager as well as on diode test structures, both fabricated on SOI silicon wafers with a built-in oxide etch-stop layer for wafer-level thinning.

In a back-illuminated image sensor, light is coupled from the side opposite to where the devices are fabricated, and after the wafer substrate has been thinned to an appropriate thickness. Despite its use in scientific image sensors, there remain a number of challenges for monolithic back-illuminated image sensor fabrication [3,4]: These include (a) accurate and uniform wafer-level thinning, (b) surface passivation following thinning, (c) wafer support during thinning, and, (d) pad opening and packaging.

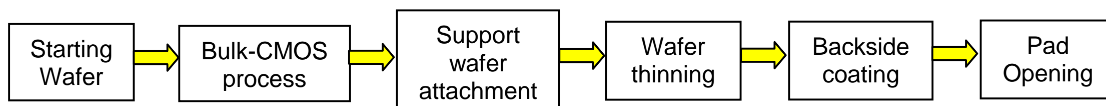

Figure 1: Schematic back-thinned imager process flow

The basic monolithic back-illuminated imager fabrication process is schematically shown in figure 1. It consists of the fabrication of a CMOS imager using an imager-compatible bulk-CMOS process on a SOI wafer. The finished wafer is attached to a second wafer for support during thinning, followed by wafer-level thinning using an oxide etch-stop. This is followed by the application of appropriate coatings on the backside of the wafer. The final step in the process is opening the pads and dicing the wafers into individual chips. The individual chip-pads are wire-bonded for electrical I/O.

Figure 2 shows the schematic cross-section of the imager wafer prior to thinning, with the substrate of the wafer facing up (the direction of optical collection). It consists of a SOI wafer as a starting material with a high-resistivity (~60 Ω-cm) p-type device layer that is 10 μm thick, and is separated from the handle wafer substrate by a 0.3 μm thermally grown high quality buried oxide (BOX) layer. The CMOS imager, designed with an 8 μm pixel-pitch, was fabricated with a 0.25 μm 4metal bulk-

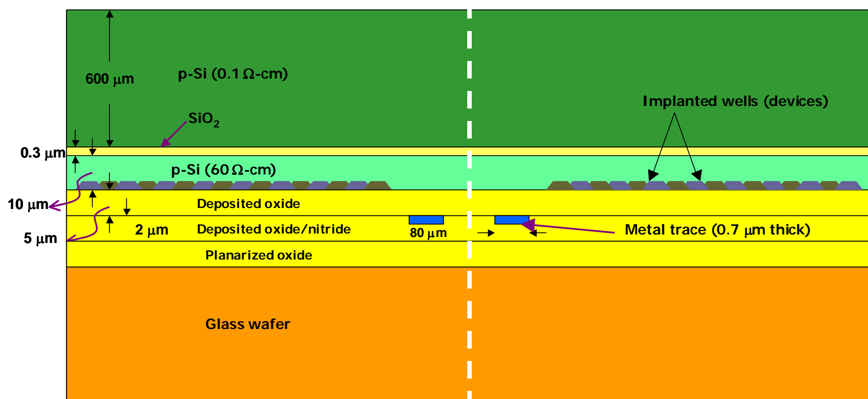

Figure 1: Schematic cross-section of the imager after glass wafer is bonded to the finished wafer (imager wafer shown upside down)

CMOS technology. The test structures were fabricated at New Jersey Inst. of Tech. 1 μm CMOS process.

The back-end-of-the-line (BEOL) consists of a 7 μm thick metal and inter-level dielectric stack, with a planarized deposited oxide being the final step. The bond-pads (indicated at metal trace in figure 1) - 80 μm wide and 0.7 μm thick - are embedded in the ILD stack. The white dashed line indicates the dicing channel separating two adjacent dies. The handle-wafer provides mechanical support during device fabrication, but is eventually etched away as part of the back-side thinning process that uses the buried oxide as an etch-stop to complete wafer-level thinning.

The finished device wafer is mounted on a glass wafer that provides mechanical support during thinning. We have used two different approaches for bonding the glass wafer – one, using a UV-cured glue and secondly, by using a room-temperature oxide-to-oxide wafer-bonding method [5]. The latter method is preferable, since it allows post-thinning anneal at 400 ^{o}C – not readily possible when adhesives are used.

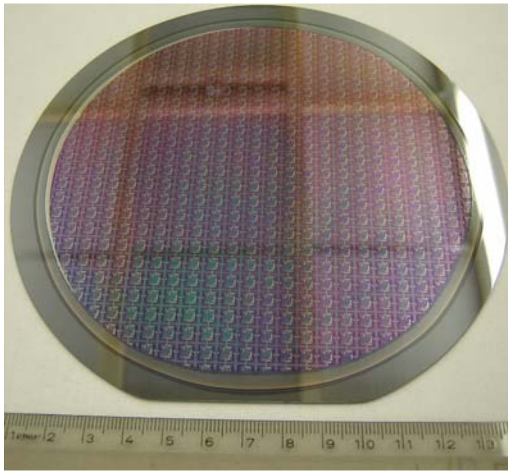

Figure 2: Picture of the room-temperature bonded wafers (device wafer can be seen through the glass wafer)

By using the room-temperature oxide-to-oxide bonding method, we successfully bonded 150 mm diameter finished device wafers consisting of planarized oxide-on-top to glass wafers with low sodium content. The glass wafer has an extremely small surface-roughness (~ 20A), and the deposited oxide is planarized using CMP < 20A measured surface roughness. Prior to room-temperature bonding, the oxides at the bonding surfaces were chemically activated [6], followed by a long duration annealing at 175°C for bond-strengthening and the elimination of voids. High-temperature annealing is ruled out, since this is being carried out post-BEOL. The bond strength even with lower temperature anneal was found to be strong enough to withstand dicing of the wafer into pieces ranging from 3mm^2 to 100 mm^2 without any delamination. Figure 2 shows picture of the bonded wafers, indicating void-free bonding across the entire wafer. The composite wafer has sufficient mechanical strength to support wafer thinning, to withstand subsequent dicing operations, and is clean enough to be taken inside annealing chamber.

Wafer-level thinning consists of etching the handle silicon wafer, using the buried oxide as an etch-stop. We have tried both wet and dry-etching methods. We have used a two-step wafer removal approach – with an initial silicon removal by lapping, wet-etching or by reactive ion etching down to ~ 100 μm thickness. Three different methods were tried for carrying out the final etch, stopping on the buried thermal oxide [7]: (i) hot KOH (50% dilution) wet etch, (ii) inductively coupled plasma RIE with SF_6, and (iii) vapor-phase dry-etching without plasma using XeF_2 gas [8]. While all the etching methods are geared for wafer-level thinning, equipment incompatibilities have forced us to carry out some of the dry-etching on smaller wafer segments. Etching with SF_6 resulted in gross thickness variations across the wafer. The etch-selectivity of SF_6 between Si and SiO_2 is ~ 70:1. Poor etch-selectivity coupled with the non-uniformities of etching resulted

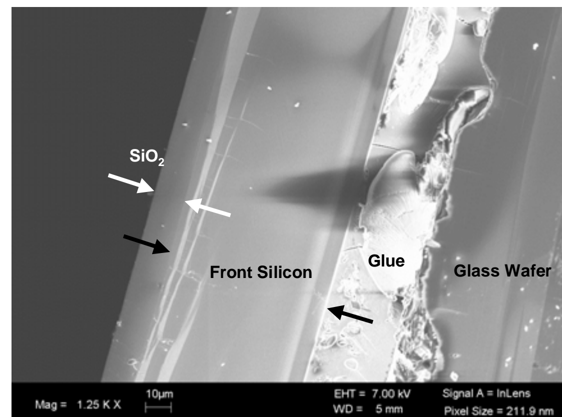

Figure 3: SEM picture of a thinned CMOS imager

in unacceptably high surface roughness, surface thickness variation over a 1 mm x 1mm area being >2000A^o. Excellent surface roughness and uniformity control was achieved both by hot-KOH etch and vapor-phase isotropic XeF_2 etch. The latter, having an etch selectivity in excess of 5000:1, produced the most uniform and planar surface, with surface roughness better than 20A (the resolution limit of the AFM probe). Figure 3 is a SEM picture of the cross-section of the imager after the handle-wafer was etched away as part of the backside thinning.

Following thinning, the chip-pads remain buried in the ILD stack under the device silicon and the exposed oxide etch-stop layer. To open the pads, we etch the silicon and SiO_2 from the back (i.e. the illuminated side) of the wafer to expose the belly of the I/O pads [9]. A small aspect ratio for etching (12 μm deep and 300 μm wide) circumvents fabrication difficulties. In addition, metal is deposited and patterned on the back of the silicon wafer both for making backside contacts and for shielding the on-chip support electronics from light. A PECVD nitride layer provides final protective layer, followed by hydrogen anneal for dark current reduction. The nitride layer provides both dark current reduction, and QE enhancement by reducing the interface-state density at the back (illumination side) side Si-SiO_2 interface, as well as by providing a level of anti-reflection coating. Figure 4 shows a picture of the pads at the intersecting corners of four dies, after pad-opening and following the application wafer protection coatings. The wafer is then sawed through the dicing channels, resulting in back-illuminated imager chips that are wire-bonded for electrical and optical tests.

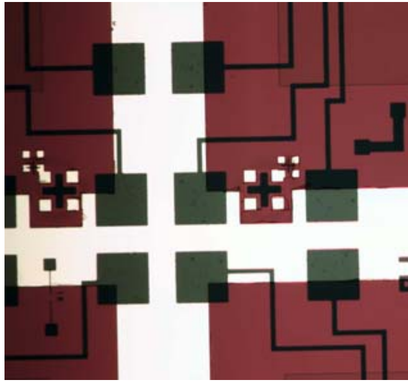

Figure 4: Picture of the wafers after pad-opening step

Figure 5 shows the schematic block-diagram of the digital megapixel CMOS imager. It consists of a pixel array with standard "3T" pixels, in-column gain stages feeding into gain-ranging a 15 bit column-parallel ADC. Careful layout and power routing was adopted to minimize fixed pattern noise (FPN) and gain non-uniformity. The "digital-imager-on-chip", consisting of bias generation circuits, and timing and control digital circuits for autonomous operation, was thinned to demonstrate back-illuminated digital imager technology. The test structures, fabricated at NJIT, consist of individual pixels arranged in a 3x3 blocks, with a readout from the center pixel. Measured data is currently available for the megapixel imager that was thinned with a glued-glass wafer as support, while more extensive backside process variations were carried out on the test structures.

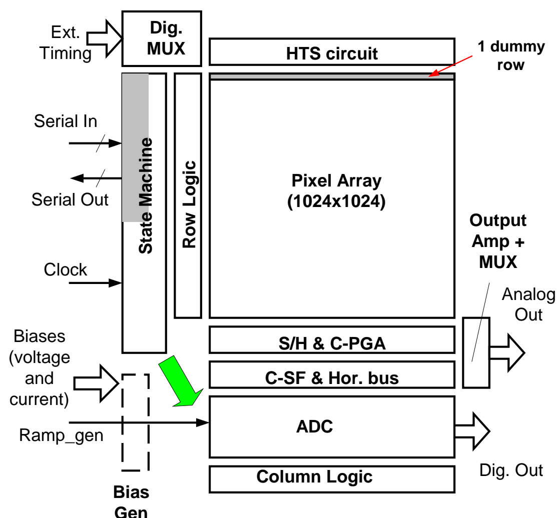

Figure 5: Schematic block diagram of the megapixel digital CMOS imager

The interface quality of the exposed surface (i.e. the light-gathering surface) is a key element of a back-illuminated imager. Additional boron was added to the device layer right under the buried oxide (BOX) during the starting wafer preparation. The purpose of the added boron layer is to hold the Si-SiO_2 interface between the buried oxide and the device silicon layer in equilibrium (providing low dark current and high blue quantum efficiency), as well as to provide a built-in electric field to suppress cross-talk by reducing lateral diffusion.

Figure 6 shows the measured dark current from the test structure for different variations of the boron content at the back-surface, presence of nitride

Boron content at the top surface	Nitride deposition	H_2 anneal	Dark Current (nA/cm^2)
None	None	None	9.1
Medium	None	None	0.8
Medium	Yes	Yes	0.16
High	Yes	Yes	0.13

Figure 6: Comparison of dark current for different top (exposed) surface conditions (from test structures)

coating on the back-side, and presence or absence of hydrogen anneal. Without the presence of boron at the exposed surface, dark current is extremely high, but is drastically reduced, even with the addition of a moderate amount of boron. By appropriately tailoring the boron concentration at the back-surface, and with the addition of PECVD nitride and H_2 anneal, the dark current can be reduced to acceptable values, typical of "3T" pixels. Thus, good interface quality can be achieved in a back-illuminated imager without requiring complex and non-traditional post-thinning processing such as flash gates, laser anneal, low-pressure oxide deposition, and MBE-based delta-doping [10-14].

Figure 7 shows the measured QE from both the megapixel imager (solid triangles) and test structures. As expected, without the presence of additional boron on the exposed surface, the blue QE is very low, but the green and longer wavelength QE is hardly affected. The blue QE increases almost by a factor of 2 with the increasing boron content. With a multi-layer AR coating, the QE is increased to near 85%. Measured results match quite well with published QE models [15,16]. Further increase in QE is possible with further optimizations in AR coating. Measured PRNU of the back-illuminated megapixel imager is the same as that in the front-illuminated case, and is only 1.4%. Both full well (80,000 e^-) and the read noise (< 7 e^-) with off-chip CDS are independent of operation in the front or back-illuminated mode. The results are strongly suggestive of the maturing of the process technology for implementing high-performance back-illuminated CMOS imagers.

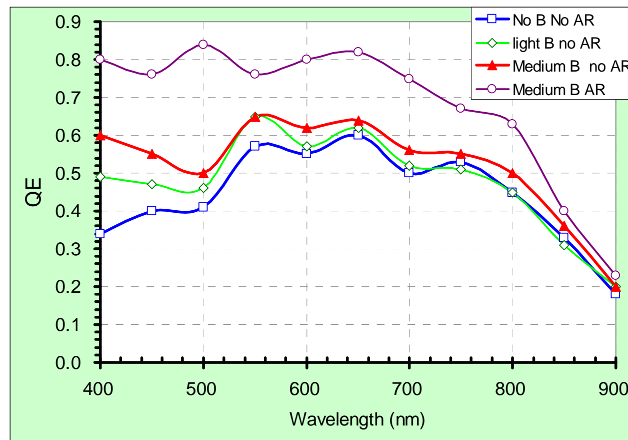

Figure 7: Measured QE for different exposed surface conditions

Acknowledgments:

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References:

1. B. Pain, *2005 IEEE Workshop CCD/AIS,* 2005.
2. S. Iwabuchi et al., *IEEE Intl. Solid-State Circuits Conference,* vol. 49, pp. 302-303, 2006.
3. R. Winzenread, *Proc. SPIE*, vol. 2198, pp. 886-894, 1994.
4. M. Lesser, *Proc. SPIE,* vol. 1447, pp. 177-183, 1991.
5. J.A. Burns et al., *IEEE Trans. Electron Devices*, vol. 53, pp. 2507-2516, 2006.
6. Q.Y.Tong and U. Gosele, in *Semiconductor Wafer Bonding*, The Electrochemical Society Press, pp. 62, 1999.
7. M.J. Madou in *Fundamentals of Microfabrication*, CRC Press, pp. 104-110, 206-211, 2002.
8. F.I. Chang et al., *Proc. SPIE*, vol. 2641, pp. 117-126, 2007.
9. K.W. Gladhill, *Proc. SPIE*, vol. 1656, pp. 585-598, 1992.
10. M. Lesser, *Proc. SPIE,* vol. 2198, pp. 782-791, 1994.
11. J. Janesick et al., *Proc. SPIE,* vol. 982, pp. 543-582, 1986.
12. R.A. Stern et al., *Proc. SPIE,* vol. 1071, pp. 43-57, 1989.
13. J.R. Tower et al., *IEEE Trans. Electron Devices,* vol. 50, pp. 218-224, 2003.
14. S. Nikzad et al., *Proc. of SPIE*, vol. 2198, pp. 907, 1994
15. C.M. Huang et al. *Proc. SPIE,* vol. 1447, pp. 156-164, 1991.
16. M. Blouke et al., *Proc. SPIE*, vol.1447, pp. 142-155, 1991.

Color filter array with sparse color sampling crosses for mobile phone image sensors

Gang Luo
luogang68@yahoo.com

Abstract

In order to solve the conflict between the size constraints of mobile phone cameras and image quality, it is an effective approach to improve the light sensitivity of imaging sensors. A color filter array comprising sparsely distributed crosses of color sampling blocks is proposed, in which nearly 69% of elements are transparent ones that detect luminance directly with a higher sensitivity than the remaining color-filtered ones. Monochromatic images resulted from the majority white pixels are of high spatial resolution and of low noise. They are used along with the sparse color samplings to generate color images. An advantage of the color sampling crosses is that monochromatic images can be estimated with less error, which is critical for the successive calculation of color images. Experiments have been conducted using a Canon 30D camera under normal and low light levels. Results showed that the color filter array could greatly reduce image noise that usually occurs with the conventional Bayer pattern under low light levels, and did not cause noticeable color artifacts that would normally occur with under-sampling of chrominance.

Introduction

Phone cameras are much more readily to use than standalone digital cameras. As mobile phones are becoming smaller and thinner, the size constraints of mobile phones put forward a request of small image sensors. At the same time, consumers are continuously pursuing higher image quality. It is a well-known fact that the reduction in sensor size causes a reduction in light sensitivity, and therefore may cause a reduction in image quality if compensating illumination is not provided, for example, by flashlights. However, when phone cameras are used as video cameras, using flashlight usually is not a possible option. In addition, market surveys show that mobile phone cameras are frequently needed under low light levels. In order to solve the conflict between sensor size and image quality, to improve the light sensitivity of sensors is an effective approach.

Comparing with a black-and-white camera, a color camera using the same image sensor and a RGB color filter array (CFA) has only 1/10 of the ISO speed of the black-and-white one [1]. Some Cyan-Magenta-Yellow CFAs and RGB CFAs with white pixels have been proposed in an attempt to increase light energy reaching image sensors [2, 3]. However, the CMY CFAs usually have color artifact problems, and those CFAs with white pixels usually provide limited improvements because of low rates of white pixels (<50%). A fundamental problem in these CFAs is that luminance and chrominance is not really separated. Hence, improvements in one generally cause losses in another. A novel imaging paradigm with majority pixels being white ones and the remaining pixels being sparsely distributed color filtered ones has been proposed by the author [4], in which white pixels generate luminance information and RGB color pixels provide pure chrominance information. Luminance and chrominance are integrated in Lab color space. Because luminance and chrominance can be separated well in sampling and processing stages, the rate of white pixels can be designed to be over 50%.

In the novel paradigm, luminance is very important because it determines the resolution of output color images. Luminance can also provide useful information for chrominance calculation as there is a strong correlation between luminance and chrominance for natural images. Therefore, it is critical to make a good estimation of luminance. A CFA comprising sparse color sampling crosses is proposed in this paper, with which good estimation of luminance can be likely.

Sparse color sampling crosses and image formation

Figure 1 shows the CFA comprising cross-shaped color sampling blocks. Each 3x3 sampling cross consists of a blue element at the center, two green elements at top and bottom respectively, and two red elements at left and right respectively. Such crosses repeat every four pixels horizontally and vertically, and the remaining elements are transparent (white elements) for direct luminance detection. The overall color sampling rate is about 31%, and luminance sampling rate is nearly 69%.

	G				G		
R	B	R		R	B	R	
	G				G		
	G				G		
R	B	R		R	B	R	
	G				G		

Figure 1. A color filter array comprising sparse color sampling crosses. Blank cells represent for transparent elements

Monochromatic images are first calculated from white pixels by means of directional interpolation based on edge information. For the center pixel of each cross block, edge is evaluated in four directions – horizontal, vertical and 2 oblique directions (Figure 2):

Horizontal: $E_h=1/[1+\text{mean}(|w2-w3|, |w4-w5|, |w6-w7|)]$
Vertical: $E_v=1/[1+\text{mean}(|w2-w6|, |w1-w8|, |w3-w7|)]$
NE oblique: $E_e=1/[1+|w3-w6|]$
NW oblique: $E_w=1/[1+|w2-w7|]$ (1)

		W1		
	W2		W3	
W4		W_c		W5
	W6		W7	
		W8		

Figure 2. Interpolation of luminance values at color sampling pixels. The center pixel W_c is first estimated, and then four tips of the sampling cross.

For the center pixel of a sampling cross, the luminance value can be interpolated possibly along four directions:

Horizontal: $I_h=(w4+w5)/2$
Vertical: $I_v=(w1+w8)/2$
NE oblique: $I_e=(w3+w6)/2$
NW oblique: $I_w=(w2+w7)/2$ (2)

The edge-weighted average of interpolation of the center pixel is:

$$W_c=(I_h*E_h+I_v*E_v+I_e*E_e+I_w*E_w)/(E_h+E_v+E_e+E_w) \quad (3)$$

Once the luminance value of the center pixel is estimated, pixel values of the four tips of a cross can then be estimated based on W1…W8 and Wc using a similar interpolation approach.

It is a reasonable and effective assumption that for natural images gray scale version and RGB versions have very similar profile. This assumption has been used in some demosaic algorithms [5, 6]. In this paper, it is assumed:

$$I(x)-kH(x)\approx c \quad (4)$$

where *I(x)* represents luminance image, *H(x)* represents either of RGB components, and *k* and *c* are constants (see Figure 3). Parameters *k* and *c* can be resolved from two pixels whose *I(x)* and *H(x)* are known. Pixels of sampling crosses can be those pixels after full frames of luminance images are calculated. RGB images can be calculated using following equation:

$$H(x) \approx \frac{I(x) - c}{k} \tag{5}$$

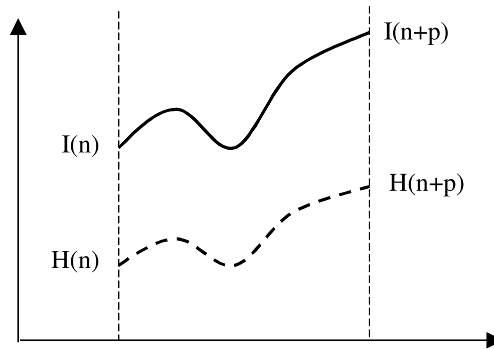

Figure 3. Estimation of color components *H(x)* based on luminance component *I(x)*. It is assumed gray scale images have similar profiles as RGB components.

To form output color images, color images estimated using equation (5) are low-pass filtered, transformed into Lab color space, and the luminance component (L) is replaced with the monochromatic images [4].

Experimental results

A simulation experiment using the proposed CFA was conducted. Tested images were captured using a Canon 30D camera equipped with a Sigma lens (18-50mm f/2.8 EX DC). The results are shown in Figure 4 and Figure 5. They are cropped to show details clearly.

Figure 4a is an underexposed picture using 6% of correct exposure level (F10, 1/1600 sec, ISO100). Bayer pattern and an adaptive homogeneity-directed demosaic algorithm [5] were used to generated the image from raw image data. As can be seen, there is severe image noise due to under-exposure in the picture. A sampled image as specified as in Figure 1 was constructed from the underexposed image as shown in Figure 4a and a correctly exposed image (F10, 1/100 sec, ISO100) – the underexposed image contributed the color filtered pixels and the correctly exposed image contributed the white pixels. Figure 4b shows the demosaiced image from the sampled image. As can be seen, image noise has been greatly reduced.

Figure 4. A simulation experimental result under a low light level. Size: 280x201 pixels. (a) A picture captured using 6% of correct exposure. Bayer CFA was used. (b) The proposed CFA was used. Chrominance is from (a) and luminance is from a correct exposure. Chrominance and luminance were combined in Lab space.

Figure 5. An experimental result under sufficient light level. The proposed CFA was used. Size: 651x371 pixels.

Figure 5 shows another picture captured under a correct exposure level. The proposed CFA was used. It can be seen that the image quality is satisfactory, and color artifacts are barely noticeable even for the fine check pattern of the shirt and the busy pattern of hay.

Conclusion

The proposed novel CFA has promising values in making small image sensors. The majority white pixels will enable mobile phone cameras to capture quality images under low light levels and sufficient light levels.

References

1. R. Baer et al, "Comparison of primary and complementary color filters for CCD-based digital photography", Proceedings of SPIE V3650, *Sensors, Cameras, and Applications for Digital Photography*; pp. 16-25, 1999
2. J. Bean, "Cyan-magenta-yellow-blue color filter array", US Patent 6628331B1, 2003.
3. T. Yamagami, et al, "Image signal processing apparatus having a color filter with offset luminance filter elements", US Patent 5323233, 1994.
4. G. Luo, "A novel color filter array with 75% transparent elements", Proceedings of SPIE V6502, *Digital Photography III*, 65020T, 2007.
5. K. Hirakawa, T.W. Parks, "Adaptive homogeneity-directed demosaicing algorithm", IEEE Transactions on Image Processing, 14(3), pp. 360-369, 2005.
6. J.W. Glotzbach, R.W. Schafer, and K. Illgner, "A method of color filter array interpolation with alias cancellation properties," in Proc. Int. Conf. Image Processing, vol. 1, Oct. 2001, pp. 141–144.

Crosstalk, color tint and shading correction for small pixel size image sensor

Samsung Electronics Co., LTD., NongSeo-Dong, Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea 446-711

Alexander Getman, Timofei Uvarov, YongIn Han, Bumsuk Kim, JungChak Ahn, YongHee Lee.

Keywords: CMOS image sensor, crosstalk, shading, spectral response, image uniformity, Bayer color filter array (CFA), Gr/Gb disparity.

Abstract

Current trend to reduce pixel size of portable camera modules brings a set of new problems for image sensor designers. The benchmarking shows that most of the portable camera modules are suffering from strong shading and unstable color reproducibility caused by spatial variation of the crosstalk between pixels [1]. This appears as a non uniform color tint on captured images and makes shading profile susceptible to spectral composition of illuminant light. While standard methods based on spatially dependent gain control are sufficiently effective for shading correction (SC) of sensors with large pixel size a more advanced technique is needed to cure crosstalk induced problems of state-of-the-art imager.

The purpose of current study is to construct robust model describing shading, color tinting and crosstalk mechanisms affecting image quality and apply the model for image correction.

The Crosstalk Model

The crosstalk in image sensor is an effect when signal from specific pixel is affected by that of adjacent pixels. The nature of the crosstalk in image sensors has various origins: electron diffusion in photo diode, not sufficient optical separation of pixels or even readout circuit [2,3]. It is natural to assume that image sensor is a linear system, with linear crosstalk existing only between horizontal and vertical neighboring pixels (closest neighbor approximation) and that it is small in comparison with the main signal, Fig. 1. Under this assumption we can use (1) for crosstalk correction:

$$X^* = C_{X,X} \cdot X + C_{L,X} \cdot Left + C_{R,X} \cdot Right + C_{T,X} \cdot Top + C_{B,X} \cdot Bottom \quad (1)$$

In equation (1) asterisk is used for signal in the absence of the crosstalk, we will call it pure or target signal. The constants $C^*_{i,X}$, *i= L,R, T,B* are responsible for crosstalk and $C^*_{X,X}$ is signal gain constant which in general is not unity. If we know parameters $C_{i,X}$, *{i=X, L, R, T, B}*, it is possible to estimate crosstalk-free signal.

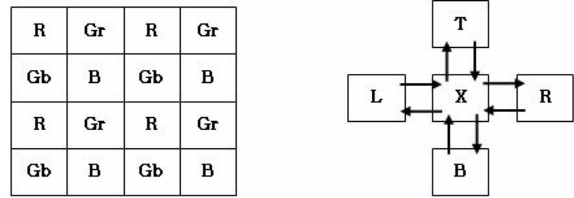

Fig.1 Bayer pattern of color filters and crosstalk interactions between adjacent pixels.

Crosstalk and gain parameters $C_{i,X}$ can be measured experimentally for a given type of the sensor. Unfortunately, it is difficult to distinguish left and right (top and bottom) crosstalk components. So, we may simplify (1) assuming these components are equal.

It is also important to take into account, that crosstalk (and gain) constants are sensitive to spectral composition of light. It is well known [1, 2], that crosstalk for red light is higher than that for blue because of different absorption rate of light in silicon. In case of color image sensor with Bayer color filter pattern we can take this effect into account introducing different crosstalk coefficients for each color channel. Eq. (1) now can be rewritten as:

$$\begin{aligned}
R^* &= C_{R,R} \cdot R + C_{G,R} \cdot \frac{Gr_L + Gr_R + Gb_T + Gb_B}{4}, \text{ for Red pixel} \\
Gr^* &= C_{R,Gr} \cdot \frac{R_L + R_R}{2} + C_{Gr,Gr} \cdot Gr + C_{B,Gr} \cdot \frac{B_T + B_B}{2}, \text{ for Gr pixel} \\
Gb^* &= C_{R,Gb} \cdot \frac{R_T + R_B}{2} + C_{Gb,Gb} \cdot Gr + C_{B,Gb} \cdot \frac{B_L + B_R}{2}, \text{ for Gb pixel} \\
B^* &= C_{G,R} \cdot \frac{Gr_L + Gr_R + Gb_T + Gb_B}{4} + C_{B,B} \cdot B, \text{ for Blue pixel}
\end{aligned} \quad (2)$$

The equation (2) is depending upon 10 different parameters. We have to use one of four equations depending upon the type of pixel to be corrected.

The structure of Eq.(2) is a composition of classical shading correction (CSC), when we apply

position dependent signal gain and crosstalk part, which is responsible for signal mixing and is also position dependent. Thus we may refer to the method, based on (2) as a Generalized Shading Correction (GSC)

Eq.2 is the final equation and will be used in the crosstalk correction algorithm.

Crosstalk Parameters Estimation

If we will capture uniformly illuminated image of uniform object (for example white paper) we should expect, that all pixels of resultant image have the same color components (R_0, G_0, B_0). In reality, we may found that the image will have brighter center (effect known as shading), color tinted regions and, probably, regular mosaic due to difference between *Gr* and *Gb* channel sensitivities. Under assumptions made in previous chapter, we can describe these effects in terms of crosstalk model characterized by distribution of 10 coefficients in (2) according to pixel position. In case of uniform object difference between neighboring pixels of the same color channel is negligible and we may simplify equation (2):

$$\begin{bmatrix} R \\ Gr \\ Gb \\ B \end{bmatrix}_{Target} = \begin{bmatrix} C_{R,R} & C_{G,R} & C_{G,R} & 0 \\ C_{R,Gr} & C_{Gr,Gr} & 0 & C_{B,Gr} \\ C_{R,Gb} & 0 & C_{Gb,Gb} & C_{B,Gb} \\ 0 & C_{G,B} & C_{G,B} & C_{B,B} \end{bmatrix} \times \begin{bmatrix} R \\ Gr \\ Gb \\ B \end{bmatrix}_{(i,j)} \quad (3)$$

In this equation *R*, *Gr*, *Gb* and *B* are the components of the Bayer cell containing pixel with coordinates *(i, j)* and target signal is expected value of *R*, *Gr*, *Gb* and *B* if there were no crosstalk. Equation (3) is equivalent to 4 linear-independent equations for 10 variables and can be solved only if we have calibration images captured for $k \geq 3$ different illuminants or colors. In this case equation (3) can be rewritten as an over determined system of linear equations:

$$\begin{bmatrix} R_1 & R_2 & \dots & R_k \\ Gr_1 & Gr_2 & \dots & Gr_k \\ Gb_1 & Gb_2 & \dots & Gb_k \\ B_1 & B_2 & \dots & B_k \end{bmatrix}_{Target} = \begin{bmatrix} C_{R,R} & C_{G,R} & C_{G,R} & 0 \\ C_{R,Gr} & C_{Gr,Gr} & 0 & C_{B,Gr} \\ C_{R,Gb} & 0 & C_{Gb,Gb} & C_{B,Gb} \\ 0 & C_{G,B} & C_{G,B} & C_{B,B} \end{bmatrix} \times \begin{bmatrix} R_1 & R_2 & \dots & R_k \\ Gr_1 & Gr_2 & \dots & Gr_k \\ Gb_1 & Gb_2 & \dots & Gb_k \\ B_1 & B_2 & \dots & B_k \end{bmatrix}_{(i,j)} \quad (4)$$

To complete Eq. (4) we should determine the procedure of evaluation of target signal. To do this in a best way we must understand structure of the sensor and mechanisms of crosstalk.

A typical structure of image sensor is represented on Fig.2. We are assuming that image sensor is made using circuit sharing technology and position dependent microlens and color filter optimization to compensate shading.

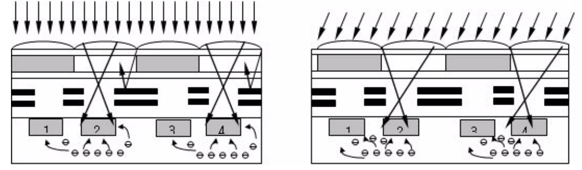

Fig.2 a schematic structure of image sensor and crosstalk behavior at the center (left) and edge (right) region of the image sensor.

A sensor from Fig.2 has several mechanisms of crosstalk. First, electrons generated in depletion region of pixels photodiode can diffuse to the adjacent photodiodes. This effect is known as electrical crosstalk which depends upon the wavelength and incident angle of light. Since it is position dependent it causes non uniform color tinting of captured image. If a circuit sharing technology is applied, adjacent pixel will have different geometry of back-end structure (pixels 1 and 2 on Fig.2). This, in turn, will result in modulation of sensitivity and crosstalk which is the origin of fixed pattern noise. The magnitude of this modulation is also a function of light incident angle and position of the pixel.

A microlens and color filter optimization technology is dedicated to minimize color tinting and shading by adjusting position of microlenses, color filter and metal layers to match specification of camera lens. Normally, at the center of the sensor the photodiode, color filter, microlens and imaging lens are aligned along common optical axis, but this is not true for the edge of the pixels array. It is because of this property, central region has higher sensitivity, best color reproduction and smallest crosstalk.

We may put these considerations into target signal estimation to set

$$\begin{bmatrix} R \\ Gr \\ Gb \\ B \end{bmatrix}_{Target} \equiv \begin{bmatrix} R \\ (Gr+Gb)/2 \\ (Gr+Gb)/2 \\ B \end{bmatrix}_{Center} \quad (5)$$

We intentionally average *Gr* and *Gb* channels to eliminate *Gr/Gb* difference in target signal. Now we may solve (4) for each pixel of the sensor using either pseudo inverse matrix or numerical methods to determine $C_{i,j}$, *i,j={R, Gr ,Gb, B}*

Now we may ask what set of images is the best for $C_{i,j}$ estimation. Well, this is closely related to the variation of the object colors and light conditions of scenes to be captured. It may be patches of Gretag Macbeth color checker table or colored paper, but the best results we may achieve by capturing interior of integrating sphere illuminated by monochromatic light. According to our experience, this experimental

configuration offers highly uniform images of 'pure' color and possibility to automate the calibration procedure.

Each of 10 elements of matrix in (4) can be characterized by a surface defined on image area. On the basis of analysis of experimentally measured crosstalk parameters distribution, we have decided to approximate it by polynomial function of two variables:

$$S(x,y) = \begin{bmatrix} 1 & y & \dots & y^n \end{bmatrix} \begin{bmatrix} s_{11} & s_{12} & \dots & s_{1,m+1} \\ s_{21} & s_{22} & \dots & s_{2,m+1} \\ \vdots & \vdots & \ddots & \vdots \\ s_{n+1,1} & s_{n+1,2} & \dots & s_{n+1,m+1} \end{bmatrix} \begin{bmatrix} 1 \\ x \\ \vdots \\ x^m \end{bmatrix} \quad (6)$$

$$x = i / HorSize, \; 0 \le x \le 1$$
$$y = j / VertSize, \; 0 \le y \le 1$$

In (6) we assume that pixel array resolution is *HorSize* by *VertSize* pixels. According to (6), the crosstalk distribution surface may be described by $(m+1)\cdot(n+1)$ constants. In our case we were using m=4 and n=4, so our method requires 250 parameters. We have managed to further reduce number of parameters by zeroing nonsignificant components. We do not present here detailed discussion of this optimization to concentrate our attention on crosstalk related effects.

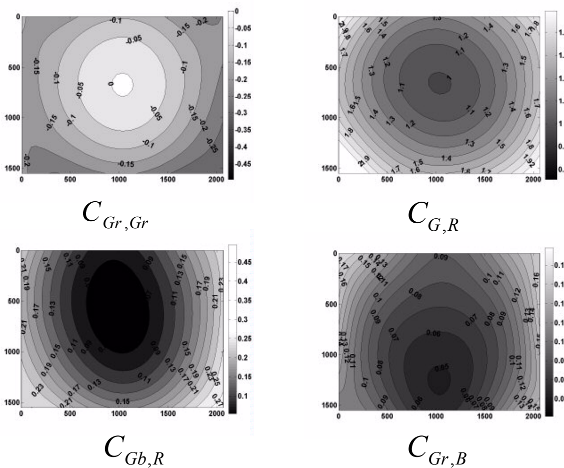

Fig.3 Example of spatial distribution of crosstalk parameters

A spatial distribution of some constants after approximation with (6) is presented on Fig. 3. We may notice that centers of symmetry of the distributions do not coincide with each other. Parameter $C_{Gr,Gr}$ is a diagonal member of matrix in (5) thus responsible for shading correction. A typical magnitude of non-diagonal elements may reach as high as 0.2~0.3 or more than 10% of corresponding diagonal element. This is well noticeable as color tint on captured images if we will keep using the classical shading correction.

The capabilities of the method can be illustrated by means of spectral response (Fig.4). These graphs show relative sensitivity to a monochromatic light for each color channel in selected region of pixel array. In case when sensor operates in linear regime, spectral response provides us full information about color reproduction.

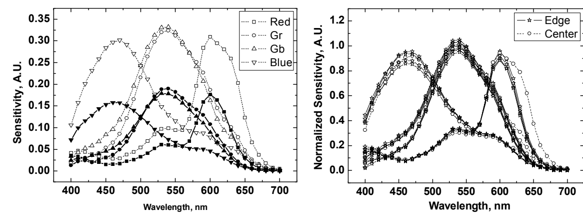

Fig.4 Spectral response and sensitivity comparison for preprocessed images. On the left graph sensitivity comparison between center (dashed line) and bottom right corner (solid line) is shown. On the right graph data from all 4 corners and the center of the sensor is normalized to the maximum of (Gr+Gb)/2 to show spectral response variation.

On Fig.4 spectral responses of central and edge regions of image sensor are compared. We may see that sensitivity of the central region is much higher than that of the edge. Even if we will apply normalization, difference between *Gr* and *Gb* channels as well as variation of spectral responses (Fig.4, Right) will remain. We may notice a strong difference between center and edge for red color channel response. This discrepancy occurs due to infrared (IR) cut-off filter. In our camera modules we are using interference-type IR filter so cut-off wavelength depends upon light incident angle.

We measure spectral response by capturing interior of integrating sphere illuminated by monochromatic light (400 to 700nm). Extracted from the images color channel signals are normalized to optical power and presented as a graph. If we apply our correction algorithm for these 'raw' images, we may easily observe how the method works. There is almost no difference in sensitivity between the center and edge (Fig.5, Left), negligibly small spectral response variation (except region, affected by IR filter) and no difference between *Gr* and *Gb* (fig.5, Right). This is another reason to refer our method to as Generalized Shading Correction. Unlike classical shading correction when we equalize 'integral' sensitivity GSC equalizes spectral response.

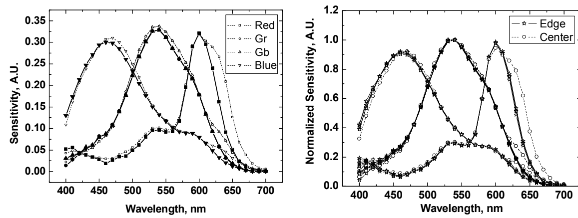

Fig.5 Spectral response and sensitivity comparison for preprocessed images. Figure layout is similar to Fig.4.

Results and Discussion

As we have shown, GSC method is capable to equalize color response of the sensor and compensate crosstalk-induced difference between Gr and Gb channels. Unlike the existing adaptive methods, where parameters for image filtering are estimated during capturing process [4], we are performing calibration based correction. This is very important property because it may correct many of image defects caused by sensor's structure with minimal losses of visual information like resolution and SNR.

First of all, we are able to correct crosstalk occurring when there is mismatch between microlens shift and imaging lens specification. In addition, we may cure modulation of sensitivity of Gr and Gb channels resulting from different pixel geometry (Fig.2).

Another important application is a camera module with optical zoom. In this case it is impossible to perform a microlens optimization for all possible zooms. If we will not use information about crosstalk distribution for a specific zoom for image enhancement, there will be strong image quality degradation. GSC method is one of the possible solutions.

Besides sensitivity equalization, the method enables us to improve color reproduction uniformity. This is one of the most common defects of existing portable camera. If fabrication process stability is good enough to provide no sample variation of color reproducibility, we are able to equalize color response with much more flexible image processing technique rather than fine-tuning of the sensors structure.

In conclusion, we are presenting comparison of our method and CSC on fig 6 and 7. Both methods were using the same test images for calibration (i.e. images taken upon illumination by monochromatic light and white target illuminated by fluorescent lamp which is different from scene illuminant, a halogen lamp) and were applied to the same images. An image interpolation and white balance were applied to the data after Classical / Generalized shading correction.

On fig.6 we are comparing overall uniformity of color reproduction of the sensor. This effect is a result of spectral response variation, presented on Fig.4 and 5. A fine detail image is shown on Fig.7. We may clearly see a checker board like noise that is pronounced on finger and almost absent on white keyboard.

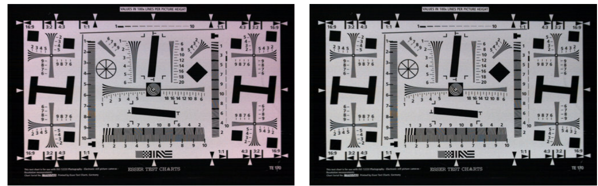

Fig.6 is an illustration of color tint correction. An image processed with CSC method is shown on left while image obtained with GSC is shown on right.

Fig.7 is an illustration of pattern noise correction. An image processed with CSC method is shown on left while image obtained with GSC is shown on right.

References

1. T. H. Hsu, Y. K. Fang, et.al., "Color Mixing Improvement of CMOS Image Sensor with Air-Gap-Guard Ring in Deep-Submicrometer CMOS Technology", IEEE ELECTRON DEVICE LETTERS, VOL. 26, NO. 5, MAY 2005
2. Igor Shcherback, Tatiana Danov et. al., "A Comprehensive CMOS APS Crosstalk Study: Photoresponse Model, Technology, and Design Trends", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 12, DECEMBER 2004
3. Gennadiy Agranov, Vladimir Berezin, "Crosstalk and Microlens Study in a Color CMOS Image Sensor", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 1, JANUARY 2003
4. Chaminda Weerasinghe, Wanqing Li, et. al., "Novel Color Processing Architecture for Digital Cameras with CMOS Image Sensors", Consumer Electronics, IEEE Transactions Volume 51, Issue 4, Nov. 2005 Page(s):1092 - 1098

A monolithic 111-M Pixel High Speed, High Resolution CCD

Richard Bredthauer Kasey Boggs Greg Bredthauer
Semiconductor Technology Associates, Inc.
27122 Paseo Espada, Suite 1004 San Juan Capistrano, CA 92677

ABSTRACT

A 111-Mega pixel, 92x92 mm^2, full-frame CCD imager with 9x9 um^2 pixel size has been developed for use in scientific applications. Recent interest for ultra-high resolution imagers for electronic imaging OEM customers in various scientific markets, including biotechnology, microscopy, crystallography, astronomy, spectroscopy, and aerial reconnaissance markets has lead to the development of the STA1600A 111-Mega pixel monochromatic charge-coupled device. Innovative design techniques were utilized in the early development of this device, yielding low RMS noise and high MTF for readout speeds ranging from 1 Mpixel/s to 25 Mpixel/sec. This paper will provide detailed information on the design and performance capabilities of the STA1600A, as well as background information on the commercial uses of this device.

Key Words: Charge Coupled Device (CCD), Charge Transfer Efficiency (CTE), RMS Noise, Quantum Efficiency (QE)

2. STA1600 DEVICE DESCRIPTION

The STA1600 is a 10560 x 10560 image element solid state Charge Coupled Device (CCD) Full Frame sensor. This device is depicted schematically in Figure 1, exhibiting split frame transfer configuration. The vertical clocks are configured such that there are eight individual sections that reduce the overall drive capacitance. This improves the vertical charge transfer efficiency (CTE), as well as reduces the risk of image smear at high frame rates. This CCD is intended for use in high-resolution scientific, space-based, industrial, military, and commercial electro-optical systems. The STA1600 is organized in two halves each containing an array of 10560 horizontal by 5280 vertical photosites. For dark reference, each readout line is preceded by 8 dark pixels. This imager is available in a full frame transfer configuration or a split frame transfer configuration with shield metallization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants. The STA1600 is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

Figure 2 represents an individual imaging subset of the STA1600A. These individually addressable output sections reduce the number of horizontal transfers, thus decreasing the readout and improving the horizontal CTE. The pixel size is 9 x 9 um in the imaging array; however the horizontal register is designed to store two times the vertical full well for binning. The output is a dual stage FET that is operable at readout rates up to 25MHz. This device was fabricated using a three-phase, triple poly, double metal process and the die size is 92 x 92 mm. The STA1600A has the capability of capturing data at a rate greater than 3 frames/second.

One difficulty with this extremely large device (die size 92 x 92 mm or 84.64 cm2) is fitting it within the useable area of a 150mm wafer. Many process areas were altered to improve not only the device yield, but also ensuring performance for a variety of end-users. Figure 3 represents a wafer from the STA1600A lot run. There are a variety of test structures around the 111-Mega Pixel imager, allowing for a timely evaluation of the fabrication process.

This device has undergone wafer level DC characterization and functional testing. The following section will cover a brief synopsis of the characterization techniques, along with detailed experimental results from the STA1600A 111-Mega Pixel imager.

3. STA1600 EXPERIMENTAL RESULTS

Fe55 images are used to calculate RMS noise and charge transfer efficiency. The STA1600A RMS noise values for various readout rates are presented in Figure 4. Figure 5 demonstrates excellent CTE of 0.999999.

Following x-ray characterization of the device are uniform illumination tests. These include PRNU, linearity, and full well measurements. The output linearity and full-well are measured using the photon transfer curve technique.[3] Figure 6 is the photon transfer curve taken with a frontside illuminated STA1600A. This chart shows an output

linearity <2%, and a pixel full-well capacity of 80000 electrons. The STA1600 has an SNR value of 78 dB at 1 MHz and 65 dB at 25 MHz.

Along with the previously mentioned specifications, cosmetic quality is of major concern for an imager of this stature. This is important criterion for the astronomical, medical, and biological imaging fields. Currently we have tested multiple STA1600A each containing a limited number of cosmetic defects. Figure 7 is a 10580 x 5280 image containing 3 column defects and 99.9993% good pixels. A column/pixel defect is defined as an area that either has excessive dark current (hot pixel) or one with poor photo-response (dark pixel).

Now that the STA1600A has undergone baseline characterization, efforts will be concentrated on high frame rate evaluation. These tests will be accomplished using the new STA Flex Cam high speed data acquisition system; where the device is currently imaging at 10MHz. This camera is an FPGA based system that utilizes high speed drivers with 40MHz at 3.5A drive capability. The video board uses a CDS analog signal chain with a 14 bit ADC.

6. SUMMARY

The STA1600A 111-Mega Pixel imager has the capability of providing high-end quality imaging for multiple markets. As camera mosaics increase in size the desirability of large scale imagers is becoming more and more evident. These STA Ultrahigh Resolution CCD's will drive down the price of scientific grade detectors by greatly decreasing the number of devices necessary for large mosaics. Also when attempting to populate a multi-gigapixel array, less devices implies a simplification in drive electronics. In conclusion the STA1600A meets the strict electro-optical detector requirements for aerial reconnaissance, thus improving the capabilities and raising the bar for industry standards.

REFERENCES

1. J. Janesick, *Scientific Charged Coupled Devices*. SPIE Press, 2001. p. 143-147, 509.

2. Philbrick, R., Geary, J.,Dunham, E., Koch, D., "95 Million Pixel Focal Plane for use on the Kepler Discovery Mission", 2004, P.Amico (ed.), Scientific Detectors for Astronomy, Kluwer Academic Publishers, p 581.

3. J. Janesick, K. Klassen and T. Elliot, "Charge-coupled device charge collection efficiency and the photon-transfer technique," *Optical Engineering* Vol. 26 No. 10 (1987).

4. S.J. Strunk, J.R.F. McMacken, S.R. Kamasz, W.D. Washkurak, F. Ma, and S.G. Chamberlain. "The development of a 4 Million Pixel CCD Imager for Aerial Reconnaissance.

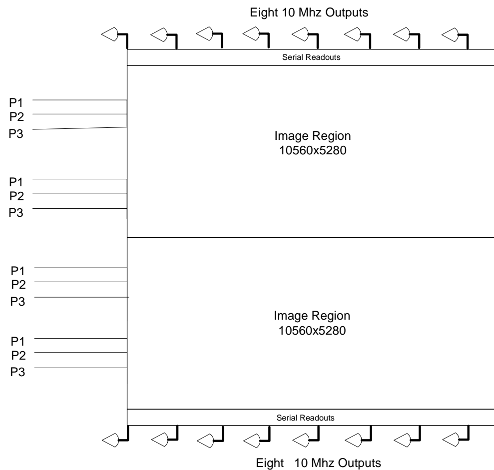

Figure 1 Configuration

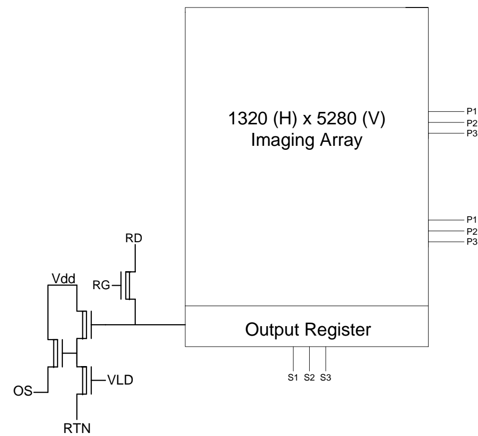

Figure 2 Single

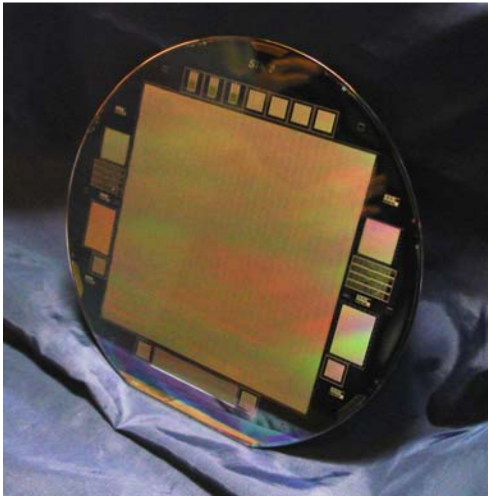

Figure 3 STA1600 Wafer

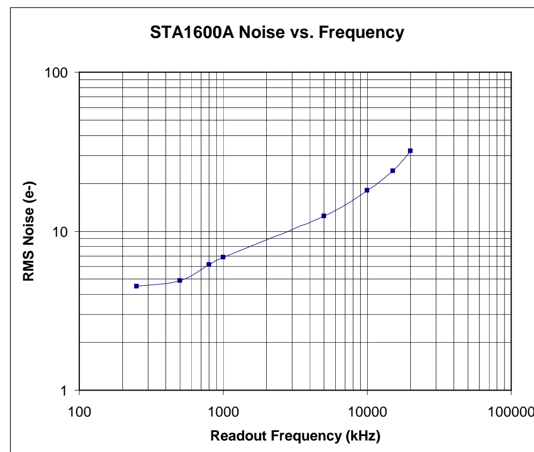

Figure 4 Noise vs

Test Parameter -75C @ 10MHz	Measured Data	Units
Parallel Charge Capacity	>80,000	e-
Serial Charge Capacity	>160,000	e-
Vertical CTE – Fe55	0.999995	per pixel
Vertical CTE – EPER	1.000000	per pixel
Horizontal CTE – Fe55	0.999985	per pixel
Horizontal CTE – EPER	1.000000	per pixel
Non-Linearity	1.0	%
Read Noise	18.2	e- rms
Dark Current	0.31	e- Non MPP
Spatial Resolution	55.56	cycles/mm
Dynamic Range	72.3	dB
Ensquared Energy	0.913	Collection Eff.
Frame Rate	3.5	frames/second

Table 1 Performance summary

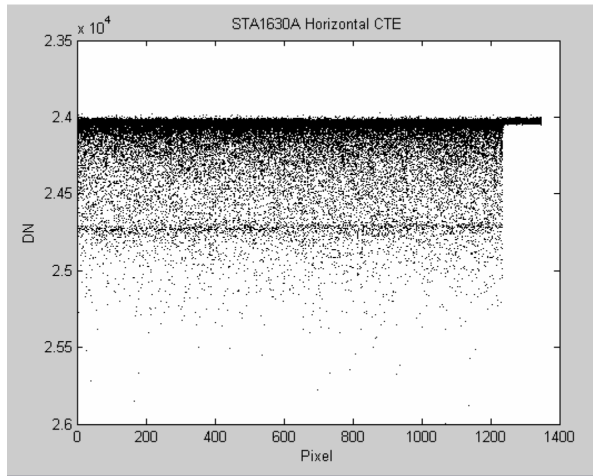

Figure 5 Charge Transfer

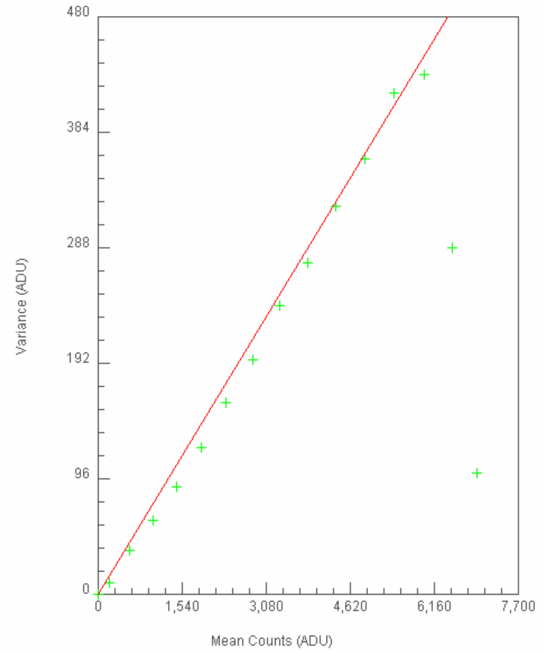

Figure 6 Photon

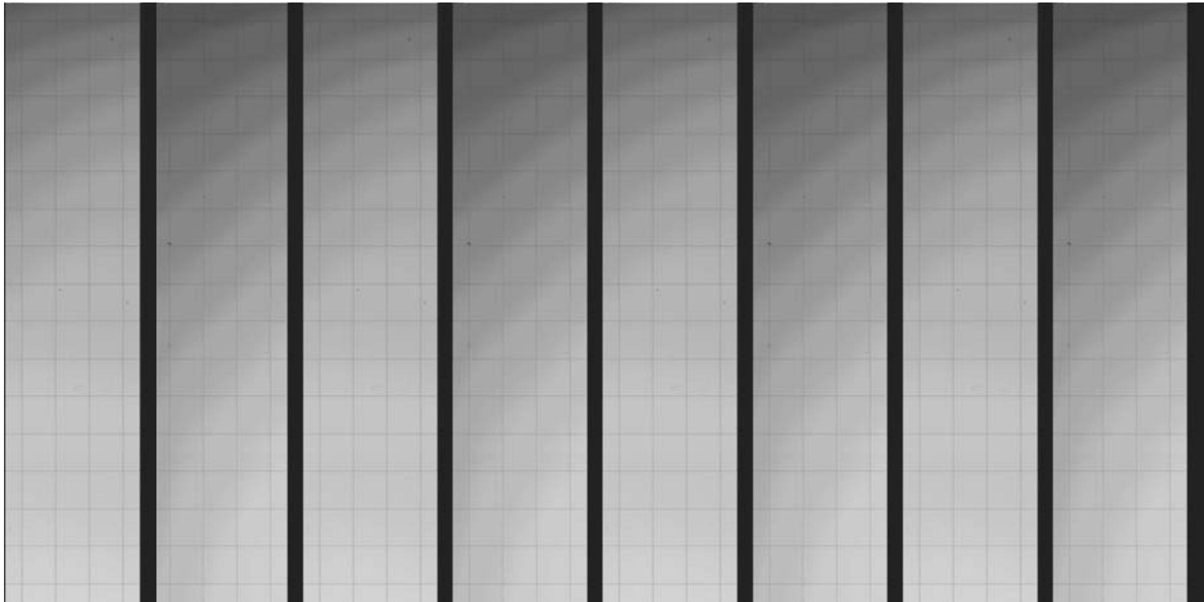

Figure 7 STA1600A 10560 x 5280 Flat Field

Sensor Development for the Large Synoptic Survey Telescope

P. O'Connor, V. Radeka, and P. Takacs
Brookhaven National Laboratory
Instrumentation Division, Bldg. 535B
20 N. Technology St., Upton, NY 11973

Abstract

The Large Synoptic Survey project proposes to build an 8m-class ground-based telescope with a dedicated wide field camera. The camera consists of a large focal plane mosaic composed of multi-output CCDs with extended red response. Design considerations and preliminary characterization results for the sensors are presented in this contribution to the Workshop.

Overview of the LSST project

The Large Synoptic Survey Telescope [1], now in the research and development phase, is designed to obtain sequential images of the observable sky every few nights from an observing site in northern Chile. With its 8.4m primary mirror, 10 deg^2 field of view, and fast readout and repointing, the LSST will yield contiguous overlapping imaging of 20,000 – 23,000 square degrees of sky in 6 optical bands covering the wavelength regime 350 – 1100 nm. Each field will be imaged thousands of times over the course of the planned 10 year survey with revisit times ranging from tens of seconds to years. The combination of wide and deep sky coverage, together with outstanding image quality provided by the site and actively-controlled telescope optics, will enable LSST to address some of the most pressing open questions in astronomy and fundamental physics.

Sensor requirements derived from science goals

The scientific goals of LSST place stringent demands on the optical, electrical, and mechanical properties of the focal plane sensors. The large field of view and plate scale of 52μm/arcsec lead to a flat focal surface of nearly 65cm diameter and 3.2Gpixels. This will be constructed as a mosaic of back-illuminated 4K X 4K CCDs having sixteenfold segmentation as shown in Fig. 1. The segmentation is chosen to allow fast parallel readout at reasonable pixel rates. The need for extended red response (> 25% quantum efficiency at 1000nm) leads to an unusually large silicon thickness. However, thick sensors require a high internal electric field to counteract diffusion. A detailed analysis of the behavior of QE and point spread function as affected by sensor thickness, resistivity, applied bias voltage, and temperature has been performed [2]. The baseline design point for LSST sensors is 100μm thickness, 10kΩ-cm resistivity, 5 kV/cm internal electric field, operating at 180K. Fig. 2 and Fig. 3 illustrate some of the tradeoffs involved. Fig. 2 shows the QE at λ=1000nm as a function of thickness and temperature, while Fig. 3 shows diffusion FWHM as a function of thickness and applied voltage.

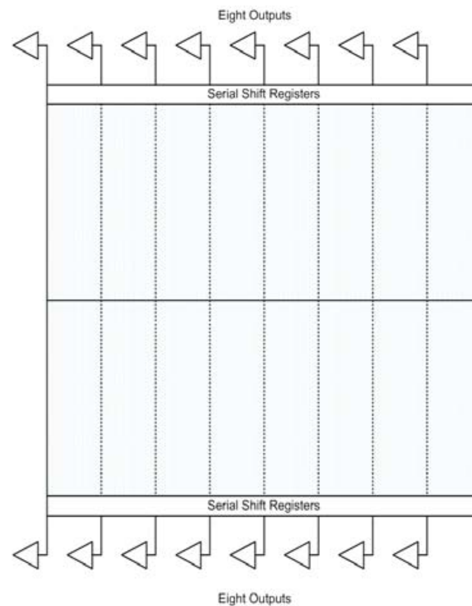

Figure 1: Proposed 4K x 4K sensor layout. Parallel clocking is vertically outward from center line. Serial registers on top and bottom shift charge to eight output amplifiers each, allowing 2s readout at 500 kpix/s.

The LSST optical system has a final focal ratio of 1/1.25; the resulting depth of focus is extremely small and both the individual sensors and the entire mosaic require careful attention to flatness. Fig. 4 shows the simulated defocus curves for sensors at three different wavelengths. To achieve LSST's PSF requirement, the sensors' entrance windows must conform to the ideal focal plane within a few microns, and the best focus must be adjusted for each band. Finally, the internal focus of the LSST's 3-mirror design constrain the camera electronics to lie directly in the shadow of the focal plane sensors. A concept for a 144Mpixel module with nine sensors and compact front end electronics has been developed in collaboration with M. Nordby at the

Stanford Linear Accelerator Center. A summary of the sensor requirements derived from LSST's ambitious survey goals is shown in Table 1.

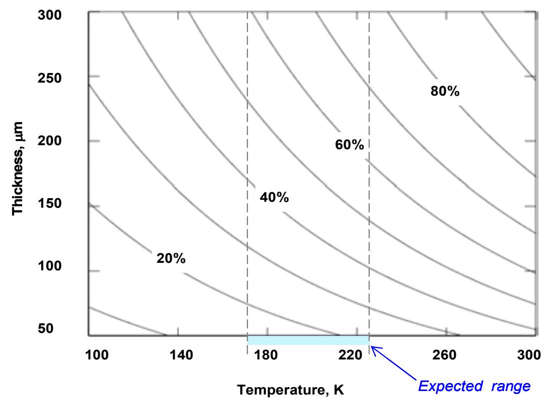

Figure 2: Quantum efficiency at 1000nm as a function of temperature and silicon thickness. LSST goal is > 25%.

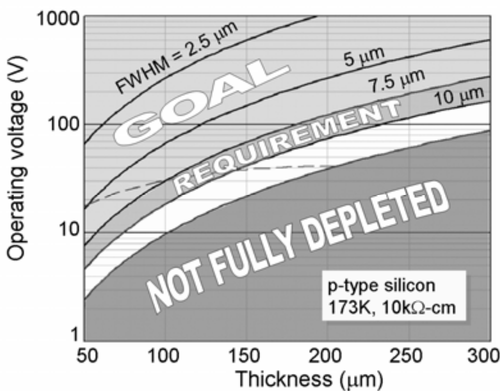

Figure 3: Diffusion FWHM as a function of silicon thickness and applied bias.

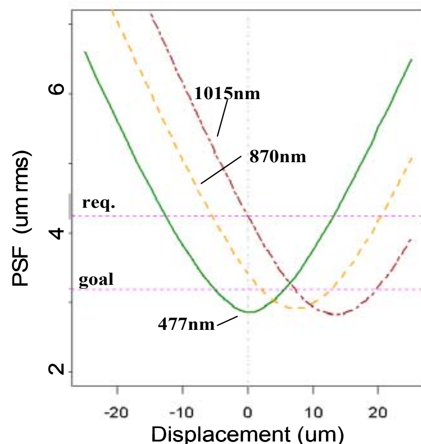

Figure 4: Defocus curves for 477nm, 870nm and 1015nm light. Position of optimum focus becomes wavelength dependent for weakly-absorbed near-IR light.

SCIENCE GOAL	SENSOR REQUIREMENT
High QE to λ=1000nm	Thick silicon (> 75µm)
Point spread function << 0.7"	Small pixel size (0.2" = 10µm) High internal field in sensor (~ 5kV/cm) High resistivity silicon (> 5kΩ-cm)
Fast f/1.2 focal ratio	Sensor flatness < 5µm pk-pk
Wide field of view (3.5°)	~3200 cm^2 focal plane ~ 200-CCD mosaic (~16cm^2 each) Industrialized production process required
High throughput	> 90% fill factor 4-side buttable package with sub-mm gaps
Fast readout (2s) with low read noise (5 e$^-$ r.m.s.)	Segmented sensors (~3200 TOTAL output ports) 150 I/O ports per CCD

Table 1: Sensor requirements derived from science goals.

Sensor Development Program

The LSST collaboration has begun a multi-year development program with several commercial CCD vendors to produce devices satisfying all technical requirements. In the first phase of this study program, vendors have delivered test devices that address the key LSST goals. Fig. 6 shows a wafer having several exploratory 4K x 4K designs, and Fig. 6 shows flatness results obtained on a set of sensors produced by a second vendor. Results of optical and electrical tests on these devices will be reported at the Workshop.

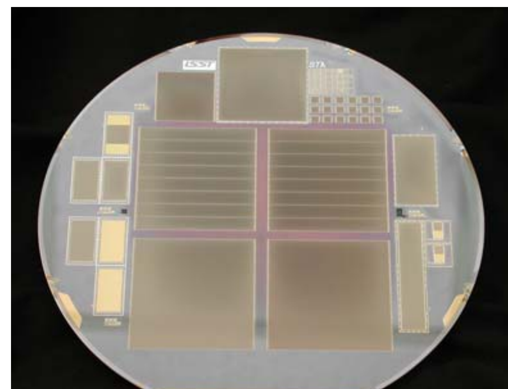

Figure 5: Test wafer having several 4K x 4K sensor designs, fabricated on high-resistivity silicon.

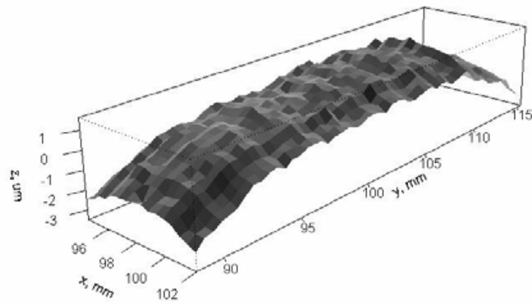

Figure 6: Flatness scan of a test device fabricated on high resistivity silicon. More than 90% of the area of each sensor is within LSST flatness specification.

References

[1] Tyson, J. A.; Wittman, D. M.; Hennawi, J. F.; Spergel, D. N., 2003, "LSST: a Complementary Probe of Dark Energy," astro-ph/0209632; Nuc. Phys. B 124, 21 (2003).
[2] P. O'Connor et al, Proc. SPIE 6276-75 (April 2006)

Lawrence Berkeley National Laboratory 2Kx4K High-resistivity CCDs for the Keck 10-meter Telescope Low Resolution Imaging Spectrograph

R. J. Stover
M.Wei
W. E. Brown
L. B. Robinson

UCO/Lick Observatory
University of California
Santa Cruz, CA 95064

The Keck 10-meter telescope Low Resolution Imaging Spectrograph[1] (LRIS) is designed to operate from the atmospheric short-wavelength cut-off at about 320nm out to a wavelength of least 1000nm. To maximize performance over the entire wavelength range the instrument is divided into a "blue" arm and a "red" arm, with separate optics and detectors in each arm. On the red side we are replacing an old Site 2048X2048 CCD with two LBNL 2048x4096 high-resistivity CCDs. At wavelengths longer than about 800nm the quantum efficiency of silicon CCDs decreases because of the increasing transparency of silicon at longer wavelengths. Since LBNL high-resistivity CCDs are up to 15 times thicker than conventional thinned CCDs (like the Site CCD now in LRIS) there is a dramatic increase in long-wavelength quantum efficiency for the LBNL CCD and this can translate directly into increased observing efficiency for many astronomical programs.

UCO/Lick Observatory has been working with LBNL for about 10 years on the development of high-resistivity CCDs[2*]. At UCO/Lick we have developed packaging techniques that allow us to create a mosaic of devices in the focal plane, with gaps between the devices limited only by the geometry of the detectors and not by the packaging. In this paper we present the characteristics of the devices which are now candidates for the LRIS spectrograph. The CCDs have 4096 rows and 2048 columns of 15-micrometer square pixels and a single serial shift register on one of the 2048-pixel sides. The CCDs have a conventional single-stage on-chip amplifier at either end of the serial register. Utilizing high resistivity silicon the CCDs are backside illuminated, fully depleted and 250 to 300 micrometers thick. These CCDs were designed by Stephen Holland of LBNL and fabricated by him, Guobin Wang, and Nick Palaio in the Microsystems Laboratory of LBNL, primarily in 2003. Preliminary results from our packaging work were presented by Stover *et.al.*[3].

The goal of the packaging effort was to produce a lightweight package which would hold the CCD optically flat at all operating temperatures and which would be convenient to use in a focal plane tiled with multiple CCDs. To achieve the greatest focal plane coverage in a tiled focal plane we required that no part of the package extends beyond the edges of the silicon of the CCD. The basic structure of the CCD package is shown in Figure 1. There are three layers of aluminum nitride (AlN) that form a mounting/cooling foot. Each of these AlN pieces is 0.080 inches thick. Between the top and bottom AlN pieces there are two floating, but captured nuts, each with a threaded hole in its center. Holes in the bottom AlN provide access to these captured nuts and allow the CCD to be mounted on a flat cold plate. Cooling of the CCD is done through the mounting foot. The three-piece foot is attached to the fourth AlN piece, which has a single-layer circuit pattern on it. The pattern, not shown in Figure 1, provides traces from the zero-insertion-force (ZIF) socket to the bond pads along the long edge of the AlN. The patterning also provides attachment points for load resistors for the CCD's on-chip amplifiers, filter capacitors, heater resistors (for temperature control) and a temperature measurement diode.

The CCD is bonded to the patterned AlN. Because the CCD is about 300 micrometers thick it is sufficiently self-supporting that it can extend beyond the two long edges of the patterned AlN, as seen in Figure 1. All of the bond pads of the CCD are exposed along these edges and simple wire bonding is used to connect these pads to adjacent pads on the patterned AlN.

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* Visit http://www-ccd.lbl.gov for access to most of the publications about LBNL high-resistivity CCDs.

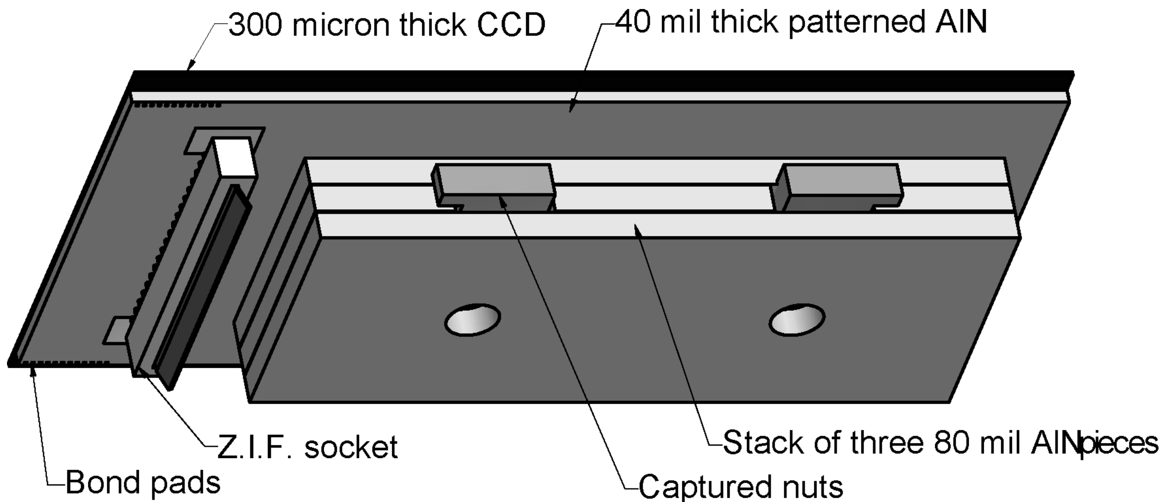

Figure 1. The structure of the CCD package consists of four layers of aluminum nitride with captured nuts that can be used for mounting the CCD to a cold surface. A zero-insertion-force (ZIF) socket accepts a ribbon cable.

All of the layers of this package are bonded to each other with Epotek 301-2 epoxy glue. The epoxy glue between each of the three AlN cold-foot pieces is about 0.004 inches thick, as is the epoxy layer between the patterned AlN and the CCD. The epoxy layer between the foot assembly and the patterned AlN is much thicker at about 0.030 inches.

The key to achieving a flat CCD is to hold the CCD flat while the epoxy glue hardens. We have achieved a high degree of flatness by holding the CCD against the face of a ceramic vacuum chuck while allowing the Epotek 301-2 glue to harden at room temperature over a two-day period. A typical grooved vacuum chuck tends to pull the CCD down into the grooves, producing a distorted CCD surface. The ceramic vacuum chuck avoids this issue with 6-micrometer pores instead of grooves. The vacuum chuck, TruVac 10"x10", grade 1, by Tru-Stone Technologies is flat to one micron over a 150 mm length. Once the CCD and patterned AlN pieces are glued together they can be handled and held with a standard, grooved vacuum chuck without distortion.

To conveniently form a focal plane array of devices all of the CCDs should have the same thickness, measured from the top of the CCD to the bottom of the cold foot. To achieve this goal the CCD packaging procedure initially produces two sub-assemblies. The first sub-assembly is the CCD glued to the patterned AlN. The second sub-assembly is the three-layer AlN foot. The thickness of the individual sub-assemblies is controlled but not critical. Final assembly is done using a precision jig to achieve the desired package thickness uniformity. The jig consists of two heavy, polished steel plates held apart by three ground and polished stainless steel spacers whose thicknesses are the same. One of the steel plates has clearance holes that match the holes in the AlN foot while the other steel plate has a typical grooved vacuum chuck pattern cut into one of its faces. The CCD is held to be vacuum chuck and the AlN foot is attached to the other steel plate with mounting screws. The steel plates are then assembled, facing each other, and held apart by the three spacers. The spacers are made so that a small gap remains between the face of the patterned AlN and the top surface of the AlN foot. This gap is filled with Epotek 301-2 and the glue is allowed to cure at room temperature.

We have assembled eight CCDs with this procedure (and several others before the final procedure was established). The average thickness of the packages is 8.778 mm with an average deviation from this mean of 0.003 mm and a maximum deviation of 0.006 mm. We also measured tilt of the CCD surface relative to the bottom of the AlN foot. The average tilt, measured at the extreme outer edges of the CCD is 0.002 mm. All of these values are within our optical tolerances for the the LRIS spectrograph.

To test dimensional stability of the CCD package we baked one of the finished CCDs in a precise temperature-controlled oven for 88 ½ hours at 80°C. We then remeasured the CCD thickness. It uniformly decreased in thickness by 6 micrometers, possibly because the epoxy glue shrank slightly. This is acceptably small, and if all device thicknesses decrease by comparable amounts they will all remain coplanar within our limits.

We have measured the flatness of the packaged CCDs. One of the CCD contour plots is show in Figure 2. It shows a peak deviation from flat of about plus or minus 5 micrometers. Because the package is fabricated from AlN, which has a very close thermal expansion match to silicon, the CCD flatness does not change appreciably when cooled from room temperature to an operating temperature of -120°C to -140°C. We have verified this result by measuring the CCD flatness while the CCD is cold and mounted in our laboratory test dewar.

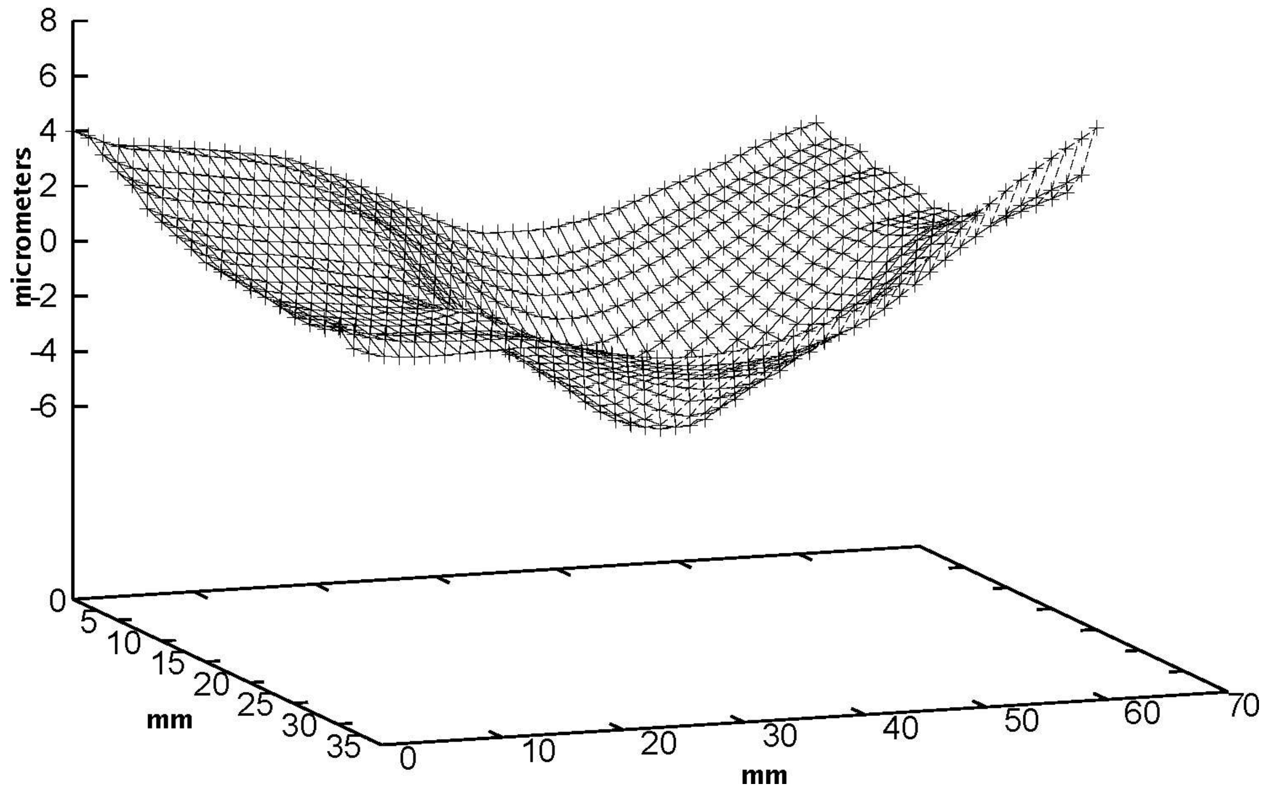

Figure 2. CCD flatness measured using a laser reflected from the CCD surface to trace the surface contour. These data show the surface shape of device 1-13 at a temperature of -137°C.

Of the packaged devices, there are three CCDs that may be good enough to be candidates for the LRIS spectrograph. Some of the other devices exhibit glowing pixels or other defects which make them unsuitable for a scientific instrument. Some of the devices have developed a very noisy amplifier and in fact we have only one device with two fully functional amplifiers. We don't know the reasons for the noisy amplifiers. Several other devices were unfortunately broken during the development of the packaging technology. Of the three best devices, one appears to be having connector problems and is functioning intermittently. We are working to understand and resolve these issues.

Once the CCDs are packaged we measure operational characteristics of all of the CCDs at cooled temperatures. In Figure 3 we show the measured quantum efficiency for device 1-13, the same CCD whose surface contours is show in Figure 2. Beyond about 800nm (8000 Angstroms) the quantum efficiency of these devices is superior to conventional thinned, backside illuminated CCDs. At 900 nm a typical thinned CCD has QE of about 20% while the device shown in Figure 3 has about 93%. At 1000 nm a typical thinned CCD has QE of about 5%, compared to 54% in the device shown.

The very high red QE also translates into another very useful characteristic, low fringing. As a conventional thinned CCD becomes transparent at the red end of the optical spectrum thin-film interference patterns develop within the CCD. These patterns are very sensitive to the exact optical illumination and to very small mechanical flexure of the instrument, and in the LRIS spectrograph changing fringe patterns is an important obstacle to the proper calibration of astronomical spectra. In the LBNL high-resistivity CCDs fringing is almost completely eliminated.

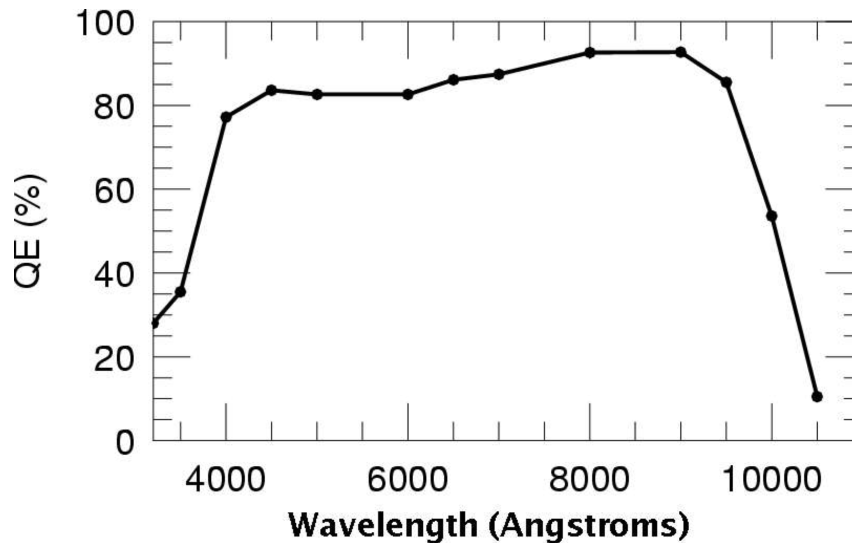

Figure 3. The quantum efficiency of device 1-13 measured at a temperature of -137°C.

We have undertaken this work to produce CCDs suitable for the Keck Observatory LRIS spectrograph. During the period of this work the understanding, design, and technologies of high-resistivity CCD manufacturing has continued to advance. CCDs produced now have superior on-chip amplifiers, a potential smaller point-spread function, and other desirable characteristics. In addition an LBNL 4Kx4K CCD may soon be available. Even with our package design there is still about a 2mm gap between active image areas of two adjacent CCDs. The use of the new 4Kx4K CCD would eliminate the gap altogether. So in the end the CCDs we have produced may end up in other applications. That decision has not yet been made.

References

1. Instrumentation at the Keck Observatory, Ian S. McLean and David Sprayberry, *S.P.I.E.*, **4841**, 1-6, 2003.
2. S. E. Holland, D. E. Groom, N. P. Palaio, R. J. Stover, and M. Wei, "Fully Depleted, Back-Illuminated Charge-Coupled Devices Fabricated on High-Resistivity Silicon," IEEE Trans. Electron Dev. 50 (3), pp. 225-238, Jan. 2003.
3. Packaging design for Lawrence Berkeley National Laboratory high-resistivity CCDs., R.J. Stover, W.E. Brown, L.B. Robinson, D.K. Gilmore, M. Wei and C. Lockwood. *S.P.I.E.*, **5499**, 518-525, 2004.

High Performance Large Format UV/optical/near IR Detector Arrays

Shouleh Nikzad, Michael E. Hoenk, Jordana Blacksberg, Todd J. Jones, Thomas J. Cunningham
Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109

Stephen E. Holland, William Kolbe, and Chris Bebek
Lawrence Berkeley National Laboratory, Berkeley, CA

There is an increasing need for large format imaging and detector arrays. For example, future NASA missions as well as DoD missions will require large format high performance imaging arrays in a mosaic or monolithic focal plane to achieve wide field of view, high-resolution imaging (and spectroscopy). The basic array design for each application might require CMOS or CCDs unique features.

CMOS arrays are the leading candidates for DoD missions where their speed/power performance and windowing capabilities are of key importance. Back-illumination of CMOS arrays allows 100% fill factor, wider spectral range, and high QE.

We have developed complete end-to-end post fabrication processes at JPL that have allowed us to produce high performance back illuminated imaging arrays of widely varying designs including n-channel CCDs, p-channel CCDs, and CMOS arrays. Delta doping was developed at JPL to enable UV sensitivity and enable high QE over the silicon spectral range. In this process an ultrathin layer of highly doped, high quality epitaxial silicon is grown on the back surface of fully fabricated array. We will present results of thinned and boron delta doped n-channel CCDs and CMOS arrays.

For many astrophysics survey missions and dark energy missions, low signal demands long integration time and low noise. CCDs are often detector of choice for these applications. Because of the redshifts involved, such missions often require very thick depletion regions to be able to detect near-IR with high QE. Lawrence Berkeley National Laboratory (LBNL) has developed p-channel devices in ultrahigh purity silicon to achieve a combination of thick fully depleted detectors and low noise required.

To address the new technology required for depleting, passivating, and enabling high QE in UV to NIR with p-channel back illuminated thick devices, we have developed a low temperature process for Sb delta-doping of silicon. This process can be used to form a thin back-surface contact for fully processed back-illuminated, high purity p-channel CCDs. Non-equilibrium growth by Molecular Beam Epitaxy (MBE) is used to achieve very high dopant incorporation in a thin, surface-confined layer. Optimization of this process has enabled the growth of a thin highly conductive back surface electrode on p-channel CCDs. The temperature is kept below 450 °C throughout the entire process, which is required for compatibility with fully processed and functional Al-metallized devices. We will present our latest results on delta-doping of large-format high purity CCDs. Performance parameters such as near-100% internal QE, dark current $< 1e^{-}$/pixel/hour, and exceptional stability and uniformity in the 200-1100 nm spectral range will be presented.

Dr. Shouleh Nikzad
Jet Propulsion Laboratory M/S 302-306
4800 Oak Grove Dr.
Pasadena, CA 91109-8099
(818) 354-7496
(818) 393-4540
email: Shouleh.Nikzad@jpl.nasa.gov.

Figures

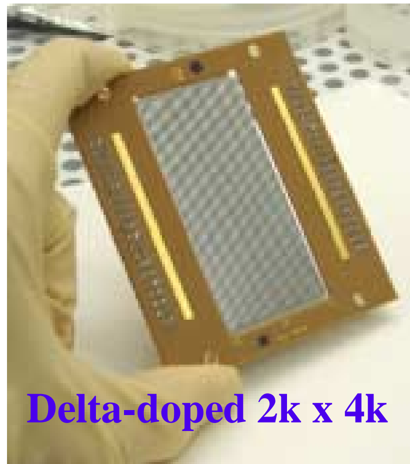

Figure 1. Photograph of an individually-packaged large format (2K x 4K) delta doped array. These arrays are 4-side buttable and can form mosaics of gigapixel focal plane arrays.

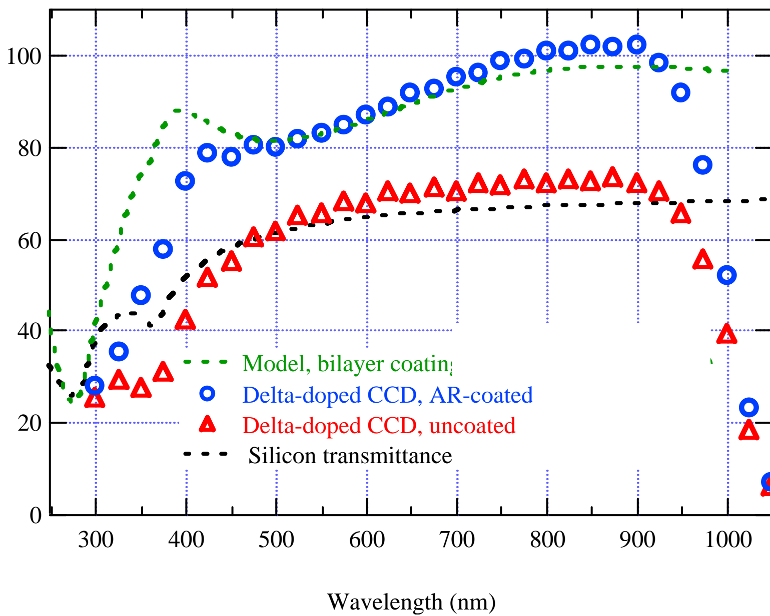

Figure 2. Response of delta doped high purity p-channel array with and without AR coating. The AR coating in this example was designed for a broadband optical/NIR response.

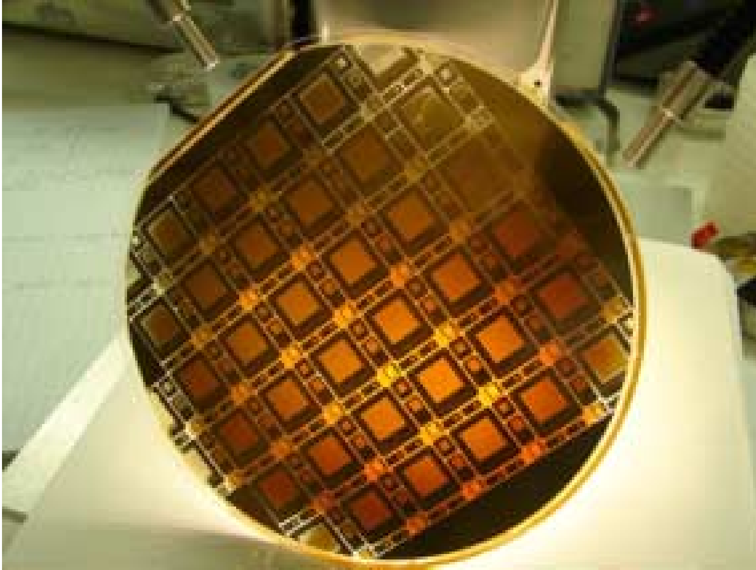

Figure 3. Photograph of a 6-inch wafer containing CMOS arrays, thinned down to several microns.

Highly Sensitive VGA FEA-HARP Image Sensor

N. Egami[1], M. Nanba[1], Y. Honda[1], Y. Hirano[1], K. Miyakawa[1], Y. Ookawa[1], T. Watabe[1], S. Okazaki[1], K. Miya[2], K. Nakamura[2], T. Niiyama[2], M. Taniguchi[2], S. Itoh[2], and A. Kobayashi[3]

[1] NHK Science & Technical Research Labs, 1-10-11, Kinuta, Setagaya, Tokyo 157-8510, JAPAN
TEL: +81-3-5494-3210, FAX: +81-3-5494-3278, e-mail: egami.n-fs@nhk.or.jp
[2] Futaba Co., Chiba 299-4395, JAPAN
[3] Hamamatsu photonics K.K., Hamamatsu-shi 438-0193, JAPAN

Abstract

A 640×480 pixel image sensor consisting of 20×20-μm pixels, which consisted of an integrated field emitter array equipped with an active drive circuit and a highly sensitive avalanche-mode photoconductive target was fabricated and tested to investigate the feasibility of a high-resolution sensor with a large number of smaller pixels. Our experimental results revealed that the prototype obtained both high sensitivity due to the avalanche multiplication effect of the target and sufficient resolution as a VGA image sensor.

1. Introduction

We have been studying a flat field emitter array (FEA) image sensor with a highly sensitive, high-gain avalanche rushing amorphous photoconductor (HARP) target [1], [2], with the aim of developing high-sensitivity compact HDTV cameras. Our previous experiments on a 256×192 pixel (pixel size, 50×50-μm) FEA-HARP image sensor confirmed that the sensor obtained high sensitivity and had sufficient resolution and a wide dynamic range [3], [4]. However, for practical purposes, a high-resolution sensor with a large number of smaller pixels must be developed. A 640×480 pixel (pixel size, 20×20-μm) VGA format FEA-HARP image sensor was fabricated and tested to investigate the feasibility of the high-resolution sensor.

This paper describes the configuration and specifications of the prototype sensor. The prototype's image pick-up characteristics are also discussed.

2. Problems with previous sensor

The configuration of the previous FEA-HARP image sensor is depicted in Fig. 1. The sensor consists of a Spindt-type FEA [5], [6], a mesh electrode, and a HARP target, in close proximity to each other. The HARP target converts incident light into electron-hole pairs. The number of holes is increased by the internal avalanche multiplication effect, and a charge (hole) pattern corresponding to the optical image is formed at the electrons' scanning side of the HARP target. Electrons emitted from each pixel of the FEA are drawn to the HARP target side by the high potential of the mesh electrode, and are focused on the HARP target by a magnetic field between the FEA and the HARP target. The output signal current is obtained by recombining holes accumulated on the HARP target and scanning electrons emitted from the FEA.

The previous sensor, with 256×192 pixels, had high potential for image sensing due to its high sensitivity, sufficient resolution, and wide dynamic-range. However, because conventional passive-matrix Spindt-type FEAs are driven by applying pulses to gate-and-cathode electrode lines from external circuits, its driving speed was limited

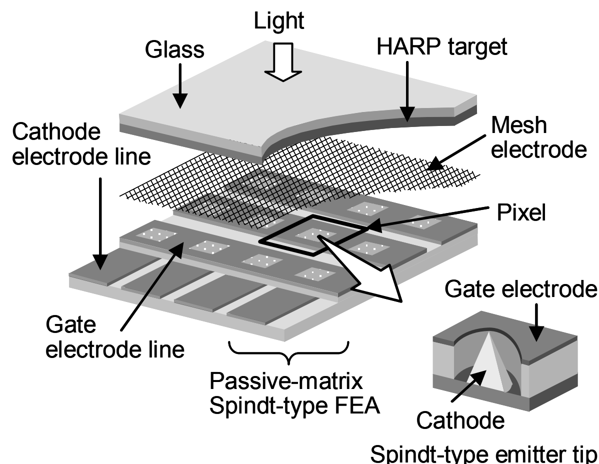

Fig. 1 Configuration of previous FEA-HARP image sensor

by a large load-capacitance between the electrode lines. A large number of interconnections between the FEA and external circuits, which was equivalent to the sum of the number of vertical and horizontal pixels, was also required to drive the FEA. These constituted limiting factors for the high-resolution FEA-HARP image sensor with a larger number of pixels.

3. Fabrication of VGA FEA-HARP image sensor

3.1 Active-matrix Spindt-type FEA

A new Spindt-type FEA with a built-in active-matrix drive circuit was developed to overcome the problems mentioned above. The configuration of this FEA is shown in Fig. 2. The active-matrix circuit consisted of pixel-select transistors in the pixel area, and vertical and horizontal scanning drivers outside the pixel area, which was fabricated on a silicon wafer using MOS-LSI technologies. The Spindt-type FEA was formed on the pixel-select transistors, and the emitter tips in a pixel and the drain of the pixel-select transistor were connected through a via plug. The gate electrode of the FEA is electrically continuous over the entire pixel area. Electrons are sequentially emitted from each pixel of the FEA by switching the pixel-select transistor in each pixel with control pulses from the vertical and horizontal scanning drivers. Figure 3 shows the circuitry of the active-matrix FEA in comparison with that of a conventional passive-matrix FEA. The active-matrix circuitry ensures high-speed operation of the FEA because the load capacitance of the active-matrix FEA is substantially smaller than that of the conventional passive-matrix FEA. Moreover, because the vertical and horizontal scanning drivers are built into the FEA, the active-matrix FEA can be driven by applying several control pulses through a small number of interconnections between the FEA and the external circuits regardless of its pixel number.

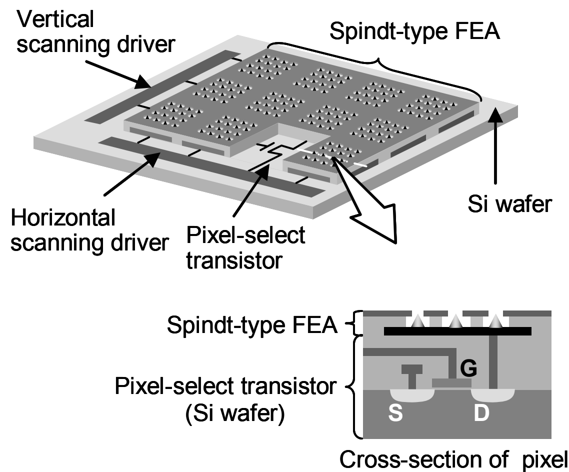

Fig. 2 Configuration of active-matrix Spindt-type FEA

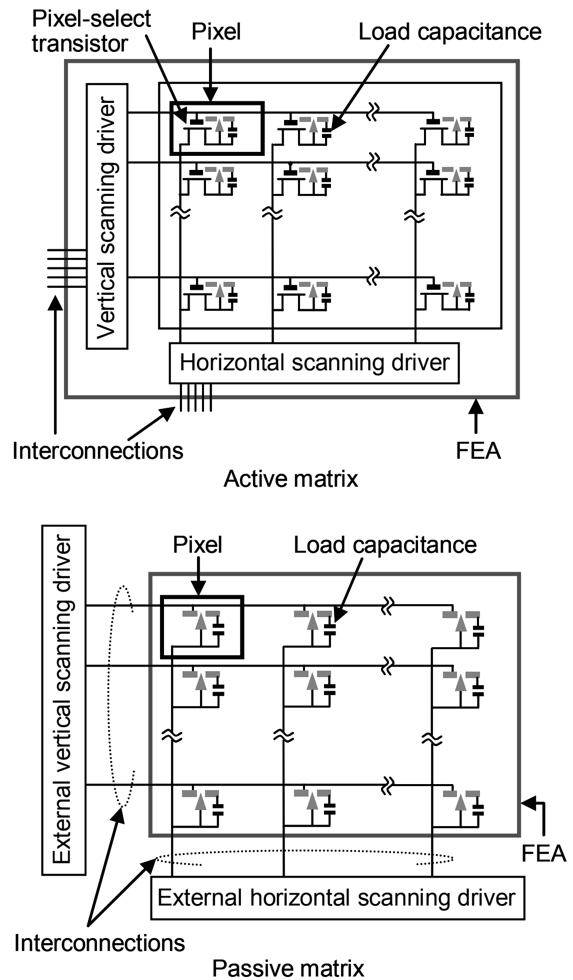

Fig. 3 Comparison of active-matrix and passive-matrix circuitries

Figure 4(a) is an overview of the fabricated active-matrix FEA, and (b) is a scanning electron microscope (SEM) image of a pixel. The FEA was 15×12 mm, and the pixel area was 12.8×9.6 mm. The vertical and horizontal scanning drivers were integrated outside the pixel area. The FEA had 640×480 pixels, which is equivalent to the VGA format, and the pixel size was 20×20 μm. To obtain sufficient emission current from each pixel, 121 Spindt-type emitter tips with a gate-hole diameter of about 0.8 μm were placed within a 14×14-μm area of

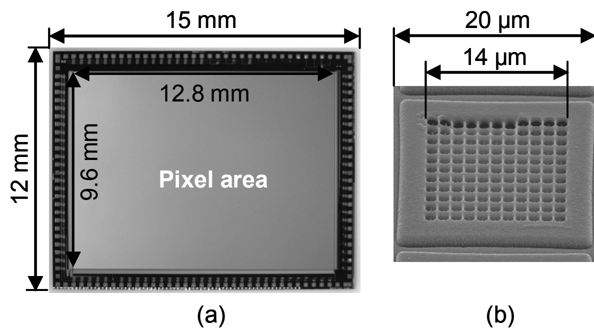

Fig.4 Fabricated active-matrix Spindt-type FEA
(a) Active-matrix FEA (b) SEM image of pixel

Fig. 6 Reproduced image taken by prototype sensor
(Illumination, of 0.3 lx,; lens iris, of F1.2)

each pixel.

3.2 VGA FEA-HARP image sensor

Figure 5 is a photograph of the fabricated VGA FEA-HARP image sensor with the active-matrix Spindt-type FEA, which was about 10 mm thick. The distance between the FEA and the HARP target was about 2.5 mm, and the mesh electrode, which had an aperture ratio of about 45%, was midway between the FEA and the HARP target. The thickness of the HARP target was 15 μm. There were only 10 interconnections to drive the FEA, which is drastically fewer than the conventional passive-matrix 256×192 pixel FEA image sensor (with 448 interconnections) [3], [4].

4. Image pick-up characteristics of prototype

The active-matrix Spindt-type FEA of the prototype sensor was driven with pixel sequential scanning that complied with the NTSC standard. By adjusting the control pulses sent to the vertical and horizontal scanning drivers, we set the width and the interval of the equivalent drive pulses for pixel sequential scanning to approximately 0.08 μs and 1/60 s, respectively. A voltage of about 700 V was applied to the mesh electrode, and a voltage of up to 1550 V was applied to the HARP target. Moreover, a uniform magnetic field with a flux density of about 0.125 T was applied inside the prototype sensor to focus electrons emitted from each pixel of the FEA.

Figure 6 is a reproduced image taken by the prototype sensor, under an illumination of about 0.3 lx and a lens iris setting of F1.2. A clear image with sufficient resolution was obtained even in lighting conditions that were as dim as moonlight.

Figure 7 plots the dependence of the output signal current on HARP target voltage. The signal current abruptly increased above the target voltage of 1200 V, indicating the presence of the avalanche multiplication effect inside the 15-μm-thick HARP target. An avalanche multiplication factor of about 200 was obtained at the target voltage of 1550 V.

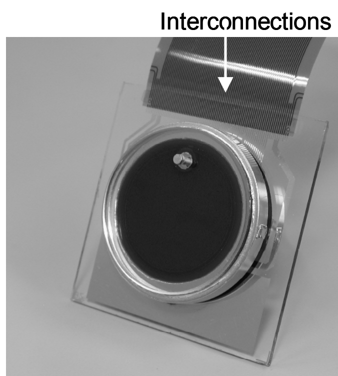

Fig.5 Fabricated VGA FEA-HARP image sensor

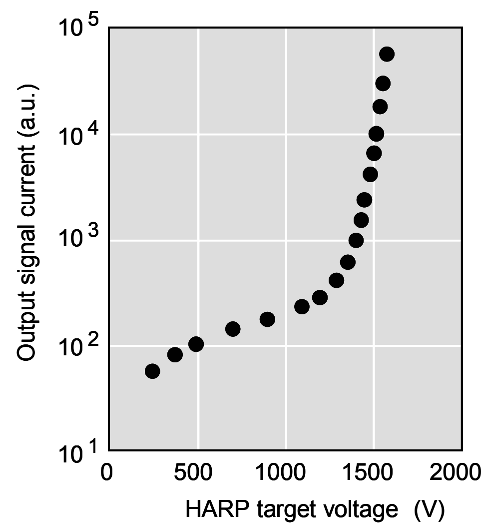

Fig. 7 Sensitivity characteristics

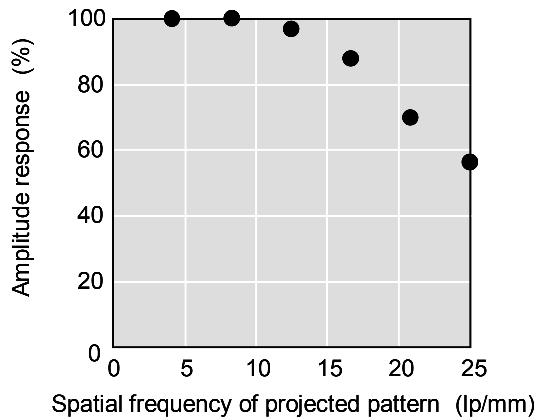

Fig. 8 Resolution characteristics

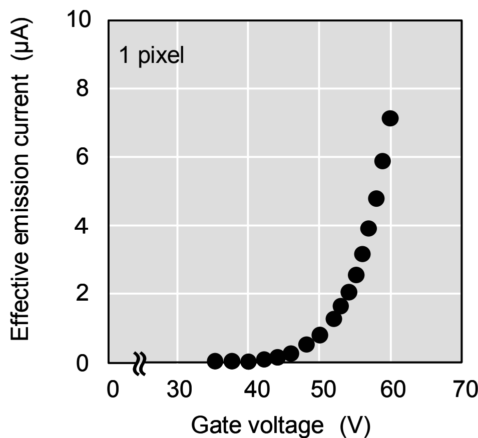

Fig. 9 Emission (dynamic range) characteristics

Figure 8 plots the resolution characteristics. The resolution was defined by the amplitude response when a black and white vertical-stripe pattern with various spatial frequencies was projected on the HARP target. The amplitude response of the prototype was about 56% at the Nyquist spatial frequency (a spatial frequency of 25 lp/mm or a stripe pitch of 20 μm), and the uniformity of resolution was good. The results demonstrate that the prototype has sufficient resolution as a VGA image sensor.

In Fig. 9, the dependence of the effective emission current on the gate voltage is indicated. The dynamic range of the FEA image sensor is determined by the effective emission current, which is defined as the current originating from electrons transmitted through the mesh electrode and reaching the HARP target. The effective emission current of the prototype was about 7 μA when the gate voltage was 60 V and the aperture ratio of the mesh electrode was about 45%. These results show that the prototype can obtain a wide dynamic range because the effective emission current required for ordinary image pick-up operation is estimated to be about 2 μA.

5. Conclusion

The goal of our work has been to develop FEA image sensors for ultrahigh-sensitivity compact HDTV cameras that can be used in various fields such as broadcasting, medicine, security, and natural sciences.

Our experimental results on the fabricated 640×480 pixel HARP image sensor with the active-matrix Spindt-type FEA revealed that the prototype sensor obtained sufficient resolution as a VGA image sensor, as well as high sensitivity and a wide dynamic range, yet offers convenient operation.

As we continue to work towards our goal, we plan to develop new FEAs with a larger number of much smaller pixels, and electro-static focusing systems.

References

[1] K. Tanioka, J. Yamazaki, K. Shidara, K. Taketoshi, T. Kawamura, S. Ishioka, and Y. Takasaki: “An-avalanche-Mode Amorphous Selenium Photoconductor Layer for Use as a Camera Tube Target,” IEEE Electron Device Letters, EDL-8, 9, pp. 392-394 (1987).

[2] K. Tanioka, T. Matsubara, Y. Ohkawa, K. Miyakawa, S. Suzuki, T. Takahata, N. Egami, K. Ogusu, A. Kobayashi, T. Hirai, T. Kawai, M. Hombo, and T. Yoshida: “Ultra-high-sensitivity New Super-HARP Pickup Tube and its Camera,” IEICE Transaction on Electronics, E86C, 9, pp. 1790-1795 (2003).

[3] N. Egami, M. Nanba, Y. Takiguchi, K. Miyakawa, T. Watabe, S. Okazaki, K. Osada, Y. Obara, M. Tanaka, and S. Itoh: “50×50 μm Pixel Magnetic Focus Field Emitter Array Image Sensor with High-gain Avalanche Rushing Amorphous Photoconductor,” J. Vac. Sci. Technol. B, 23, 5, pp. 2056-2062 (2005).

[4] Y. Hirano, M. Nanba, Y. Honda, K. Miyakawa, T. Watabe, S. Okazaki, and N. Egami: “Highly Sensitive Magnetic Focus FEA Image Sensor with HARP Target,” Proc. of IEEE Workshop on CCD&AIS, R14, pp. 521-55 (2005).

[5] C.A. Spindt, I. Brodie, L. Humphrey, and E. R. Westerberg: "Physical Properties of Thin-film Field Emission Cathodes with Molybdenum Cones," J. Appl. Phys., 47, 12, pp. 5248-5263 (1976).

[6] S. Itoh, N. Mutoh, M. Tanaka, and T. Tonegawa: “Development of Field Emission Display,” Tech. Digest 16th IVMC, I3-1, pp. 19-20 (2003).

A 1½D CMOS Active Pixel Sensor for X-ray imaging

R.Turchetta[a], A. Fant[a], P. Gasiorek[a], C. Esbrand[b], J. A. Griffiths[b], M. G. Metaxas[b], G. J. Royle[b], R. Speller[b], C. Venanzi[b], P. F. van der Stelt[c], H. Verheij[c], G. Li[c], S. Theodoridis[d], H. Georgiou[d], D. Cavouras[e], G. Hall[f], M. Noy[f], J. Jones[f], J. Leaver[f], D. Machin[f], S. Greenwood[f], M. Khaleeq[f], H. Schulerud[g], J. M. Østby[g], F. Triantis[h], A. Asimidis[h], D. Bolanakis[h], N. Manthos[h], R. Longo[i], A. Bergamaschi[i]

[a] Rutherford Appleton Laboratory, Chilton, Didcot, Oxon, OX11 0QX, United Kingdom, [b] Department of Medical Physics & Bioengineering, University College London, [c] Academic Centre for Dentistry, Vrije Universiteit & University of Amsterdam, The Netherlands, [d] Department of Informatics & Telecommunications, University of Athens, Greece, [e] Medical Image and Signal Processing Laboratory, Department of Medical Instrument Technology, Technological Education Institution of Athens, Greece, [f] High Energy Physics Group, Department of Physics, Imperial College, London, U.K, [g] Division of Electronics and Cybernetics, SINTEF, Oslo, Norway, [h] Department of Physics, University of Ioannina, Greece, Department of Physics, University of Trieste, Italy.

We present a novel 1 ½ D CMOS Image Sensor for X-ray application. This sensor was developed within the EU-funded project *Intelligent Imaging Sensors for Industry, Health and Security* (I-ImaS).

The main target of the project is the development of a system for mammography and X-ray extraoral dental imaging. The camera concept (figure 1) is novel and is patented by the consortium. The camera consists of two lines of sensors. The image is built-up by scanning the sensors across to cover the full area. In the first scan, about 80% of the normal dose is delivered. The obtained image is processed in real time and information about interesting areas is extracted. Only those areas are imaged in the second scan. Simulations show the image quality is preserved while reducing the dose.

For the scanning approach, we considered both Time Delayed Integration (TDI) and Step-and-shoot approaches (S-S). TDI in CMOS sensors reduces the signal-over-noise [1]. In the S-S approach, the sensor integrates light for a fixed time in a each position before moving to the next one. In order to optimize the integration time, 32 lines of pixels are laid out on the sensor, hence the name 1½ D.

The floorplan of the sensor is shown in figure 2. It consists of 520x40 pixels, including 4 lines on each side for edge effect reduction. The 8 extra rows can be read out, although they would not normally be. Only the central 512 columns are readout. They are organized in 16 blocks of 32x32 pixels. Rolling shutter readout is used.

The pixel size is $32x32\mu m^2$ and the estimated collected charge per pixel changes with the energy of the X-ray, the scintillator used and the exposure time. The estimated value ranges (in electron/hole pairs) used for this design are reported in Tab 1, assuming a structured CsI scintillator and a 10 ms exposure as for the mammography case.

The collected charge for the dental imaging application is approximately the same, considering that the X-rays have higher energy (around 100keV) but the best exposure time is about a third (3ms), so one detector can fulfill both needs. Choosing to resolve at least 4 times the average tissue level to reach the skin line level [3], and keeping some dynamic range available in case the scintillator performs next to the its expected best, we chose a full well capacity for the diode of around 200000 e^-. With a 3.3V reset voltage and a 5V drive on the reset transistor's gate, the available output voltage range is about 2.2V. The required diode capacitance can then be defined as:

$$C_d = \frac{Q_{max}}{\Delta V_{max}} = 14.5\,fF$$

The k_BTC noise is then fixed at 48.4 e^- ENC (@300K) and the maximum S/N rate is 72.2dB.

Different pixel reset schemes are possible, including hard, soft and flushed, in order to reduce the KTC noise [4, 5].

At the bottom of each column (on the left in figure 3), a 3-bit circuit for FPN reduction is implemented together with an analogue multiplexer. There is no sampling capacitance as in normal camera operation the sensor is illuminated only during data taking. For testing with constant

illumination or in other application, Correlated Double Sampling (CDS) is used: each time the pixel is addressed, the floating node voltage is first read, the pixel is then reset and the reset voltage is read out and stored in memory. It will then be subtracted at the next reading. Each block of 32 columns is analogue multiplexed into a Programmable Gain Amplifier (PGA), with gain settings of 1 and 2. The output of the PGA is digitized on chip by a 14-bit SAR ADC. The SAR ADC (figure 4) has a hybrid architecture [2], using a resistive ladder for the 4 MSB and a capacitance bank for the other 10 bits. The capacitor bank is split into two banks, each taking care of 5 bits. The two banks are connected together by a series capacitance with a 5-bit calibration network. This architecture was chosen as the best compromise between capacitance matching, noise and area. The ADC can run at 20 MHz and takes 16 clock cycles (2 cycles for sampling the pixel voltage) for one conversion. The sampling rate is then 1.25MHz. Most of its power consumption is due to the dc current through the resistor string, around 2.5mA per ADC. The digital output multiplexer scans through all ADCs' outputs and splits them to be sent out on a 7 bit bus at 40MHz rate. Since there are 16 ADCs and it takes 16 clock cycles for a conversion, there's no dead time and all data are read out before a new sample (next pixel value) is converted.

Tab 1: Estimate of the collected charge per pixel

		minimum	maximum
White level		250000	500000
Tissue		30000	60000
Dense	max	25000	50000
tissue	min	12500	25000

The sensor (figure 5) was designed and manufactured in 0.35 μm CMOS Image Sensor technology on a 14 um thick epitaxial layer. The sensor was characterised optically (figure 6) and for direct X-ray conversion (figure 7) and then with a CsI scintillator mounted on it for indirect X-ray detection (figure 8). The test results shown here were obtained at the synchrotron machine Elettra in Trieste, Italy. The spatial resolution of the sensor plus scintillator is dominated by this latter. A structured scintillator will be used for the camera design as this would give the best MTF.

Images (figure 9 and 10) of different objects were obtained by scanning a single sensor across the imaging area. All images were then stitched together by using the correct pixel overlap. Gain corrections were then applied to take into account both variations in gain within the sensor and variation in beam intensity during the scan. Below is an image of a sensor mount ceramic card. The image shown below was taken at 75 kVp and 4 mA. The card is 30x10mm and the distance between each scanning step was taken equal to 832 μm, corresponding to 26 pixels. The integration time for each single step was 10 ms. For this image, the sensor was coupled to an unstructured CsI scintillator.

The full camera would consist of two lines of 10 sensors. A prototype is currently being developed and its construction should be completed in the next few months.

Acknowledgements

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Reference

[1] H. Michaelis et al., *CMOS-APS Sensor with TDI for High Resolution Planetary Remote Sensing*, Extended programme of 2005 IEEE Workshop on CCDs and AIS, Japan, 31-34
[2] A. I. Krymski et al., *A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS* Sensor, IEEE Trans. on Electron Devices, vol. 50, no. 1, January 2003, 130-135
[3] M.M. Tesic, M. Fisher Piccaro, and B. Munier, *Full field digital mammography scanner*, European Journal of Radiology 31 (1999) pp. 2-17
[4] H. Tian, B. Fowler, and A. El Gamal, *Analysis of temporal noise in CMOS photodiode active pixel sensors*, IEEE JSSC, vol. 36, no. 1, Jan 2001
[5] B. Pain, G.Yang, T.J. Cunningham, C. Wrigley, and B. Hancock, *An enhanced-performance CMOS imager with a flushed-reset photodiode pixel*, IEEE Electron Devices, vol. 50, no. 1, Jan 2003 pp. 48-56

Figures

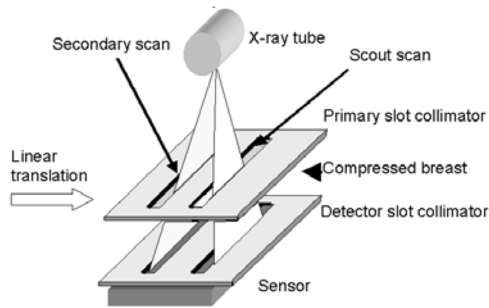

Figure 1. I-ImaS X-ray camera, with the double-scanning concept

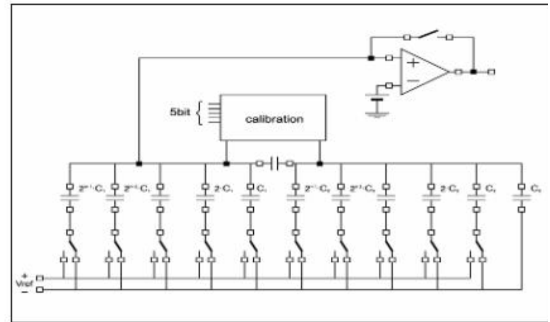

Figure 4. Block diagram of the SAR ADC, resistive ladder not included

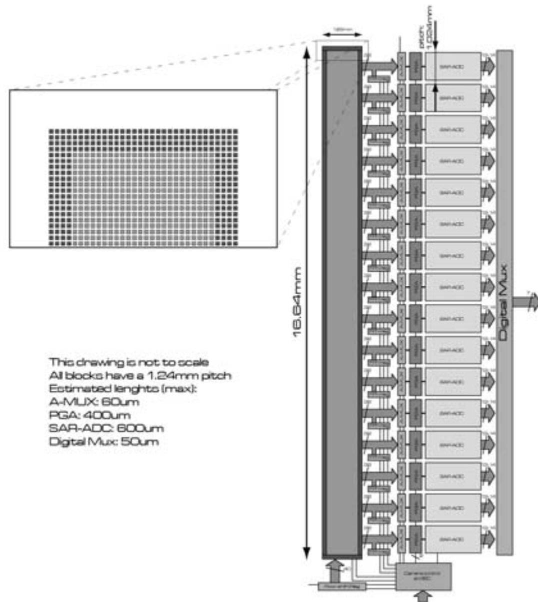

Figure 2. Floorplan of the I-ImaS 1½D sensor

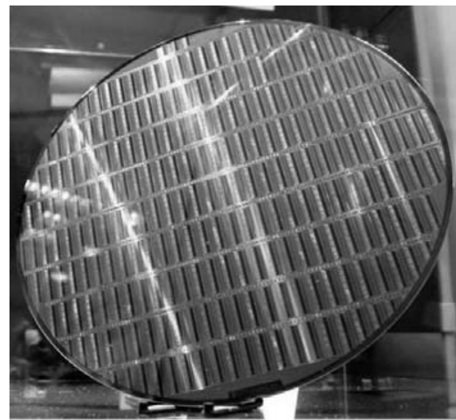

Figure 5. I-Imas sensor wafer

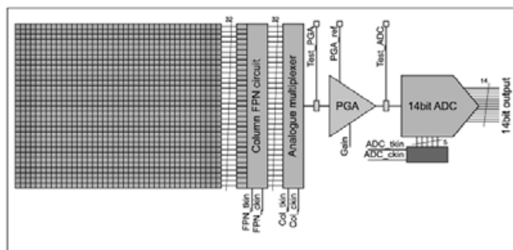

Figure 3. Schematic diagram of one readout channel

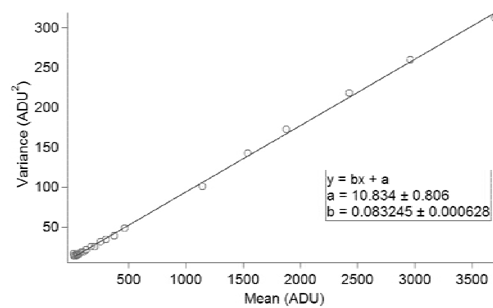

Figure 6. Optical PTC

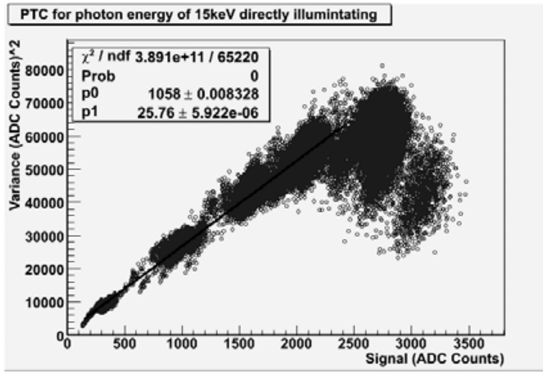

Figure 7. Direct X-ray detection PTC

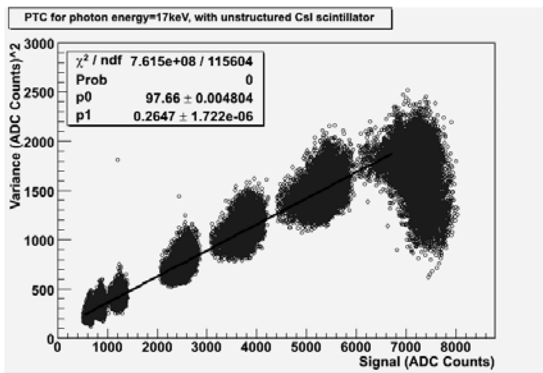

Figure 8. Indirect X-ray detection PTC.

Figure 9. Image of a ceramic PCB; taken at 75kVp and 4mA current.

Figure 10. Image of a tooth taken at 70kVp and 6mA current.

SOI-based Monolithic Imaging Technology for Scientific Applications

Bedabrata Pain, Chao Sun, Xinyu Zheng, Suresh Seshadri, and Thomas J. Cunningham
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov

This paper describes the development of SOI-based CMOS monolithic visible imagers for astronomy and astrophysics applications that require extended NIR response.

Many existing and next generation astronomy applications require very large format imager arrays with low dark current and excellent quantum efficiency (QE) and modulation transfer function (MTF) above 1 μm. The requirement of large format arrays makes silicon a natural choice as the detector material, although there has been significant progress in substrate-removed InGaAs or HgCdTe materials [1] for extending higher frequency response of materials that have been more traditionally used for infrared detection.

Achieving high optical sensitivity and high modulation transfer function (MTF) at above 1 μm with silicon require the use of extremely low-doped wafers that are very thick (~ 50-100 μm) and are fully depleted. To deplete 50-100 μm of silicon of a few kΩ of resistivity, more than 30-50 V of reverse-bias is necessary. Such voltages are not compatible with sub-micron CMOS processes.

Both CCDs [2,3] and CMOS imagers [4,5,6] have been built in high-resistivity silicon. However, unlike CCDs that use a monolithic approach, these CMOS imagers have been built using a hybrid approach. In these hybrid imager arrays, the detector and readout electronics exist in two separate silicon wafers. Each detector pixel is connected in a "one-to-one" basis to a corresponding readout element on the other chip. The advantage of such an approach is that it allows "mixing and matching", and independent optimization of both the detector and readout. On the other hand, hybridization – i.e. making millions of interconnects across two wafers – presents manufacturability challenges. Most common hybridization techniques employ indium bump-bonding, although in recent years, the "3-D" electronics technology featuring wafer-to-wafer aligned bonding, and through-wafer high density interconnects have been developed [7]. However, the mainstream of emerging "3-D" electronics technology is geared towards wafer-to-wafer interconnect density and pitch that are not compatible with large format arrays with small pixel pitch. Another problem that has been reported with hybrid detectors is the presence of intra-pixel capacitance resulting in large and signal-dependent pixel-to-pixel cross-talk [8].

Our approach uses a SOI-based monolithic CMOS imager concept [9, 10]. Similar concepts have been used for particle detection [11, 12]. Previously, we had reported the SOI imager concept as well as the formation of starting materials. The reported dark current was high, although dark current reduction strategies were enumerated [10, 13]. In this work, we report the development, and initial measurement results from a 512x512 SOI imager in a 9 μm pixel pitch, implemented in a 0.18 μm 3 metal partially-depleted SOI CMOS fabrication process.

SOI technology solves the problems mentioned above by using the built-in buried oxide layer to separate the diode layer (handle wafer) from the pixel readout electronics layer (top SOI layer), allowing independent optimization and biasing of both – as shown schematically in figure 1. The use of SOI technology allows integration of the diode and pixel readout is carried in a monolithic fashion, without requiring hybridization either of bump-bonding kind or of the "3-D" interconnect kind.

The pixel diode, residing in the handle wafer, is formed between an implanted deep n-well region and the handle wafer substrate, and is connected to the source of the reset FET residing on the SOI layer by a tungsten via plug. The bottom of the handle-wafer is biased to a large reverse-bias (~-30V), while the top

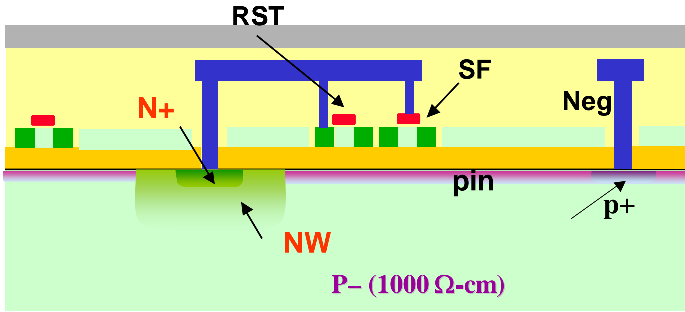

Figure 1: Schematic cross-section of an SOI imager pixel

of diode (the n+ contact tied to the deep n-well) has voltage excursions (~1-2V) that are within the permissible voltage limits of the fabrication technology. A pinning implant layer (appropriately biased) holds the interface between the buried oxide and the handle wafer silicon in equilibrium, preventing surface dark current generation.

Figure 2 shows the detailed cross-section of the diode in the handle-wafer and the required potential profiles. In order to minimize dark current, the surface is kept in accumulation by adding a boron implant acting as pinning layer, biased at a small negative voltage. In order to prevent ohmic conduction between the pinning layer and the bottom of the handle wafer – the voltage difference between the two being close to 30V, a barrier is placed in the vertical direction, as shown schematically in figure 2. The barrier is created by pinching off a region between the two adjacent n-wells, achieved by appropriately spacing the two n-wells as well as by tailoring the doping profiles of the pinning layer and the deep n-well (called field-shaping in figure 2). The pinch-off region results in a local potential maxima (a "crest") in the vertical direction, and a local potential minima in the horizontal direction (a "trough"). The potential trough prevents coupling of field lines from one deep n-well to its adjacent one, preventing intra-pixel capacitance and capacitive cross-talk, as shown in the simulated potential distribution in

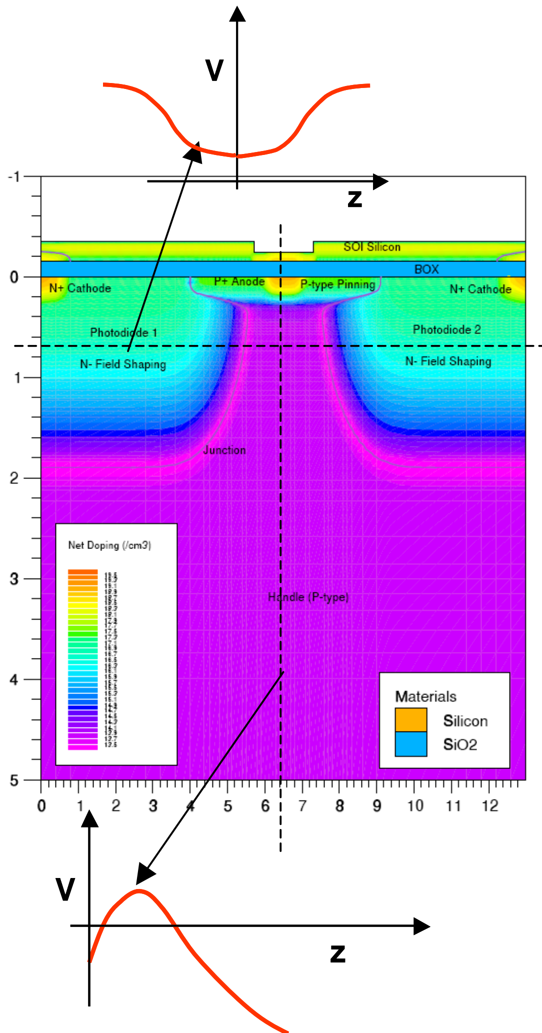

Figure 2: Simulated cross-section of the pixel and the required potential profiles

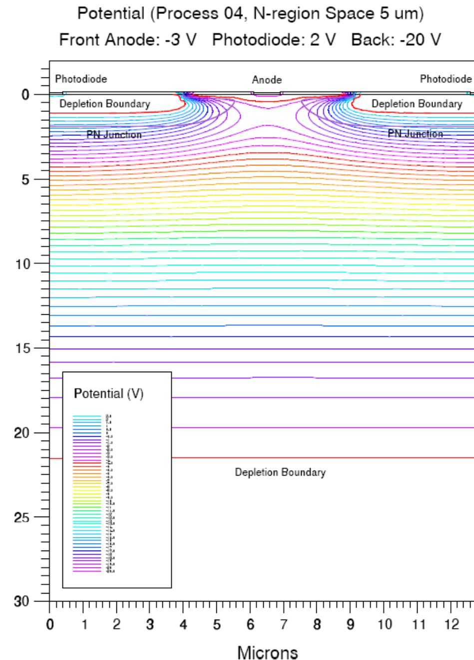

Figure 3: Simulated potential distribution in the handle-wafer diode

figure 3.

The spacing between the adjacent n-wells and their implant conditions are carefully tailored to achieve the pinch-off condition for all pixels – pinch-off condition being essential to prevent ohmic conduction across the handle wafer. The simulated potential distribution across the handle-wafer diode is shown in figure 3. The large back-bias to the handle-wafer is brought in through the front-side by using an

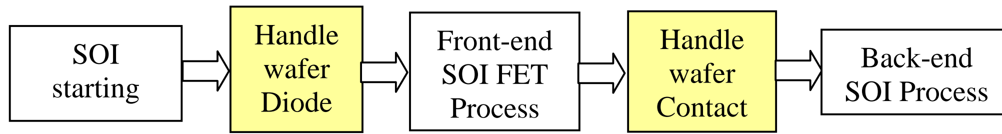

Figure 4: Modular process flow schematic block diagram

appropriately spaced p^+ guard-ring structure to prevent Si or SiO_2 breakdown. The guard ring structure also holds the edge of the chip in inversion screening the contaminants in this area and preventing them from affecting the diode behavior.

Figure 4 shows the schematic process flow. The diode process steps are integrated within the standard SOI process flow in a modular fashion to fit within the available thermal budget of the SOI FET process. Since the pinning implant is carried out through the SOI layer, its energy and dose are carefully optimized to provide effective buried oxide surface pinning without affecting the overlaying SOI FET performance.

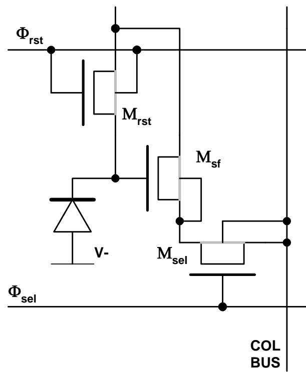

Figure 5: Pixel Schematic

The imager consists of typical “3T” CMOS APS pixels, each pixel consisting of a handle-wafer diode, and three transistors (M_{sf}, M_{sel}, and M_{rst}) residing in the SOI layer, as shown in the pixel schematic in figure 5. The transistors use a double-gate Flexfet™ [14] structure, featuring a gate trench and a self-aligned back implant, resulting in a compact, planar connections to all four transistor terminals. The back gates of the source follower and the switch FET are tied to the respective sources, eliminating the body-effect, and providing near ideal source follower performance.

The reset switch is also an n-type FET in order to prevent inadvertent forward-biasing of the sense node during reset-switch turn-off. The back gate of the reset FET is connected to the front-gate in order to set the minimum anode potential such that the pinch-off condition is maintained for all illumination conditions.

In addition, this configuration also increases the back-bias of M_{rst}, preventing parasitic conduction in the FET channel, thereby suppressing sense node leakage. Figure 6 shows the layout of the chip, with the inset showing the pixel layout.

A key element of this device is the proper operation of the handle-wafer diode. Before completing the full imager fabrication, a short loop run of the diode array (using the

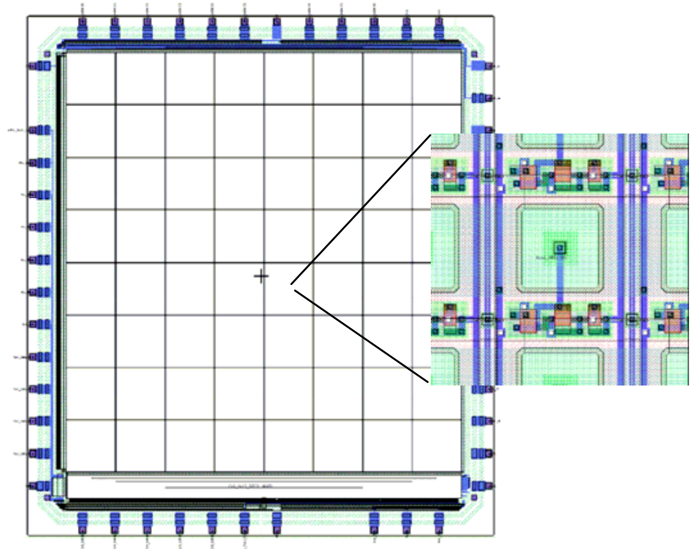

Figure 6: Layout of the 512x512 SOI imager chip, with the pixels shown as an inset

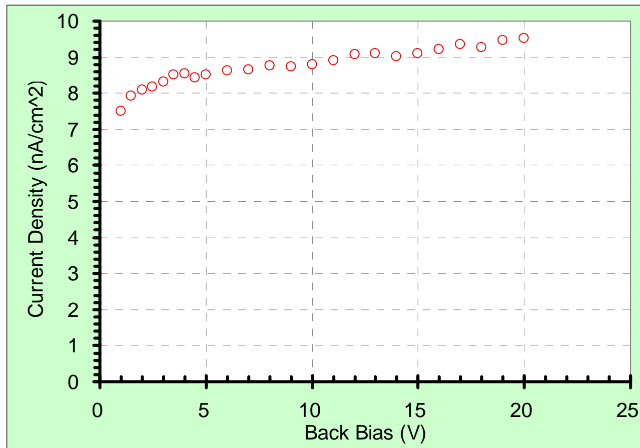

Figure 7: Measured leakage current from handle-wafer diode

same set of masks) was built as a proof-of-concept. Figure 7 shows the measured leakage current from a 10x10 diodes connected in parallel for 4 µm spacing between n-wells. The surface pinning layer is biased to –1V, while the back-bias which is brought to a pad at the chip-edge is swept to reverse-bias the diode from –1V to –20V. Figure 7 shows that the dark current is well-behaved, although somewhat higher than our target.

Most importantly, the dark current does not depend linearly with the back-bias, which would have been the case had the pinch-off not been achieved between the two adjacent n-well diodes. The dark current dependence on back-bias is consistent with the presnce of pinch-off condition between the n-well diodes – a condition that is critical for reducing intra-pixel capacitance and capacitive cross-talk.

The dark current is also thermal in origin, as shown in the Arhennius plot in figure 8. The extracted activation energy is 0.61 eV for a back-bias of 10V, indicating thermal generation within the depletion region.

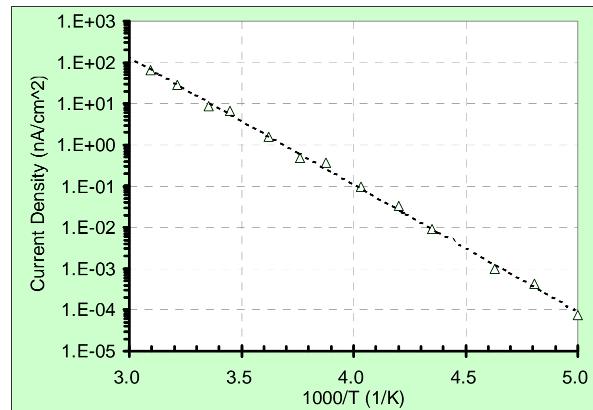

Figure 8: Measured leakage current from handle-wafer diode

Initial measurements of quantum efficiency indicates a value > 60% at 1 µm. These initial results are strongly indicative of the possibility of achieving high-performance large-format monolithic scientific arrays with high NIR QE and low-cross-talk between pixels.

Acknowledgments:

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References:

1. T. Chuh, *Proc. SPIE*, vol. 5783, pp. 907-916, 2005.
2. S. Holland et al., *IEEE Trans. Electron Devices,* vol. 50, pp. 4-11, 2003.
3. R.J. Stover et al. Proc. SPIE vol. 3019, pp. 183-188, 1997.
4. V. Suntharalingam et al., *Tec. Dig. 2005 IEEE Intl. Solid-state Circ. Conf.*, pp. 356-357, 2005
5. Y. Bai et al., *Proc. SPIE*, vol. 5167, pp. 83-93, 2004.
6. A.W. Hoffman et al., *Proc. SPIE*, vol. 5499, pp. 240-249, 2005.
7. J.A. Burns et al., *IEEE Trans. Electron Devices*, vol. 53, pp. 2507-2516, 2006.
8. A. Moore et al., *Proc. SPIE*, vol. 5167, pp. 161-170, 2003.
9. W. Zhang;et.al., *Proc. IEEE Intl. SOI Conference 1999,* pp. 102-103, 1999.
10. X. Zheng et al., *Proc. IEEE Intl. SOI Conference 2000,* pp. 138-139, 2000.
11. L. Bosisio et.al., *Conf. Record IEEE Nuclear Science Symp. and Medical Imaging Conf.*, pp 230-232, 1992.
12. B. Dierickx et al., *IEEE Trans. Nuclear Science,* V40- 4 , pp 753-8, 1992.
13. X. Zheng et al., *Proc. IEEE Intl. SOI Conference 2003,* pp. 101-102, 2003.
14. R. Hayhurst et al. *Proc. IEEE Intl. SOI Conference 2005,* pp. 102-103, 2005.

A 10b Column-wise Two-step Single-slope ADC for High-speed CMOS Image Sensor

Jeonghwan Lee, Seunghyun Lim, and Gunhee Han
Department of Electrical and Electronic Engineering
Yonsei University, 134, Sinchon-dong, Seodaemun-gu, Seoul, Korea
Phone:+82-2-2123-7710, Fax:+82-2-312-4584
Email: jhlee@cad.yonsei.ac.kr

***Abstract*–This paper proposes a column-wise two-step Single-Slope (SS) ADC, which improves the sampling rate while maintaining the architecture of the conventional SS-ADC for high-speed CIS. To remove the problem of missing code in multi-stage structures, occurring on every boundary between steps of the coarse ADC, the range of the fine ADC is doubled to cover the boundary. The sampling rate of the ADC is increased by a factor of 2^{m+n} / ($2^m + 2^{n+1}$) compared to the conventional one. A prototype chip was fabricated in 0.35-µm CMOS process. The proposed ADC has a 10-bit resolution and the sampling rate of 240-kS/s at 25-MHz clock frequency, which has been increased by a factor of 10 compared to the conventional SS-ADC. QVGA imager using the proposed ADC can achieve the theoretical maximum frame rate in excess of 1000-fps with power increase of about 25%.**

I. INTRODUCTION

Recently, applications of CMOS Image Sensor (CIS) extend over not only mobile devices but applications considered as next-generation format such as digital broadcasting using a 2-million-pixel High-Definition Television (HDTV) format with satellite and digital cinemas being reduced for practical use, a 8-million-pixel format [1].

The Single-Slope (SS) ADCs have been widely used for column-wise ADCs in imagers because they provide a significant compromise between frame rate, ADC resolution, power consumption, and extendibility [2]. However, a drawback of the SS-ADC is its conversion time that increases exponentially with the number of bits. A multiple-ramp SS-ADC which improves the conversion time by a factor of 3.3 has been reported [3]. However, it requires several ramp generators and extra circuitry compared to a SS-ADC.

This paper proposes a compact 10-bit two-step SS-ADC, improving the conversion time by about a factor of 10. This paper is organized as follows. In Section II, the principle of two-step SS-ADC and the technique of error correction are described. In section III and IV, experimental results are presented, and conclusions are described at the end.

II. PROPOSED TWO-STEP SINGLE-SLOPE ADC

A. Principle of two-step single-slope ADC

The two-step SS-ADC consists of an m-bit coarse SS-ADC and an n-bit fine SS-ADC using the proposed ramp signal as shown in Fig. 1. The first ramp signal for quantizing m-MSBs has 2^m steps in the full-scale range. The second ramp signal for quantizing n-LSBs has 2^n steps. The n-LSBs, however, range only a single step of the coarse ADC. The ADC needs only (2^m+2^n) clocks per sample while the conventional requires 2^{m+n} clocks per sample.

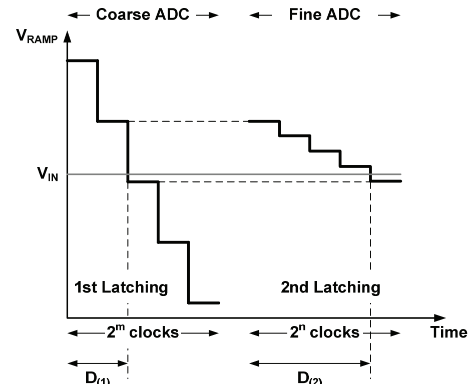


Fig. 1. Ramp signal of two-step SS-ADC.

The conventional ADC with Correlated Double Sampling (CDS) method is composed of a counter, a ramp generator, a comparator, switches and capacitors as illustrated in Fig. 2.(a) [4]. In addition to the conventional ADC, the two-step ADC requires only a few extra circuitries: a capacitor C_H, three-switches (S_{ADC1}, S_{ADC2}, FB_{SW}) and a SYNC block. A ramp signal is coupled via switch FB_{SW} to the positive input of the comparator (V_{COMP}) and via switch S_{ADC2} to the capacitor. Switch S_{ADC1} couples the capacitor to reference voltage (V_{REF}). V_{REF} is given by

$$V_{REF} = V_{RAMP0} - \Delta V_{LSB.1} \qquad (1)$$

where V_{RAMP0} is the initial value of ramp signal and $\triangle V_{LSB.1}$ is a LSB voltage of the coarse ADC.

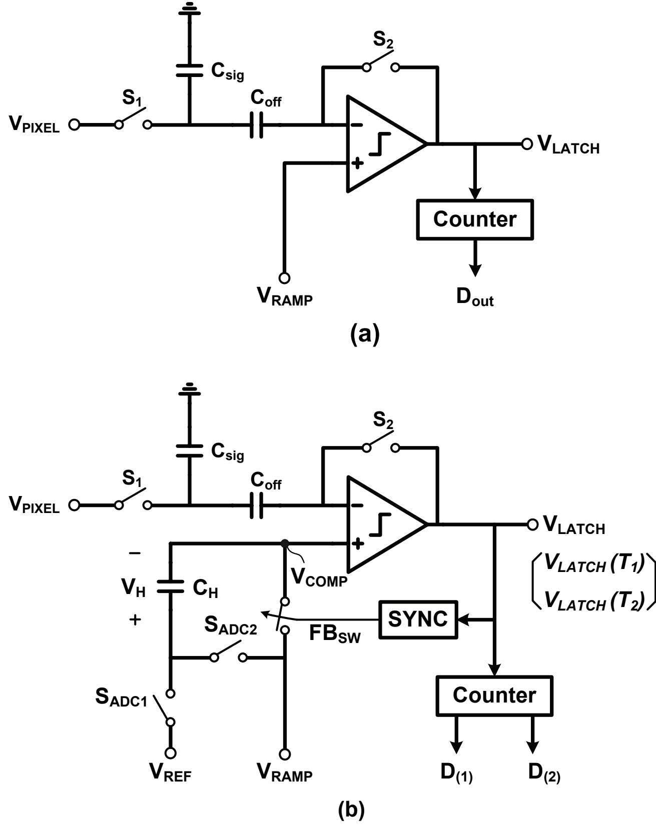


Fig. 2. Architecture of ADC. (a) Normal SS-ADC. (b) Two-step SS-ADC.

As shown in Fig. 3, switch FB_{SW} is on when the 'coarse ADC state' starts, and during the state, switch S_{ADC1} is also on, so that C_H can store the ramp signal ($V_{RAMP}(t)$). The latch signal is generated when $V_{RAMP}(t)$ is lower than V_{IN}, then the output of the counter becomes the result of the coarse ADC ($D_{(1)}$) and switch FB_{SW} is off by the SYNC block. The voltage C_H stores after coarse ADC state is given by

$$V_H = V_{REF} - V_{RAMP}(T_1) \tag{2}$$

where $V_{RAMP}(T_1)$ is the ramp signal at T_1 when the latch signal is generated. Since V_H is the same as the resulting analog voltage of the coarse ADC state, there is a merit that this architecture needs no DAC to find the range for the next 'fine ADC state.'

During the fine ADC state, switch S_{ADC2} is on. When S_{ADC2} is closed, ramp signal is coupled via capacitor C_H to the positive input of the comparator (V_{COMP}), which is given by

$$\begin{aligned} &V_{COMP}(t) \\ &= V_{RAMP}(t) - V_H \\ &= V_{RAMP}(T_1) + \Delta V_{LSB.1} - \{V_{RAMP0} - V_{RAMP}(t)\} \end{aligned} \tag{3}$$

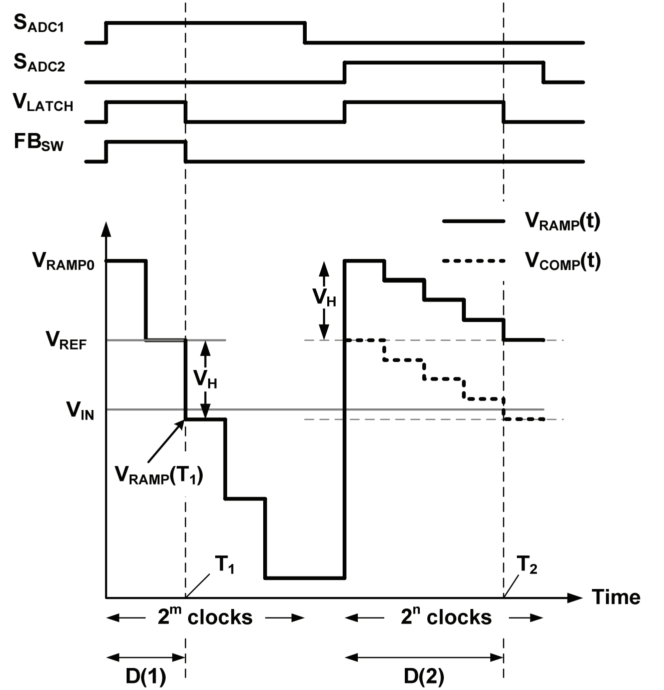


Fig. 3. Timing diagram of two-step SS-ADC.

Since the ramp signal in the state ranges from V_{RAMP0} to ($V_{RAMP0} - \triangle V_{LSB.1}$), V_{COMP} also has the range given by

$$V_{RAMP}(T_1) \leq V_{COMP}(t) \leq V_{RAMP}(T_1) + \Delta V_{LSB.1} \tag{4}$$

Therefore, two inputs of the comparator, V_{IN} and V_{COMP}, are guaranteed to intersect at T_2 as illustrated in Fig. 3. At that time, the latch signal is generated and the output of counter is set to be the result of fine ADC ($D_{(2)}$).

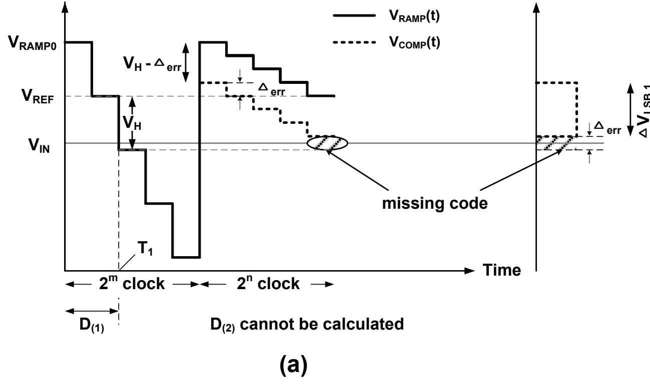
Combining two results of ADC, $D_{(1)}$ and $D_{(2)}$, the total output code of two-step ADC, D_{out}, can be calculated as ($2^n \bullet D_{(1)} + D_{(2)}$) by adding the n-step shifted $D_{(1)}$ and the original $D_{(2)}$.

B. *The technique of error correction*

After the execution of the coarse ADC, the voltage V_H can be disturbed and contain an error ($\triangle$err) from several reasons such as thermal noise, parasitic capacitance, and feed-through. Due to an error, the range of V_{COMP} is shifted as shown in (5).

$$V_{RAMP}(T_1) + \Delta_{err} \leq V_{COMP}(t) \leq V_{RAMP}(T_1) + \Delta V_{LSB.1} + \Delta_{err} \tag{5}$$

In the case, V_{COMP} and V_{IN} fail to intersect. It causes the latch signal not to be generated and makes the problem of missing code. This problem is unavoidable on the boundary in a multi-step structure [3, 5]. Fig. 4.(a) illustrates the range of V_{COMP} with error and V_{IN}. When V_{IN} is in the shadowed region, V_{IN} is not in the range of V_{COMP} any more and $D_{(2)}$ cannot be calculated. Therefore, an error correction technique is necessary in multi-step structures.



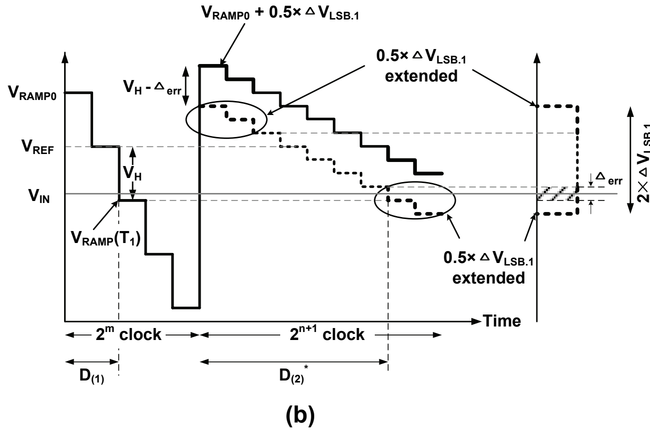


Fig. 4. Error-added ramp signal of two-step ADC. (a) without error correction technique. (b) with error correction technique.

To remove the problem of missing code in two-step ADC structure, the range of the fine ADC should be doubled to cover the boundary between steps of coarse ADC. The ramp signal is modified so that the upper boundary and the lower boundary are expanded $0.5\times\triangle V_{LSB.1}$, on both sides.

$$V_{RAMP0} - 1.5\times\Delta V_{LSB.1} \le V_{RAMP}(t) \le V_{RAMP0} + 0.5\times\Delta V_{LSB.1} \tag{6}$$

The problem of missing code does not occur because the range of V_{COMP} is doubled by (3,6) as shown in (7) and includes the V_{IN}.

$$V_{RAMP}(T_1) + \Delta_{err} - 0.5\times\Delta V_{LSB.1} \le V_{COMP}(t) \le V_{RAMP}(T_1) + \Delta V_{LSB.1} + \Delta_{err} + 0.5\times\Delta V_{LSB.1} \tag{7}$$

Using the error correction technique, the fine ADC output code $D_{(2)}$ is changed to (n+1)-bits due to the expanded range of $2\times\triangle V_{LSB.1}$. The Changed output code, named $D_{(2)}^*$, has a redundant digit. On the other hand, the coarse ADC output code $D_{(1)}$ is equal to that of ADC without the error correction technique. The sampling rate of the ADC is increased by a factor of $2^{m+n} / (2^m + 2^{n+1})$ compared with the conventional SS-ADC. In this principle, the more increased the resolution of the ADC is, the more advantageous the proposed ADC is.

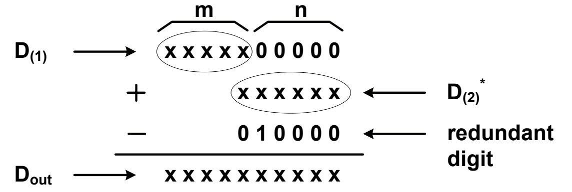


Fig. 5. Calculation of output code.

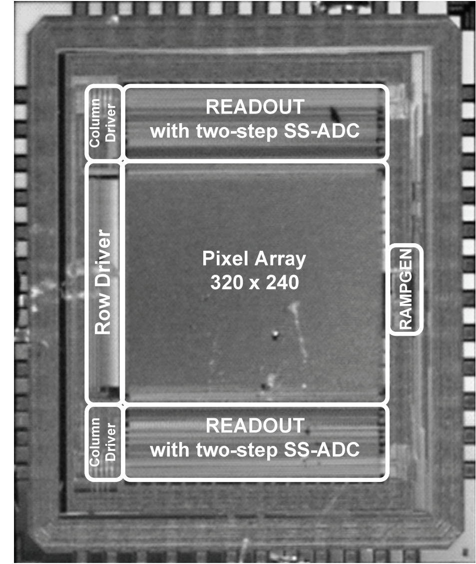


Fig. 6. Chip micrograph.

Combining the redundant digit with $D_{(1)}$ and $D_{(2)}^*$, the total output code of ADC with error correction technique D_{out} can be calculated as $(2^n \bullet D_{(1)} + D_{(2)}^* - 2^{n-1})$ by subtracting the redundant digit from the sum of n-step shifted $D_{(1)}$ and the original $D_{(2)}$ as shown in Fig. 5.

III. Experimental Results

A prototype image sensor shown in Fig. 6 was fabricated in 0.35-µm CMOS process. The pixel array has 320 × 240 pixels, with a pixel pitch of 5.6-µm. Fig. 7 shows measured images and histograms of the prototype imager at 80-fps. It shows that the missing code problem is perfectly resolved using the proposed error correction technique. The performance of the prototype imager is summarized in Table. I. The two-step SS-ADC was implemented with a 5-bit coarse SS-ADC and a 6-bit fine SS-ADC. The proposed ADC has 10-bit resolution and the sampling rate of 240-kS/s at 25-MHz clock frequency. The conversion time of the proposed ADC is 4.2-µs, whereas 40-µs is used for a conventional SS-ADC. The sampling rate of the proposed ADC is increased by a factor of 10 compared with the conventional SS-ADC. With the optimized digital circuitry, QVGA imager for verifying performance of the ADC is able to achieve the theoretical maximum frame rate in excess of 1000-fps.

The power consumption of the analog circuitry is 17.6mW, of which 5.6mW is used by ramp generator and 12mW is used for column readout. Compared with an imager with SS-ADC, the total power consumption is only increased about 25%.

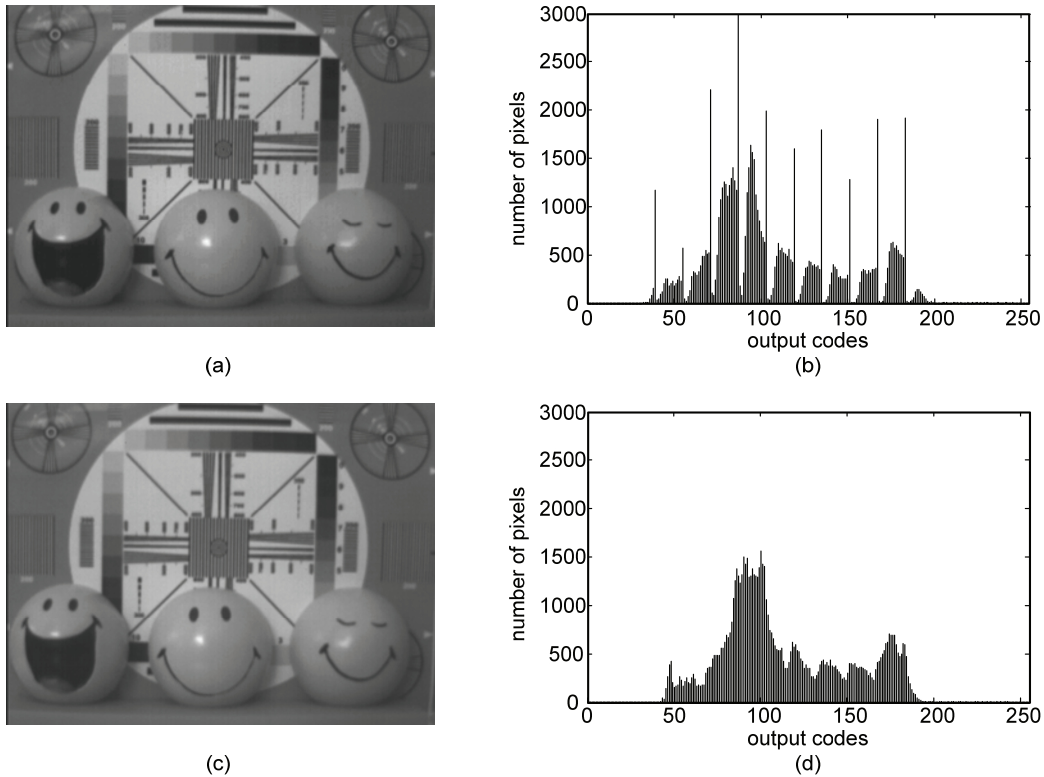


Fig. 7. Measured images and histograms. (a) image without error correction technique. (b) histogram of (a). (c) image with error correction technique. (d) histogram of (c).

TABLE I.
PERFORMANCE SUMMARY.

Technology	0.35 μm CMOS 2P3M
Array Format	320 × 240
Pixel Size	5.6 μm × 5.6 μm
ADC Resolution	10 bits (coarse 5b, fine 6b)
Column FPN	< 0.0837 % (@dark)
Sampling Rate	240 kS/s (@25MHz clock frequency)
Maximum Frame Rate	>1000 fps
Power Supply	2.8 V
Power Consumption (Analog Circuitry)	17.6 mW

IV. CONCLUSIONS

In this paper, a two-step single-slope ADC for high-speed CIS is proposed. A technique of error correction is also presented to remove the problem of missing code in two-step structure. Compared with the single-slope ADC, it improves the sampling rate by a factor of 10 while increasing only a quarter of the total power consumption. The proposed two-step SS-ADC can be used for high-resolution, high-speed image sensors with reasonable power consumption such as HDTV and scientific measurement applications.

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REFERENCES

[1] I. Takayanagi, M. Shirakawa, K. Mitani, M. Sugawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, “A 1.25-inch 60-Framesps 8.3-M-Pixel Digital-Output CMOS Image Sensor,” *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2305-2314, Nov. 2005.

[2] S. Ham, W. Jung, D. Lee, Y. Lee, and G. Han, “Ramp Slope Built-in-Self-Calibration Scheme for Single-Slope Column Analog-to-Digital Converter Complementary Metal－Oxide－Semiconductor Image Sensor,” *Japanese Journal of Applied Physics*, vol. 45, no. 7, pp. L201−L203, Feb. 2006.

[3] M. F. Snoeij, P. Donegan, A. J. P. Theuwissen, K. A. A Makinwa, J. H. Huijsing, “A CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC,” in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. papers*, San Francisco, CA, Feb. 2007, pp. 506-507.

[4] S. Lim, J. Cheon, S. Ham and G. Han, "A New Correlated Double Sampling and Single Slope ADC Circuit for CMOS Image Sensors," in *Proc. Int. SoC Design Conf.*, Seoul, Oct. 2004, pp. 129-131.

[5] P. Figueiredo, P. Cardoso, A. Lopes, C. Fachada, N. Hamanishi, K. Tanabe, J. Vital, “A 90nm CMOS 1.2V 6b 1GS/s two-step subranging ADC," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. papers*, San Francisco, CA, Feb. 2006, pp. 568-569.

Pixel-level A/D conversion: comparison of two charge packets counting techniques

A. Peizerat, M. Arques, P. Villard, J-L. Martin
CEA/LETI - MINATEC
Grenoble, France
arnaud.peizerat@cea.fr

***Abstract*— A comparison between two techniques for pixel-level ADC in CMOS image sensors is presented. As the charge represents accurately the amount of illumination, the principle of both techniques consists in counting small charge packets which come from the detector. Based on a 0.13 µm CMOS technology, simulation results and first measurements are presented showing that the LSB value can be reduced to 1900 electrons with a static power of 250nW per pixel. For the moment, due to the technology available, this technique is restricted to medium size pixels, i.e. 50x50 µm² or 25x25 µm² when the fill factor is close to 100%.**

I. Introduction

Pixels of an image sensor are composed of two parts: the detector, which converts incident photons energy into electron-hole pairs, and the readout electronics, which converts these electron-hole pairs into a readable signal. In the conventional Active Pixel Sensor (APS), this signal is an analog voltage drop which is transferred off-chip, since the detector current discharges the integration capacitor (C_{INT}). Because reliability and performance are always an issue, and also because of the evolution of technology, the Analog-to-Digital Conversion (ADC) tends to be integrated into the CMOS image sensor. The purpose of a pixel-level conversion, in comparison to chip or column-level ADC, is first, power reduction, thanks to a lower conversion frequency, and second, noise reduction, because analog multiplexing is suppressed [1]. The main constraint is, in fact, the limited pixel area.

Several papers suggest different methods for pixel-level ADC. A 1st order $\Delta\Sigma$ approach with multiplexed pixels [2] shows a 7-bit resolution but requires off-chip decimation filtering. The MultiChannel bit-Serial (MCBS) technique [3], which associates the single-slope ADC concept with the Gray-code quantization, is very efficient for small pixels, but the resolution obtained is of 8 bits only. With separate MSB and LSB conversions [4], a 12-bit resolution is reached but linearity is affected. An ASIC for medical applications [5] presents good performance but the LSB value of the ADC is too large because of the application specifications. Inspired by those papers, we present here a comparison between two techniques, which we call "voltage reset technique" and "charge reset technique". In both techniques, a pixel-level ADC is performed with a low LSB value, good linearity, and high resolution.

II. First Approach of the Two Techniques

The common principle which consists in counting charge packets coming from the detector is also called charge-balancing technique [6]. As illustrated in Fig. 1, I_{DET}, created by the illumination, discharges C_{INT} until V_{INT} crosses V_{TH}, then the comparator commands the injection of Q_0 at the integration node and the counter (not drawn on the figure) is incremented by one. At the end of integration time, the counter contains the number N. Since the LSB value of the A/D conversion is Q_0, $N.Q_0$ has been detected. The only difference between the two techniques is the way Q_0 is generated. In the "voltage reset" case, $Q_0=C_{INT}.\Delta V$ and so the LSB is highly dependent on V_{TH}. This technique is thus very sensitive to the performance of the comparator but allows an efficient layout. In the "charge reset" case, Q_0 is generated by a charge injector, thus it relaxes constraints on the comparator and on C_{INT} precision, providing the charge injector has good performance.

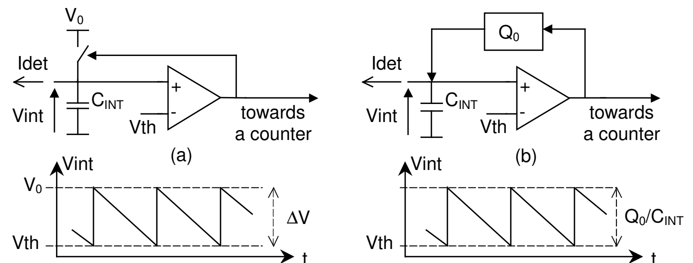


Figure 1. principles of the two techniques (a) voltage reset technique and (b) charge reset technique, assuming I_{DET} is constant

For these two techniques, you can trade off the number of bits against the conversion time which depends on the frame rate. In other words, with twice the integration time and one more flip-flop in the counter, the dynamic range is doubled. That's the reason why it is particularly appropriate to discuss the LSB value, Q_0 , which is not dependent on the conversion time. Indeed the performance of the conversion is given by the properties of Q_0.

III. VOLTAGE RESET TECHNIQUE DESIGN

Since $Q_0=C_{INT}.\Delta V$, this technique is sensitive to C_{INT} and ΔV variations. ΔV variations can be due to threshold voltage variations (V_{TH}) or reference voltage variations (V_0).

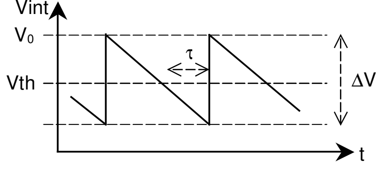


Figure 2. Influence of the delay (τ) of the comparator when $I_{DET}>Q_0/\tau$

Considering the comparator as a first order lowpass filter with a time constant τ , the effective threshold seen by V_{INT}, Fig. 2, is given by:

$$V_{TH_eff} = V_0 - V_{TH} + \tau.I_{DET}/C_{INT} \quad (1)$$

As a result, Q_0 varies depending on the value of I_{DET}, the linearity error of the A/D conversion is then:

$$\frac{\Delta Q_0}{Q} = \frac{\tau \cdot I_{DET}/C_{INT}}{V_0 - V_{TH}} \quad (2)$$

Considering the input referred noise e_n of the comparator and the thermal noise introduced by the reset switch, Q_0 varies at each reset. So, assuming that the reset noises are not correlated with one another, the standard deviation $\sigma_{READOUT_e-}$ (in electrons), at the end of integration time can be written as:

$$\sigma_{READOUT_e-} = \frac{1}{q} \cdot \sqrt{N \cdot C_{INT}^2 e_n^{\ 2} + N \cdot kTC_{INT}} \quad (3)$$

where q is the charge of a single electron, k the Boltzman's constant and T the temperature.

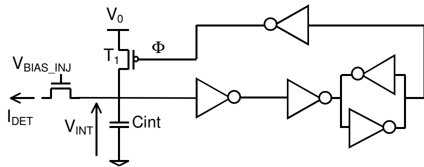


Figure 3. Schematic of a pixel

In our design, Fig. 3, we chose the smallest value for C_{INT} in order to minimize $\sigma_{READOUT_e-}$. For that purpose, a common gate (or direct injection) transistor, T_{INJ}, is used in saturation or weak inversion region to make sure C_{INT} is not dependent on C_{DET}, the capacitance of the detector. This means that C_{INT} can be as small as possible, i.e., a parasitic capacitor. Of course, this implies that an I_{DET} -dependent pole is introduced. Suppose T_{INJ} in weak inversion, then the value of that pole is:

$$p = \frac{q}{n.k.T} \cdot \frac{I_{DET}}{C_{DET}} \quad (4)$$

where n is the ideality factor (≈1.2 for the process we use). That restriction has to be taken into account if the conversion time specification is very severe.

Fig. 3, the comparator is composed of a simple CMOS inverter and a trigger circuit. The CMOS inverter exhibits a good trade-off between bandwidth and power consumption. The trigger circuit introduces hysteresis and high gain to ensure noise immunity during the decision step and to prevent metastability.

IV. CHARGE RESET TECHNIQUE DESIGN

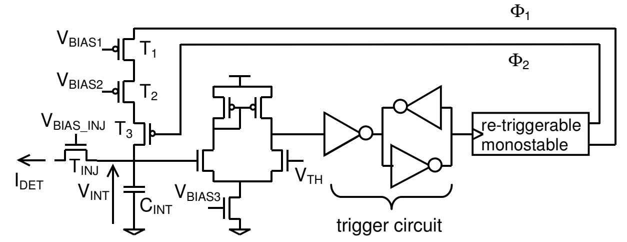


Figure 4. Schematic of a pixel

Fig. 4, the scheme of this technique is very similar to that of the voltage reset technique. Since Q_0 is not dependent on V_{TH} variations, the use of a differential pair with poor bandwidth but without big current spikes is possible. The trigger has the same function as previously.

When the output of the trigger circuit falls, a monostable circuit creates two pulses, Φ1 and Φ2, which control the charge injector (T1, T2 and T3) whose scheme is borrowed from CCD technology. Fig. 5, while Φ2 is high, Φ1 first fills the potential well formed by T1 and T2 with charges (Φ1 = '1') and then the charges are spilled out of the potentiel well (Φ1 = '0'). A certain amount of charges, Q_0, is thus stored under the gate of T2. Assuming that overlap and junction capacitors are negligible:

$$Q_0 = C_{OX}.W_{T2}.L_{T2}.(V_{BIAS1} - V_{BIAS2}) = C_{INJ}.(V_{BIAS1} - V_{BIAS2}) \quad (5)$$

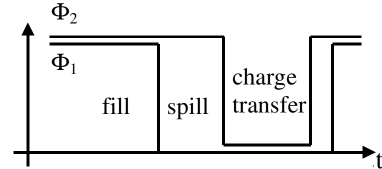


Figure 5. Timing diagram of Φ1 and Φ2

Then, when Φ2 falls, this amount of charges Q_0 is transferred onto the capacitor of the integration node. Fig 6 illustrates, thanks to a potential well representation, the different charge flows.

Both signals, Φ1 and Φ2, can be chosen to control the counter.

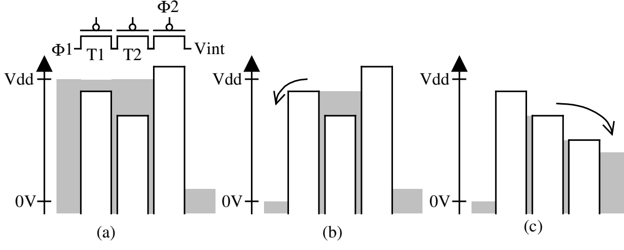


Figure 6. The different charge flows (a) the fill step, (b) the spill step and (c) the charge transfer step

For a given C_{INT}, the smaller Q_0 is, the lower the ΔV (= Q_0 / C_{INT}) will be each time the charge reset appears on the integration node, the worst option being that the comparator might not return to its waiting state because of the delay of the comparator (Fig. 7). The condition of this worst option can be expressed as:

$$I_{DET} > Q_0 / \tau \quad (6)$$

where τ is the delay of the comparator.

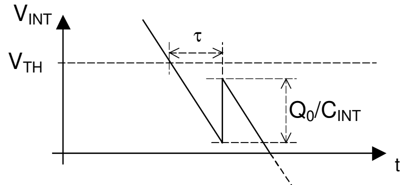


Figure 7. Influence of the delay (τ) of the comparator when $I_{DET}>Q_0/\tau$

This problem can be solved by the use of a retriggerable monostable circuit. If the comparator does not switch back after a charge injection, the circuit automatically re-triggers after a period τ_{MONO} lower than τ, the delay of the comparator. As shown in Fig. 8, it guarantees a good functionality until saturation when I_{DET} reaches the limit:

$$I_{DET} > Q_0 / \tau_{MONO} \quad (7)$$

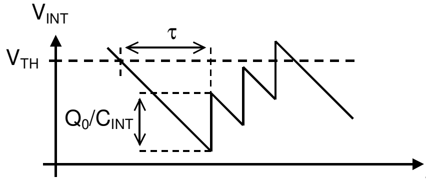


Figure 8. Waveform of V_{INT} when the monostable circuit re-triggers

For the calculation of noise, let's consider, as in the previous section, that the reset noises are not correlated with one another, then the standard deviation $\sigma_{READOUT_e-}$, at the end of integration time can be written as :

$$\sigma_{READOUT_e-} = \frac{1}{q} \cdot \sqrt{C_{INT}^2 {e_n}^2 + N \cdot kTC_{INJ}} \quad (8)$$

where N is the number of charge resets and C_{INJ} is defined in (5). Compared to (3), the influence of e_n is negligible (except for great value of C_{INT}) because it does not increase with N. One can also note that the reset noise is not dependent on C_{INT} but on C_{INJ}, the capacitance of the charge injector.

V. Simulation Results

The results concern one pixel of each technique without the counter. The circuit was designed using a 0.13 µm process with 1.2 V power supply voltage. Integration time was set to 2 ms and the maximum I_{DET} to 5 nA (I_{DET_MAX}). So the maximum detected charge is 10 pC (Q_{MAX}). Given that the LSB value is 2000 electrons or 0.35 fC (Q_0), the resolution reached is slightly lower than 15 bits. The overall characteristics are summarized in Table 1.

Note that the noise results are expressed as the ratio of $\sigma_{DETECTOR_e-}$ by $\sigma_{READOUT-e-}$. Indeed $\sigma_{READOUT_e-}$ has to be compared to the RMS detector noise present at the input of the converter. Assuming that the detector is a photodiode, the noise is a conventional shot noise, and its standard deviation ($\sigma_{DETECTOR_e-}$), in electrons, is :

$$\sigma_{DETECTOR_e-} = \sqrt{I_{DET}\, T_{INT} / q} \quad (9)$$

In the case of a detector with a quantum efficiency, η, above one (e.g. detection of high energy photons), its standard deviation ($\sigma_{DETECTOR_e-}$), in electrons, becomes:

$$\sigma_{DETECTOR_e-} = \sqrt{\eta \cdot I_{DET}\, T_{INT} / q} \quad (10)$$

The ratio $\sigma_{DETECTOR_e-}/\sigma_{READOUT_e-}$ is then improved by $\sqrt{\eta}$.

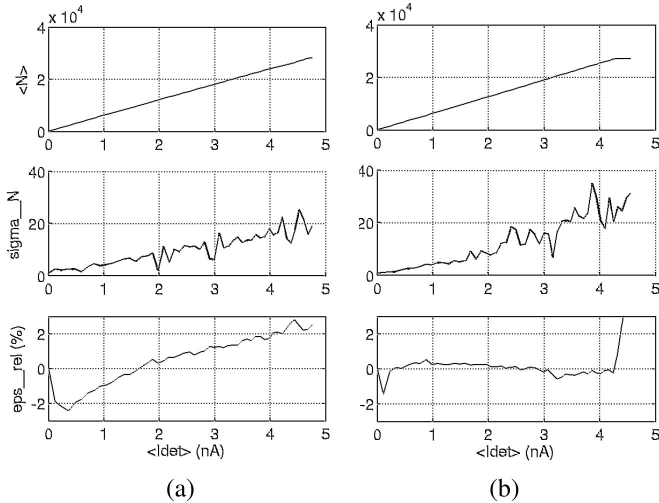
TABLE I. Summary of simulation results for 2 ms integration time

	Voltage reset	**Charge reset**
Idet range	[5 pA; 5 nA]	[5 pA; 5 nA]
LSB (electrons)	2000	2000
Linearity (over Idet range)	2%	0.2%
Noise ($\sigma_{DETECTOR_e-}/\sigma_{READOUT_e-}$)	3.4 @ 5nA	1.7 @ 5nA
Layout (w/o the counter)	8µm x 6µm	22µm x 12µm
Power (µW)	0.2 @ 5pA 1.4 @ 5nA	0.2 @ 5pA 1.5@ 5nA

VI. Experimental Results

A test-circuit was fabricated in a 0.13 µm process with 1.2V power supply voltage. As the objective was more to validate these pixel-level ADC techniques rather than to

realize an image sensor, this test chip only contains a few pixels. Each pixel is composed of the structure in Fig. 3 or Fig. 4, plus buffers and a photodiode acting as a low noise current source. The test consists then in lightening the chip with a LED and counting the generated pulses by software methods. For a given LED current, several acquisitions are carried out so as to extract the mean (<N>), the standard deviation (sigma_N) and the linearity (eps_rel) of the number of counted pulses. The curves of Fig. 9 give the evolutions of these features with the current I_{DET} measured by an on-chip reference-pixel.



(a) (b)

Figure 9. Mean, standard deviation and linearity error of N as a function of I_{DET} (a) for the voltage reset technique and (b) for the charge reset technique. N is the number of charge injections during 2 ms

TABLE II. SUMMARY OF EXPERIMENTAL RESULTS FOR 2 MS INTEGRATION TIME

	Voltage reset	**Charge reset**
Idet range	[5 pA; 4 nA]	[5 pA; 4 nA]
LSB (electrons)	1900	1900
Linearity (over Idet range)	4%	0.4%
Noise ($\sigma_{DETECTOR_e-}/\sigma_{READOUT_e-}$)	0.3 @ 4nA	0.1 @ 4nA
Power (µW)	0.25 @ 4pA 1.8 @ 4nA	0.25 @ 4pA 1.9@ 4nA

Experimental results are close to simulation results except for noise performance. Indeed noise is one order of magnitude larger than expected. Fig. 10 illustrates an experiment which consists, for the "charge reset" technique, in observing N (the number of counted pulses during Tint) over a large period of time. The presence of steps is an unexpected phenomenon. Those steps occur for the two techniques and their magnitude strongly depends on the chip being tested. The "worst" chips in our batch of 25 can show a ratio of 1% between the magnitude of the steps (ΔN) and the absolute value (N). Those technological fluctuations and a ΔN/N of 1% indicate that this phenomenon could be due to RTS (Random Telegraph Signal) noise. We are currently working on design solutions even if electrical simulators do not include RTS noise for the moment.

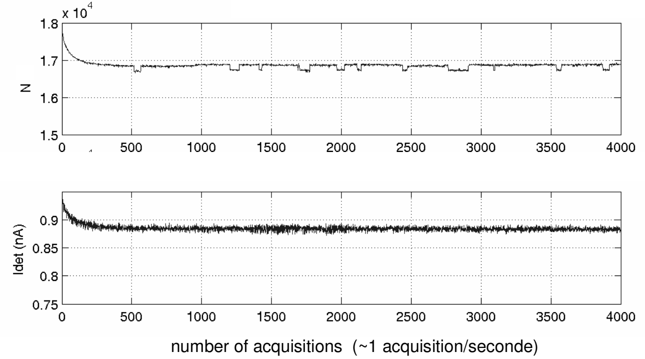


Figure 10. Measured results and apparition of steps when observing N (here for the charge reset technique) over a large period of time. T_{INT}=2ms, one acquisition lasts one second.

VII. CONCLUSION AND FURTHER RESEARCH

Two pixel-level ADC techniques have been developed achieving a 15-bit resolution over a 2 ms integration time, with good linearity and a very small LSB. The voltage reset version has a more efficient layout implementation and the charge reset version shows high linearity. For the moment, due to the technology available, these techniques are restricted to medium size pixels, i.e. 50x50 µm2 or 25x25 µm2 when the fill factor is close to 100%.

Noise reduction and dynamic range (DR) enhancement are subjects for further research. A 120 dB DR is expected at the cost of a reduced fill-factor.

REFERENCES

[1] B. Pain and E. R. Fossum, "Approaches and analysis for on-focal-plane analog-to-digital conversion," SPIE, vol. 2226, 1994, pp. 208-218.

[2] D. Yang, A.E. Gamal and B. Fowler, "A 128x128 pixel cmos area image sensor with multiplexed pixel-level A/D conversion," IEEE, Custom IC Conference, 1996, pp 303-306.

[3] D. Yang, A.E. Gamal and B. Fowler, "A nyquist-rate pixel-level ADC for CMOS image sensor," IEEE, JSSC, 1999, pp 348-356.

[4] J. RHEE and Y. JOO,. "Wide dynamic range CMOS image sensor with pixel level ADC," IEE, Electronics Letters, Vol. 39, No. 4, Feb. 2003, pp. 360-361.

[5] G. Mazza, R. Cirio, M. Donetti, A. La Rosa, A. Luparia, F. Marchetto and C. Peroni, "A 64-channel wide range charge measurement asic for strip and pixel ionisation detectors," IEEE, Transactions on Nuclear Science, Vol. 52, No. 4, Aug. 2005, pp. 847-853.

[6] P. Horowitz and W. Hill, The Art of Electronics, 2nd edition, Cambridge University Press, 1980, pp. 626-629.

[7] G. Grandbois and T. Pickerell, "Quantized feedback takes its place in analog-to-digital conversion," Electronics, October 1977.

Three-Dimensional Integration Technology for Advanced Focal Planes*

Craig Keast, Brian Aull, Jim Burns, Chenson Chen, Jeff Knecht, Brian Tyrrell, Keith Warner, Bruce Wheeler, Vyshi Suntharalingam, Peter Wyatt, and Donna Yost. keast@LL.mit.edu, 781-981-7884
Lincoln Laboratory, Massachusetts Institute of Technology, 244 Wood Street, Lexington, MA 02420

Introduction

Over the last several years MIT Lincoln Laboratory (MIT-LL) has developed a three-dimensional (3D) circuit integration technology that exploits the advantages of silicon-on-insulator (SOI) technology to enable wafer-level stacking and micrometer-scale electrical interconnection of fully fabricated circuit wafers[1].

Advanced focal plane arrays have been the first applications to exploit the benefits of this 3D integration technology. The massively parallel information flow present in 2D imaging arrays maps very nicely into a 3D computational structure as information flows from circuit-tier to circuit-tier in the z-direction. To date, the MIT-LL 3D integration technology has been used to fabricate four different focal planes including: a 2-tier 64 x 64 imager with fully parallel per-pixel A/D conversion[2]; a 3-tier 640 x 480 imager consisting of an imaging tier, an A/D conversion tier, and a digital signal processing tier; a 2-tier 1024 x 1024 pixel, 4-side-abutable imaging module for tiling large mosaic focal planes[3]; and a 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array, using a 30 volt APD tier, a 3.3 volt CMOS tier, and a 1.5 volt CMOS tier[4]. This last focal plane is an excellent example of one of the principal strengths of the 3D integration technology—the ability to integrate the best technology for the desired function within each tier of the circuit stack.

This talk will provide a brief overview of MIT-LL's 3D-integration process, and discuss some of the focal plane applications where the technology is being applied including a mixed material short-wave infrared (SWIR) focal plane array.

3D Technology

3D focal planes and circuits are fabricated by transferring and interconnecting fully fabricated 150-mm SOI substrates to a base wafer. The base wafer can be a high fill factor detector wafer or another circuit wafer and does not have to be a SOI substrate. The assembly process and a 3D chip consisting of three tiers are shown in Figure 1. Each functional section is labeled a tier, in a 3D system of n tiers, and consists of the interconnect and active devices. Tier 2 is transferred to the base tier, tier 1, after face-to-face infrared alignment, and oxide-oxide bonding at 150-275°C. The handle silicon of a transferred tier is removed by grinding the silicon to a thickness of ~50 µm followed by a silicon etch in a 10% TMAH solution at 90 °C. Since the ratio of silicon to BOX etch rates in TMAH is 1000:1, the handle silicon is removed without attacking the BOX and without introducing a thickness variation in the transferred tier, a factor that is essential when forming the vertical connections, or 3D vias. For this reason all circuits to be transferred are fabricated with SOI substrates. Then 3D vias are patterned and etched through the BOX and deposited oxides to expose metal contacts in both tiers. The fully depleted SOI (FDSOI) transistors are mesa isolated and the 3D vias are defined and etched through existing dielectric regions in the field, so that lining the vias with a deposited dielectric is not required to achieve insulation between the vertical connections. The 3D vias are then filled with damascene tungsten plugs planarized by chemical mechanical polishing (CMP) to electrically connect the two tiers. A third tier, tier 3, can then be added to the tier 1-2 assembly using the same processes, except that the front side of tier 3 is bonded to the BOX of tier 2, and 3D vias connect the top-level metal of tier 3 to the first-level metal of tier 2. The 3D chip is shown after bond pads are etched to expose the back of the first-level metal for probing and wire bonding. If the 3D chip is a digital circuit, the bond pads are etched through the BOX and deposited oxides of tier 3. If it is a back-side-illuminated imager, tier 1 is a detector wafer in which photodiodes were fabricated. An additional transfer to a carrier wafer is then required, and bond pads are etched after thinning the back side of the detector wafer to tune the detector layer to the required optical absorption. The cross-sectional scanning electron micrograph (SEM) of a three-tier ring oscillator shown in Figure 2 illustrates interconnections between tiers and the compactness possible with the 3D technology. Figure 3 shows some of the new technology developments including stacked 3D vias, and scaled 3D vias. In its current form the 3D integration technology can support ~1-µm-diameter 3D-vias on a 3.4 µm pitch. Of the three enabling technologies for 3D integration (precision wafer-to-wafer overlay, low temperature oxide bonding, and high-density 3D vias) it is the wafer-to-wafer overlay tolerance that has the largest impact on 3D via pitch. Figure 4 shows typical wafer-to-wafer overlay data for the precision alignment tool designed and fabricated at MIT-LL. This tool routinely provides a 0.5 µm (3σ) overlay tolerance on fully fabricated 150-mm-diameter wafer pairs.

Focal Plane Applications of 3D Technology

The 3D technology has been used to fabricate several different focal planes at MIT-LL. Figure 5 shows the image of a 4-side-abuttable, 1024x1024, 8µm-pixel pitch, 100% fill factor visible focal plane. This design enables the construction of large focal plane arrays with minimal (~3 pixel) seam loss.

Figure 6 shows and a 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array, using a 30 volt APD tier, a 3.3 volt CMOS tier, and a 1.5 volt CMOS tier.

Figure 7 shows the application of the 3D integration technology to a 150-mm-diameter InP wafer. A SOI CMOS circuit layer was successfully transferred and interconnected with perfect yield to a metal landing pad on the compound semiconductor wafer. Building on this demonstration, MIT-LL is working on a 3D-integrated SWIR focal plane array using an InGaAs detector wafer.

Summary

A three-dimensional circuit integration technology based on silicon-on-insulator layer transfer and micron-scale 3D interconnects has been developed. The 3D technology allows two or more different process technologies to be stacked and interconnected enabling complex focal architectures with ideal fill-factors and a broad range of spectral sensitivities.

* *This work was sponsored by the Defense Advanced Research Projects Agency under U.S. Air Force contract FA8721-05-C-0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the Department of Defense.*

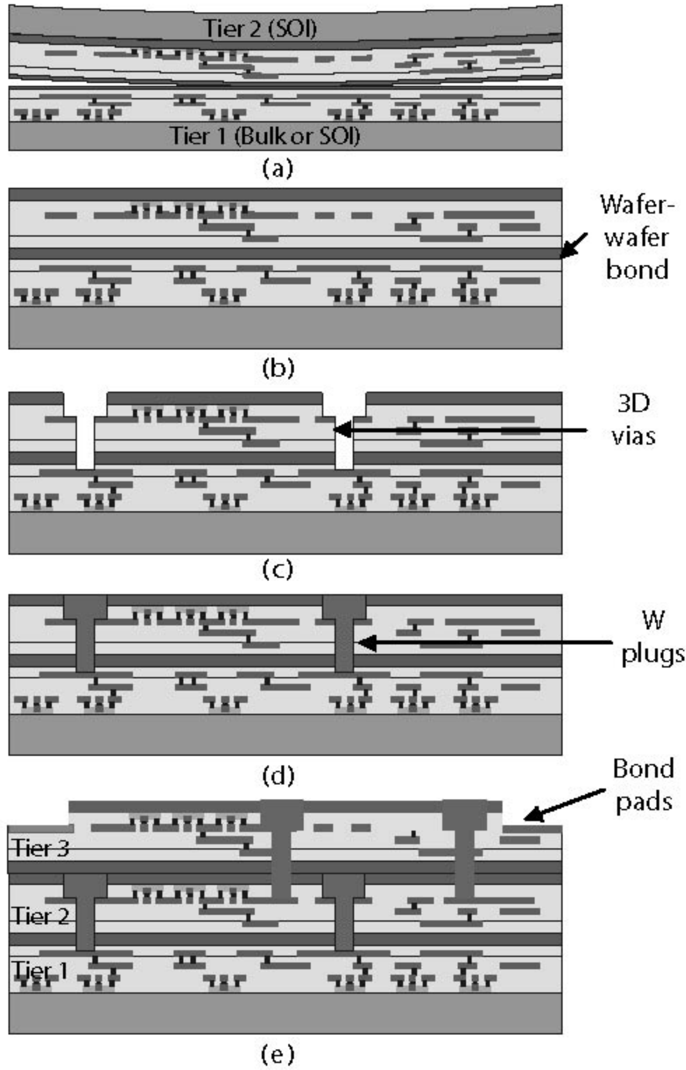


Figure 1. Assembly process for a 3D chip: (a) Two completed circuit wafers are planarized, aligned, and bonded face to face; (b) the handle silicon is removed; (c) 3D vias are etched through the deposited BOX and the field oxides; (d) tungsten plugs are formed to connect circuits in both tiers; and (e) after tier 3 is transferred, bond pads are etched through the BOX for testing and packaging.

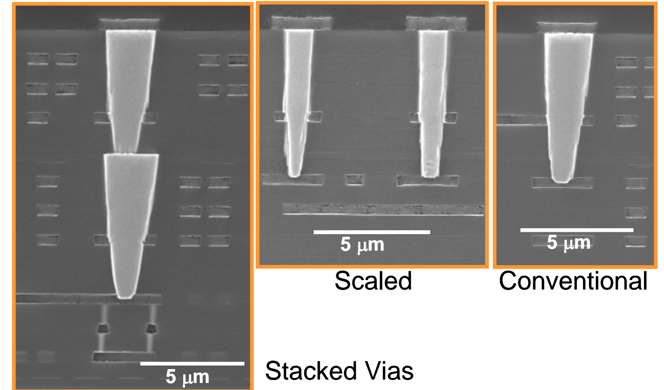


Figure 3. Cross-sectional SEM images of 3D-vias used in the 3D interconnect technology. On the left are stacked 3D-vias which can be used to provide a direct connection from the top-most tier to the bottom-most tier (tier-3 to tier-1 in this case). These metal plugs can also double as thermal vias to carry heat out of the 3D-stack for high performance circuit applications. The two images on the right show a conventional sized 3D-via next to the scaled via now being implemented in the MIT-LL technology. This via (~1-µm-diameter via) can support 3D-via pitches of 3.4 µm.

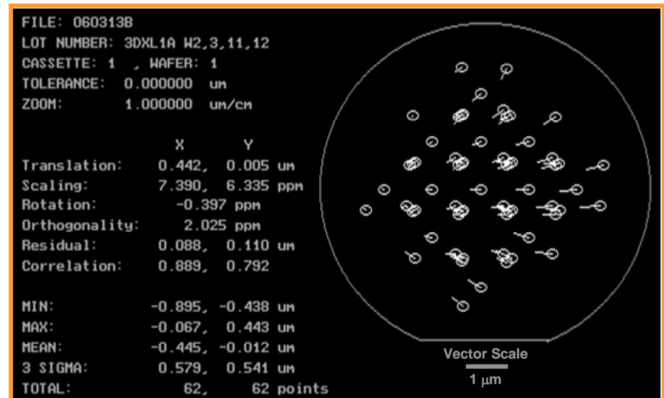


Figure 4. Wafer-to-wafer overlay tool measurement of two fully processed and 3D-interconnected 150-mm-diameter circuit wafers. Typical overlay tolerances of 0.5 µm (3σ) are obtained with the MIT-LL precision aligner/bonder. Wafer-to-wafer overlay is the principal factor determining 3D-via pitch.

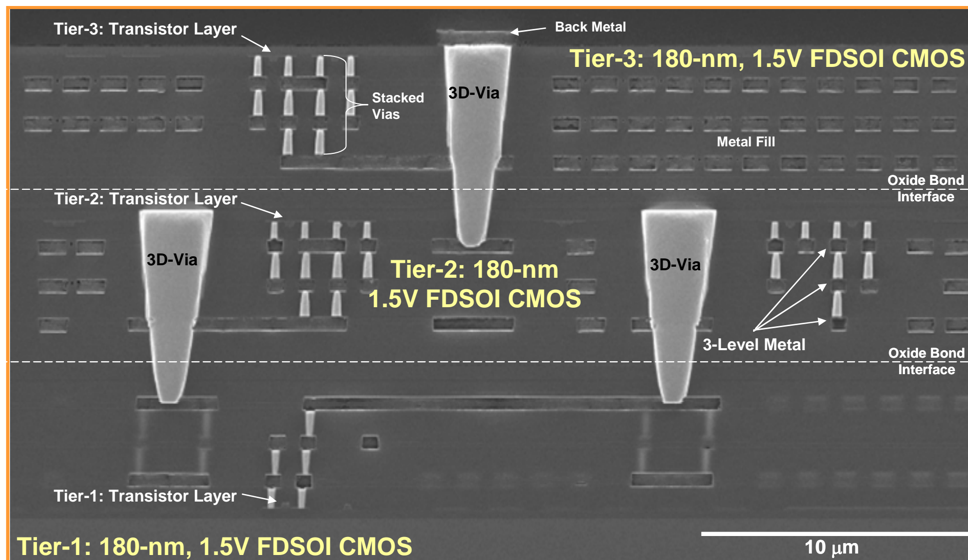


Figure 2. Cross-sectional SEM of a functional three-tier ring oscillator circuit designed to test all three active transistor tiers and all ten metal interconnect layers. The tiers are bonded and interconnected with tungsten plug 3D-vias; the conventional interlevel connections are seen in in each of the 3 FDSOI tiers. Note that the 3D vias are located in the isolation (field) region between transistors.

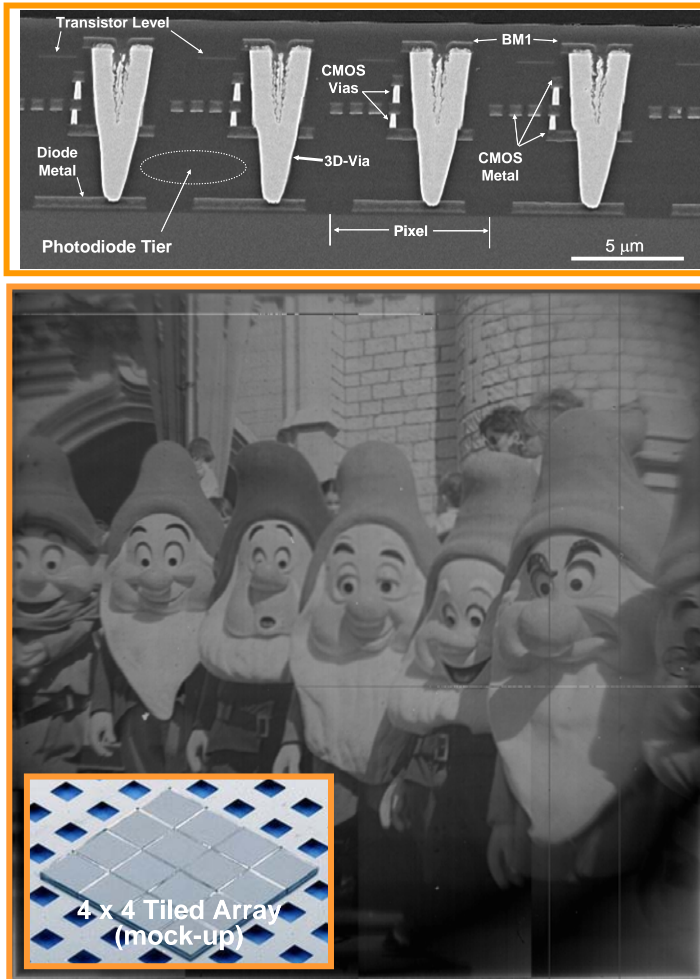
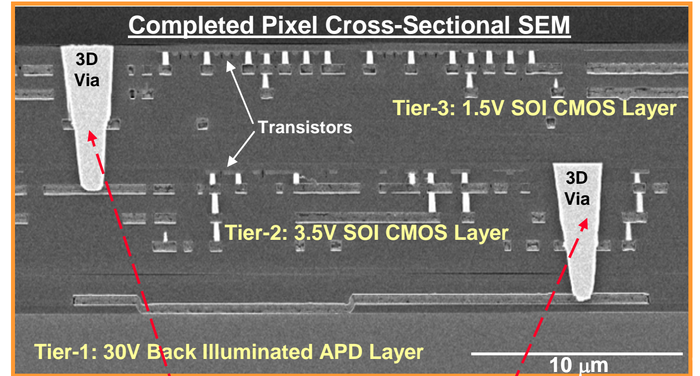


Figure 5. Top image is a cross-sectional SEM of four pixels of a two-tier, 4-side-abuttable, 1024x1024, 8µm-pixel pitch, 100% fill factor visible focal plane. Below is an actual 1024x1024 test image from the 3D integrated focal plane. Inset image is a mock-up 4x4 imager tile "mosaic" array, showing how the 4-side-abuttability enabled by the 3D integration can allow larger focal planes to be tiled together with minimal seam loss (~3 pixels).



To-Scale Pixel Layout of Completed 3-tier Laser Radar Focal Plane

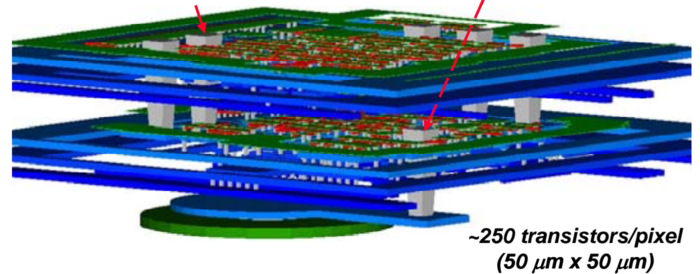


Figure 6. Cross-sectional SEM of a single pixel from a functional 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array. Tier-1 is a 30 volt APD tier which is 3D-integrated to tier-2, a 3.3 volt CMOS interface circuit tier, which is 3D-integrated to tier-3, a 1.5 volt CMOS high-speed timing circuit tier. Below the cross-sectional image is a CAD drawing of the completed pixel layout. There are ~250 transistors and six 3D-vias per pixel in this circuit.

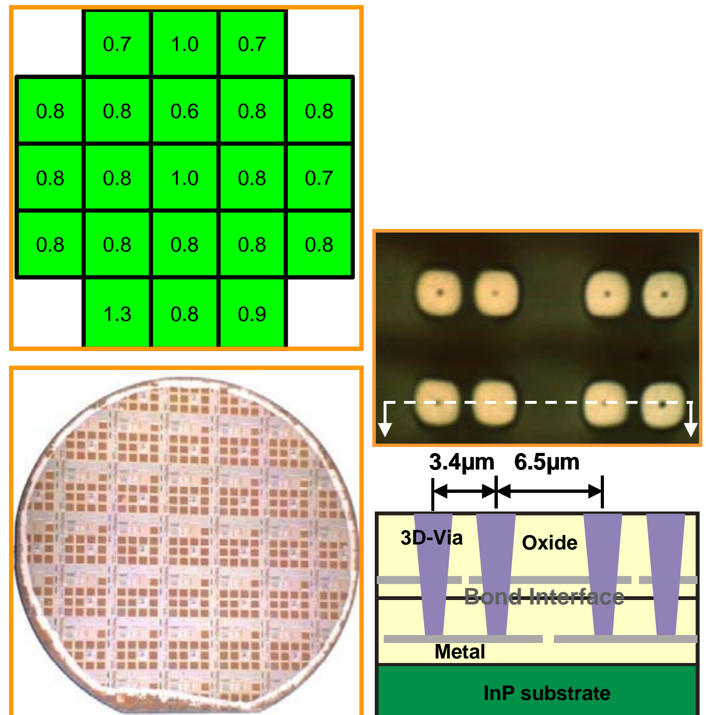


Figure 7. Bottom left is a photograph of a SOI CMOS circuit tier 3D-integrated to a pattern 150-mm-diameter InP wafer. This two-tier stack was used to evaluate the effectiveness of the 3D integration process with mixed semiconductor material systems. Top left is a die yield map showing 100% yield of 10,000-link 3D-via-chains. The number in each green box is the average resistance per 3D-via-link in the chain. Right side of figure is top-down image and cross-sectional drawing of a section of the completed 3D-via-chain.

References

[1]J.A. Burns, et. al., "A Wafer-Scale 3-D Circuit Integration Technology," *IEEE Transactions on Electron Devices,* vol. 53, no. 10, pp. 2507-2516, Oct. 2006.

[2]J.A. Burns, et. al., "Three-dimensional integrated circuits for low power, high bandwidth systems on a chip," *2001 ISSCC Int. Solid-State Circuits Proceedings, Digest of Technical Paper*s vol. 44, pp. 268-269, Feb. 2001.

[3]V. Suntharalingam, et. al., "Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology," *2005 ISSCC Int. Solid-State Circuits Proceedings, Digest of Technical Paper*s vol. 48, pp. 356-357, Feb. 2005.

[4]B. Aull, et. al., "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers", *2006 ISSCC Int. Solid-State Circuits Proceedings, Digest of Technical Paper*s vol. 49, pp. 304-305, Feb. 2006.

High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology

Chung-Wei Chang[1, 2], Shou-Gwo Wuu[1], Dun-Nian Yaung[1], Chien-Hsien Tseng[1], Han-Chi Liu[1], David Yen[1], Yi-Jiun Lin[1], Chun-Ming Su[1], Chun-Yao Ko[1], C.Y. Yu[1], C.H. Lo[1], F.J.Hsiu[1], C.S.Tsai[1], Chung S. Wang[1], Mingo Liu[1], Chrong-Jung Lin[2], Ya-Chin King[2]

[1]Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, R.O.C.

[2]Microelectronics Lab, Department of Electrical Engineering, National Tsing Hua University, Hsin-Chu,Taiwan, R.O.C.

Tel:(886)35636688 Ext.7088150, Fax:(886)35784848, E-mail: cwchang@tsmc.comT

Abstract

The optical effects of dielectric film properties and thickness are investigated for 0.18um enhanced CMOS image sensor. The spectral response degradation caused by destructive interference was observed in the photodiode under Si surface with thicker contact etch stop layer (CESL) and thicker oxide on Si surface. Investigations of optical effect on dielectric films show proper film structure and thickness that can result in higher quantum efficiency. In this paper, an low extinction coefficient (low-k) SIN for CESL combined with CESL/Oxide/Si films structure have been proposed by the experimental and simulation results of quantum efficiency. The spectral response can be improved and offer an optimized dielectric film thickness for CESL/Oxide/Si film structure. To improve photo-sensitivity, we also developed a high refraction-index (R.I.) inner microlens in CMOS image sensor, which result in increasing photo-sensitivity by 50% at least.

Introduction

There are several advantages for CMOS image sensor (CIS) compared to CCD image sensor. The CMOS image sensor (CIS) has the superior characteristics: low power consumption, selective read-out, and compatibility with CMOS logic technology and on-chip functionality [1-2]. Continuous pixel shrink has been created due to the strong demand for smaller chip size and high resolution of CIS[7-9]. As the pixel size is shrunk and CMOS technology is downscaled to deep sub-micron, the fabrication of high performance CIS will be limited by standard CMOS logic process, such as silicides and high refraction-index (R.I.) films [3-5]. An additional dielectric film as a CESL for borderless contact (BLC) has been widely used in CMOS technology to minimize the chip size by restricting the clearance of contact-to-silicon and contact-to-poly to zero [6]. The selective Co-silicide is only formed on poly-gate and Oxide is remained on S/D region and photo-diodes [7-9]. However, these additional layers will cause extra interference and reflection effect then impact the photo response of CIS. Several reports studied the optical effect on backend dielectrics structure for photosensitivity improvements [10-12]. In this paper, the actual optical response of photodiode for different film properties and thickness are proposed and lead to proper film structure, properties and thickness. In addition, the quantum efficiency (Q.E.) and reflectivity simulation show the relation between spectral response, reflectivity and dielectric films thickness to find the optimized dielectric properties for high photosensitivity. Moreover, a high R.I. inner microlens for CMOS image sensor is proposed to improve photosensitivity.

Technology

The basic technology is 0.18um enhanced CMOS image sensor technology, including shallow trench isolation (STI), retrograde channel doping, self-aligned silicide gate and S/D. Special process modifications such as non-silicide, optimized junction profile of floating node, thinner backend thickness, and shrunk contact/ well/ metal to 0.13um CIS design rule are implemented to improve pixel performance[7-9]. The advanced application software "Medici" for optical device was used to simulate the quantum efficiency of photodiodes with different dielectric films and thickness. Furthermore, in order to increase photo response when pixel size is scaled down to 2.2um, we have developed a high sensitivity of dielectric film structure, and a high refractive inner microlens for CMOS image sensor. Fig.1(a) shows the cross section of typical backend dielectric structure and photodiode under CESL/ Oxide/ Si structure for logic process. Fig.1(b) shows a cross sectional TEM picture of non-silicide S/D pixel. Co-silicide is only formed on poly-gate and oxide is remained on S/D region. Contact etch stop layer (CESL) is directly coated on Co-silicide and oxide. The n type sensor on p-sub will be dedicated for our study. The inner microlens structure was made on each pixel. The processes for inner microlens are compatible with standard CMOS logic process, just added to define inner microlens after passivation film deposition. The higher RI dielectric film for inner microlens, such SIN, enhanced the ability of inner microlens to focus the incident light.

Experimental Results

Fig.2 illustrates measured quantum efficiency with different passivation structure and thickness. Both PASS_SIN and low-k_SIN of passivation film show similar Q.E result, so we focused on CESL/ Oxide/Si dielectric structure in this paper. Fig.3 shows the measured quantum efficiency of photo diodes with different contact etch stop layer: (a) CESL_SIN (b) low-k_SIN . The low-k_SIN shows better quantum efficiency than CESL_SIN. It's attributed to low-k_SIN dielectric film with low extinction coefficient (k) as Fig.4 presented. Fig.5 illustrates the measured quantum efficiency of photo diodes with different CESL_SIN thickness at same oxide layer thickness. Increasing CESL_SIN thickness, shows the worse quantum efficiency, especially for blue light (400nm~500nm). The simulated Q.E. of Fig.6 shows the similar results. Fig.7 plots on the reflectivity, different CESL_SIN dielectric film thickness are interacted. The higher reflectivity and destructive interference is presented to degrade quantum efficiency of photo diodes by contact etch stop layer thickness increasing.

Fig.8 illustrates measured quantum efficiency of photo diodes with different oxide layer thickness at same contact etch stop layer CESL_SIN. Increasing oxide thickness, shows the worse quantum efficiency, especially for blue light (400nm~500nm). The simulated Q.E. of Fig.9 shows the similar result, increasing oxide thickness degrades Q.E., which is more serious for short wavelength region. This higher reflectivity and destructive interference is presented when oxide thickness increasing as Fig.10 presented.

For the further improvement of sensitivity by collecting more incident light, we develop an additional dielectric inner microlens for each pixel. Fig.11 is the pixel sensitivity versus the inner microlens thickness, indicating that high photo-sensitivity is obtained for adding the inner microlens. There is more than 50% sensitivity enhancement compared with standard condition (without inner microlens). The spherical shape and curvature of inner microlens were split by dielectric thickness, the best sensitivity was performed on thinner inner microlens dielectric thickness.

Conclusion

The optical effects of of dielectric films structure and thickness variation have been investigated. The spectral response of photodiode is obviously dependent on dielectric film properties and thickness, especially for CESL_SIN/ Oxide/ Si structure. By suppressing reflection and interference effects between CESL_SIN/ Oxide/ Si structure can get the best performance. In addition, the higher sensitivity CESL dielectric film (low-k_SIN), and high R.I inner microlens in CMOS image sensor has been successfully developed to increase photo-sensitivity further.

Acknowledgements

The authors would like to thank R.D. McGrath, Hung Doan, Christopher. Parks, and Gang Shi of Eastman Kodak company for their valuable discussion.

Reference

[1] R. M. Guidash, IEDM Tech. Dig., pp.927-929, 1997.
[2] Sunetra K. Mendis, IEDM Tech. Dig., pp.583-586, 1993.
[3] Hon-Sun Wong, IEDM ED, pp.2131-2142, 1996.
[4] Hi-Deok Lee, IEEE ED, pp.1848-1850, 1998.
[5] S. J. Park, ICVC on VLSI and CAD, pp.211-213, 1999.
[6] W. C. Liu, IEEE EDL, pp.344-346, 2000
[7] S. G. Wuu, IEDM Tech. Dig., pp.705-708, 2000.
[8] H. C. Chien, IEDM Tech. Dig., pp.813-816, 2002
[9] C.H.Tseng, IEDM Tech. Dig., pp.997-1000, 2004
[10] Tohru Yamada, IEEE CCD&AIS workshop, pp. 131-135, 2003
[11] T.H. Hsu, IEEE CCD&AIS workshop, pp. , 2005
[12] T.H. Hsu, IEEE EDL, pp.547-549, 2005

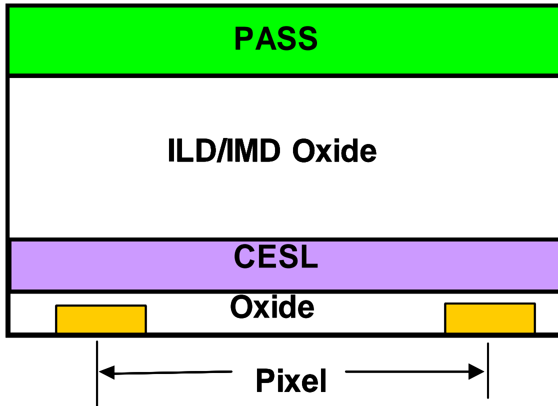


Fig.1(a) Cross section of typical backend dielectric structure of CIS

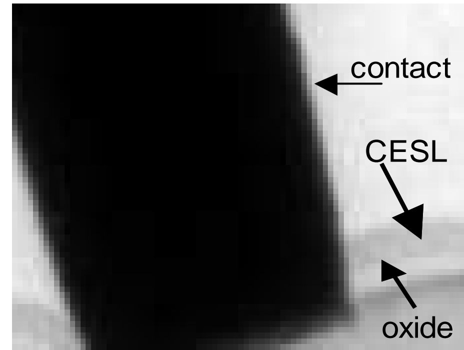


Fig.1(b) Cross sectional TEM photographs of pixel

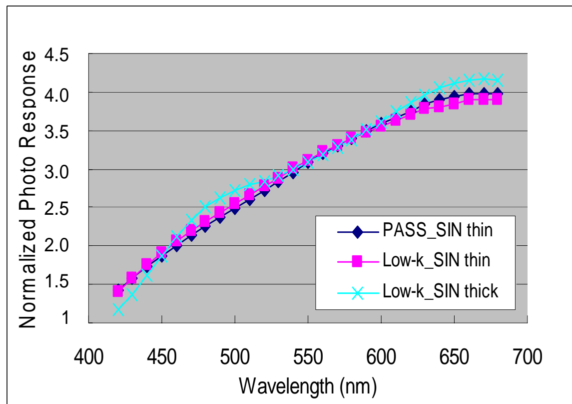


Fig.2 Photo response for different passivation dielectric film structure & thickness

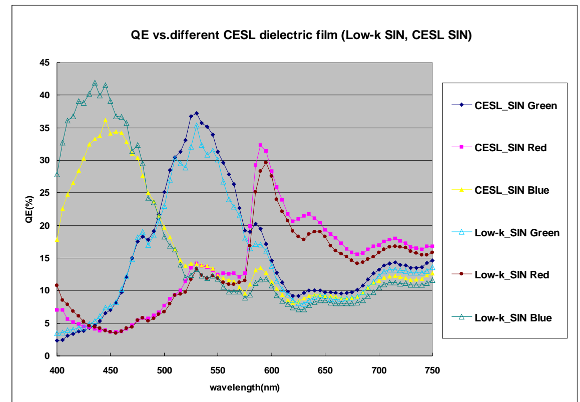


Fig.3 Real Q.E for different CESL dielectric film structure

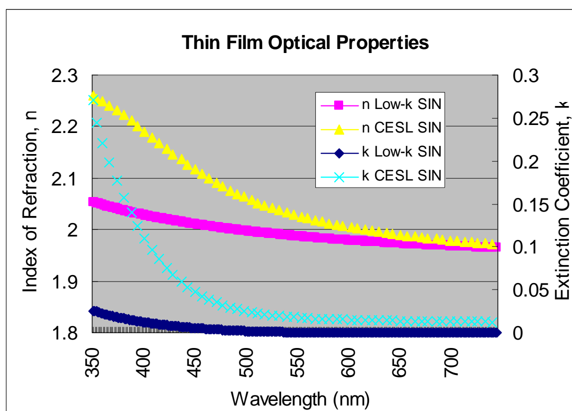


Fig.4 Dielectric film n, k properties for contact etch stop layer

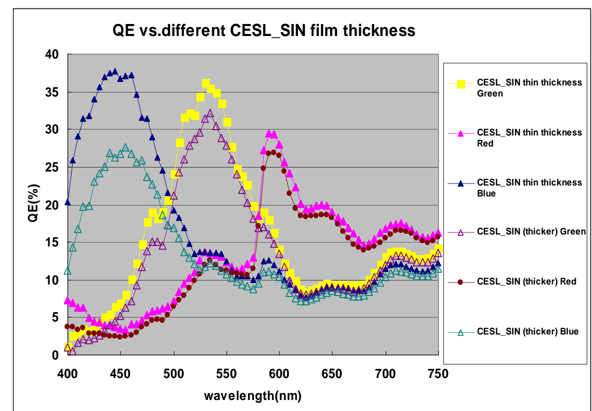


Fig.5 Real Q.E for different C.E.S.L dielectric film thickness

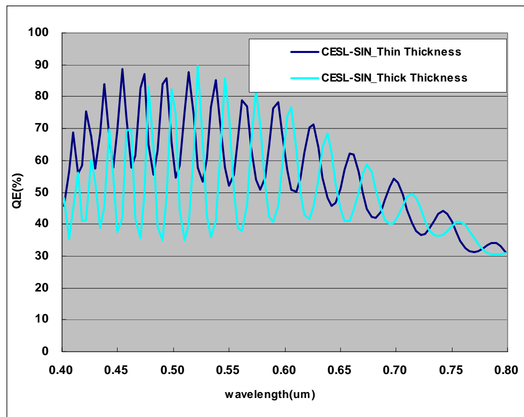


Fig.6 Simulated Q.E for different CESL_SIN dielectric thickness

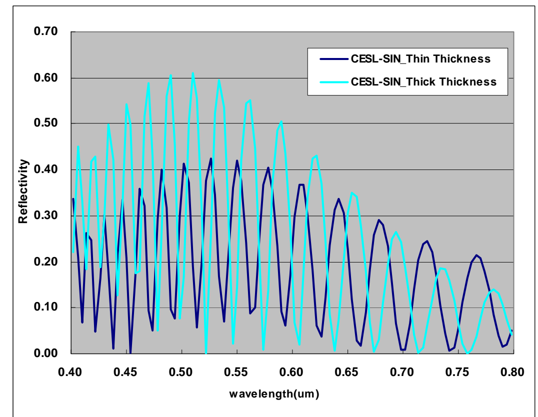


Fig.7 Simulated reflectivity rate for different CESL_SIN thickness

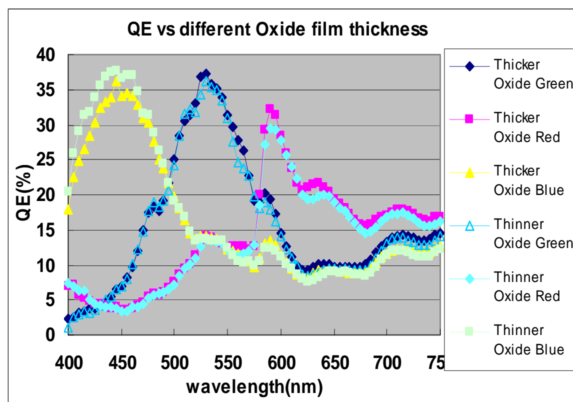


Fig.8 Real Q.E for different oxide film thickness

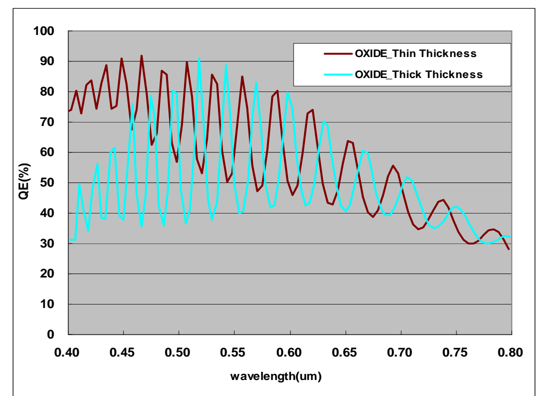


Fig.9 Simulated Q.E for different oxide thickness

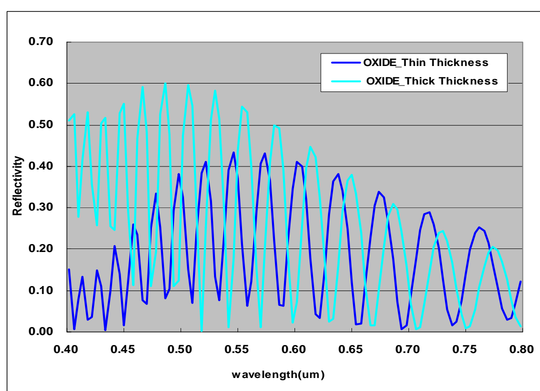


Fig.10 Simulated reflectivity for different oxide thickness

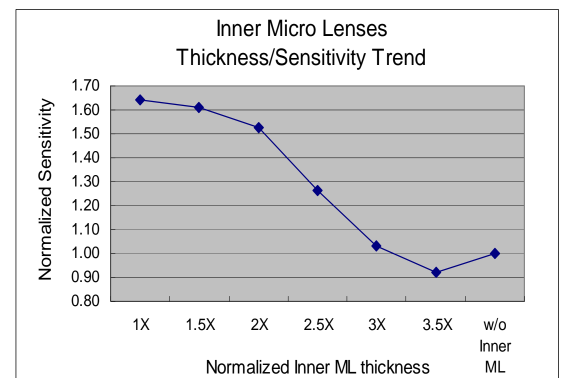


Fig.11 The inner microlens thickness and sensitivity in CMOS image sensor

Reliability of CMOS image sensor with polymer lightpipe

J. Gambino, K. Ackerson, B. Guthrie, B. Leidy, W. Abadeer, S. Mongeon,
D. Meatyard, J. Adkisson, R. J. Rassel, J. Ellis-Monaghan, M. Jaffe

IBM Microelectronics, 1000 River Street, Essex Junction, VT, 05452
phone: 802-769-0433 fax: 802-769-9452 email: gambinoj@us.ibm.com

Abstract

The reliability is assessed for a CMOS imager technology using Cu wiring and a polymer light-pipe. The reliability of both the Cu interconnects and the pixel devices are characterized. No reliability problems are observed with the Cu wires, due to an SiN barrier that lines the lightpipe. However, with a non-optimized process, an increase in dark current is observed on some modules after a stress at 130°C in 85% humidity. It is proposed that the increase in dark current is due to diffusion of mobile ions into the transfer gate through openings in the SiN barrier.

Introduction

Copper interconnect technology offers advantages for CMOS imagers, allowing thinning of the optical path, resulting in improved angular response [1]. However, the SiN capping layers used to passivate the surface of the Cu introduce discontinuities in the refractive index, that can reflect light and reduce the sensitivity of imager [1]. Hence, the SiN must be removed from the optical path [1-3].

Another problem common to all image sensors is the decreasing photodiode size as the pixel size decreases. Because of the small photodiode size, pixel sensitivity is reduced and crosstalk increases. In a previous report [4], a lightpipe process was described that provides high quantum efficiency and high angular response. In this report, the reliability of affect of the light-pipe process on device reliability is described.

Experiment

CMOS imagers were fabricated using a 4T-shared pixel architecture, with 0.18 μm foundry process for the devices [5] and a 0.13 μm foundry process for the Cu wires [6]. The imagers have four levels of metal; M1 through M3 are Cu, with an undoped SiO_2 dielectric, and the last metal level is Al. The minimum M1 and M2 pitches are 0.32 and 0.40 μm, respectively, while the minimum via diameter is 0.23 μm. After etching the final Al metal layer, the lightpipe is formed by etching through the entire dielectric stack above the photodiode, then coating the surface with an SiN layer. The lightpipe is filled with an organic planarizing layer, and then color filters and microlenses are formed using conventional processing (Fig. 1 and 2).

To test the reliability of the lightpipe process, CMOS imager chips were fabricated with or without the lightpipe. The test chips consisted of 512x512 imager arrays with 2.2 μm pixels, and were built into modules in a ceramic, wirebond package with glass lids. The modules were pre-stressed to remove early fails, and then were subjected to the reliability stresses. Six different stress conditions were examined (Fig. 3), including high temperature storage (HTS), temperature-humidity-bias (THB) at 40°C or 85°C, high temperature operating life (HTOL), and thermal cycle T/C), and unbiased highly accelerated stress test (uHAST).

The performance of the modules was characterized before and after stress using tests measuring pixel response to saturation light levels, 75% of saturation for blue, green and red light, and dark conditions at varying integration times. The saturation field was done with the blue, green and red light emitting diodes turned on to 1.5X their 75% level voltage. Pixel by pixel data from each of the light conditions was used to obtain mean saturation, color response by pixel color, read noise, defect levels and dark current. The mean dark current for each module was calculated from pixel response (leakage) at two different integration times. The delta of the two integration times (864mS and 54mS in this instance) was used to obtain dark current in the units of electrons per second. After stress, samples were characterized by transmission electron microscopy (TEM) to determine the failure mode.

Some wafer level tests were also conducted to test the integrity of Cu wiring adjacent to the lightpipe. Stacked via structures were formed and were exposed to an accelerated humidity test (130°C, 85% relative humidity), while monitoring the change in via resistance.

Results and Discussion

The spacing between the lightpipe opening and the Cu wiring must be carefully controlled. If the Cu is exposed to the resist strip process, severe oxidation of the Cu will occur which can degrade yield and affect reliability. With

proper control of the lightpipe spacing to adjacent Cu wires, high Cu reliability can be achieved. There is no increase in via resistance, even after a 96 h accelerated humidity stress (Fig. 4), implying that the SiN and Ta-based barriers form a good hermetic seal, even in the presence of the lightpipe.

The mean saturation is the same before and after each stress, for modules with or without a lightpipe, indicating that there is no degradation in the optical performance of the imager. An example is shown in Fig. 5, for a THB stress at 40°C. This suggests that there is no degradation of the polymer fill material as a result of temperature or humidity.

Histograms of dark current are shown in Fig. 6, for modules tested before and after a THB stress at 40°C. The dark current is similar for samples with or without a lightpipe, indicating that the lightpipe process has not degraded dark current. In addition, exposure to humidity at 40°C or 85°C does not degrade the dark current.

The situation is different after a uHAST stress at 130°C in 85% humidity. In this case, some modules (with a non-optimized lightpipe process) show an increase in the mean dark current , after stressing for 100 h (Fig. 7). The degradation is also evident in dark field images from these modules, especially after 125 h (Fig. 8).

TEM analysis from failing modules reveals a number of problems with the non-optimized lightpipe process (Fig. 9-11). The lightpipe etch has removed some of the polysilicon for the transfer gate (Fig. 9). There is also an etch residue from the lightpipe etch over the SiN etch stop layer and the final SiN passivation on the sidewalls of the lightpipe is thin (Fig. 10). Note that despite the thin SiN passivation, there are no problems with the Cu wires (Fig. 11).

Based on the TEM analysis, it is proposed that the degradation in dark current during the uHAST stress is due to diffusion of mobile ions (such as sodium) into the transfer gate through openings in the SiN barriers. The mobile ions can change the surface potential under the gate, resulting in high generation currents. To improve the reliability of parts fabricated with the lightpipe, the process has been optimized to minimize erosion of the SiN etch stop, remove the etch residues, and increase the sidewall coverage of the final SiN passivation (Fig. 13.) With the optimized process, the dark field pixel response remains low, even after a 192 hr uHAST stress (Fig. 14).

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Conclusion

The reliability is assessed for a CMOS imager technology using Cu wiring and a polymer light-pipe. The reliability of both the Cu interconnects and the pixel devices are characterized. No reliability problems are observed with the Cu wires, due to an SiN barrier that lines the lightpipe. However, with a non-optimized process, an increase in dark current is observed on some modules after a stress at 130°C in 85% humidity. It is proposed that the increase in dark current is due to diffusion on mobile ions into the transfer gate through openings in the SiN barrier.

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Acknowledgement

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References

1. J. Adkisson, J. Gambino, T. Hoague, M. Jaffe, R. Leidy, R.J. Rassel, J. Kyan, D. McGrath, D. Sackett, C. Stancampiano, Proc. IEEE Workshop Charge Coupled Devices Adv. Image Sensors, 2005, p. 1.
2. Y.C. Kim, Y.T. Kim, S.H. Choi, H.K. Kong, S.I. Hwang, J.H. Ko, B.S. Kim, T. Asaba, S.H. Lim, J.S. Hahn, J.H. Im, T.S. Oh, D.M. Yi, J.M. Lee, W.P. Wong, J.C. Ahn, E.S. Jung, Y.H. Lee, IEEE Sol. St. Circuits Conf., 2006, p. 494.
3. J. Gambino, J. Adkisson, T. Hoague, M. Jaffe, R. Leidy, R.J. Rassel, J. Kyan, D. McGrath, D. Sackett, C. Stancampiano, AMC 2005 Proc., MRS, 2006, p. 153.
4. J. Gambino, B. Leidy, J. Adkisson, M. Jaffe, R.J. Rassel, J. Wynne, J. Ellis-Monaghan, T. Hoague, D. Meatyard, S. Mongeon, T. Kryzak, IEDM Proc., 2007, p. 131.
5. B. Agarwala, M. Armacost, S. Biesemans, L. Burrell, B. Chen, K. Han, D. Harmon, J. Heidenreich, K. Holloway, N. Rovedo, S. Kapur, T. Kebede, D. Kiesling, P. Kim, G. Matusiewicz, J. Lukaitis, P. Nguyen, N. Prabhakara, S. Rauch, G. Friese, F. Grellner, E. Kaltalioglu, M. Hoinkis, C. Lin, R. Mahnkopf, O. Prigge, T. Schafbauer, T. Schiml, K. Schruefer, S. Srinivasan, M. Stetter, M. Unger, R. Zoeller, ESSDERC'99, 1999, p. 632.
6. A. Stamper, C. Adams, X. Chen, C. Christiansen, E. Cooney, W. Cote, J. Gambino, J. Gill, S. Luce, T. McDevitt, B. Porth, T. Spooner, A. Winslow, R. Wistrom, Proc. AMC 2002, MRS, 2003, p. 485.

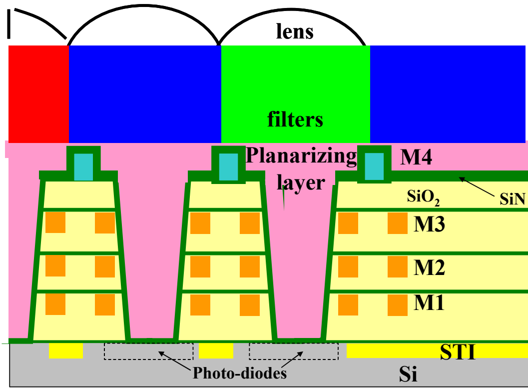

Fig. 1. Schematic of lightpipe.

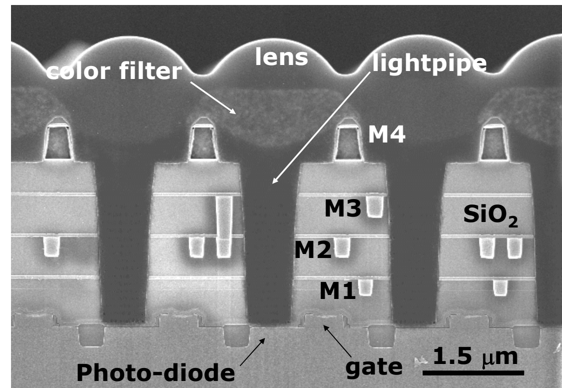

Fig. 2. SEM cross-section of 2.2 µm pixel with lightpipe and Cu wiring.

Pre-Stress:
125°C, 24h bake + 10 T/C (-40 to +60°C) + 125°C, 24h bake

Stress:
* HTS: 125°C, no bias, 1000 h
* THB_40: 40°C, 85% RH, 4.3V, 1000 h
* THB_85: 85°C, 85% RH, 4.3V, 1000 h
* HTOL: 125°C, 4.3V, 1000 h
* T/C: -55 to +125°C, 1000 cycles
* uHAST: 130°C, 85% RH, 125 h

Fig. 3. Summary of stress conditions.

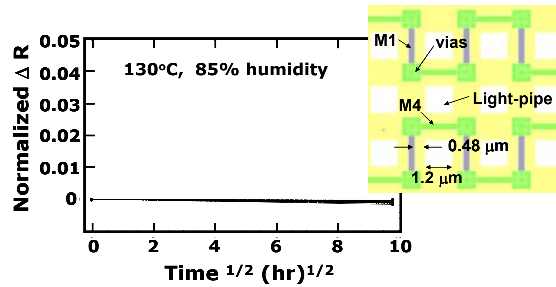

Fig. 4. Variation of via resistance with stress time for stacked via chains next to lightpipe during high temperature humidity test.

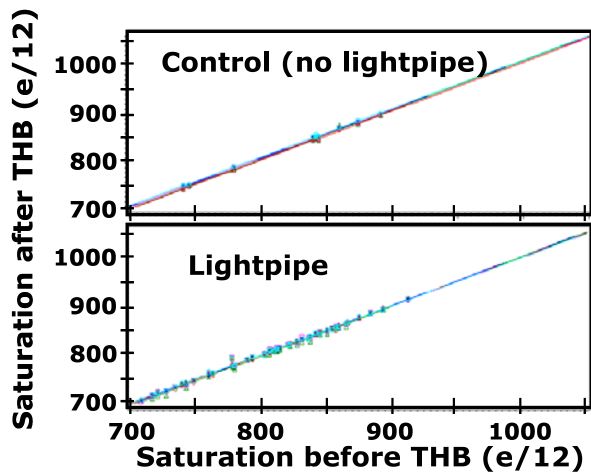

Fig. 5. Mean saturation for each module before and after THB stress at 40°C for 1000 h.

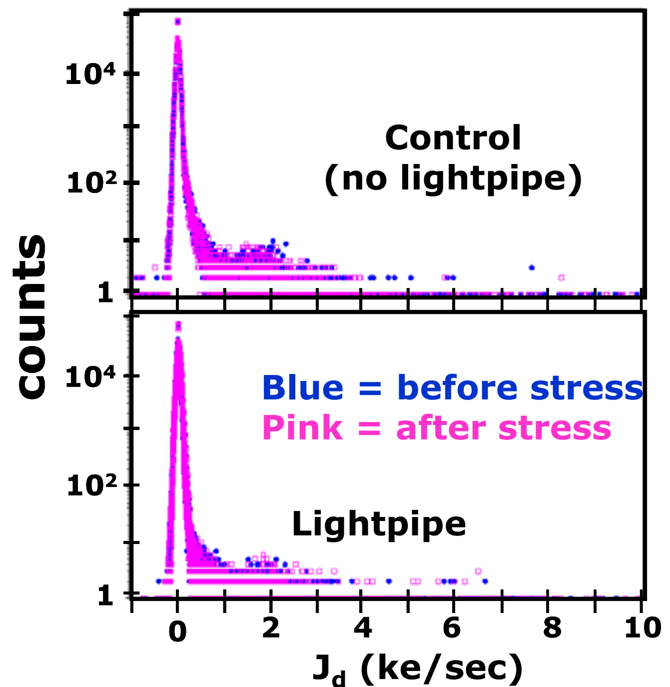

Fig. 6. Dark current histograms by pixel before and after THB stress at 40°C for 1000 h.

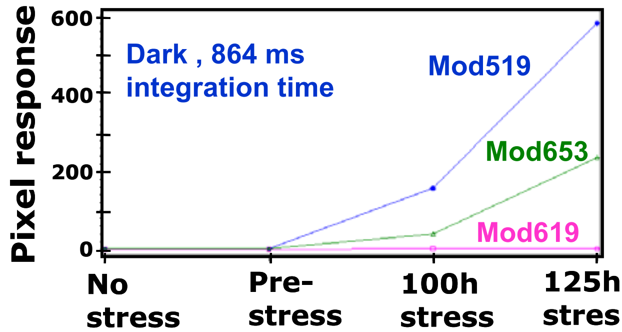

Fig. 7. Mean pixel response in a dark field for different modules with non-optimized lightpipe after uHAST stress.

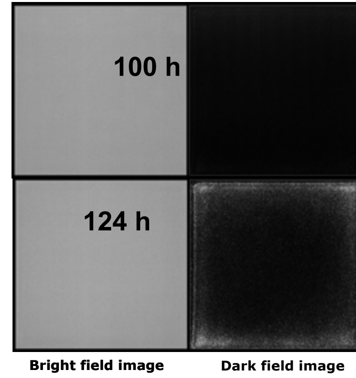

Fig. 8. Images taken from modules after uHAST stress.

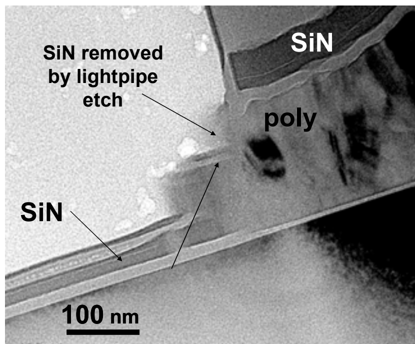

Fig. 9. TEM of sample with non-optimized lightpipe after uHAST stress.

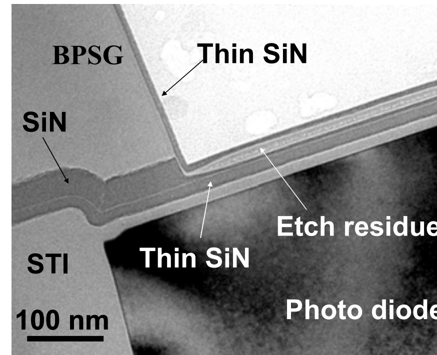

Fig. 10. TEM of sample with non-optimized lightpipe after uHAST stress.

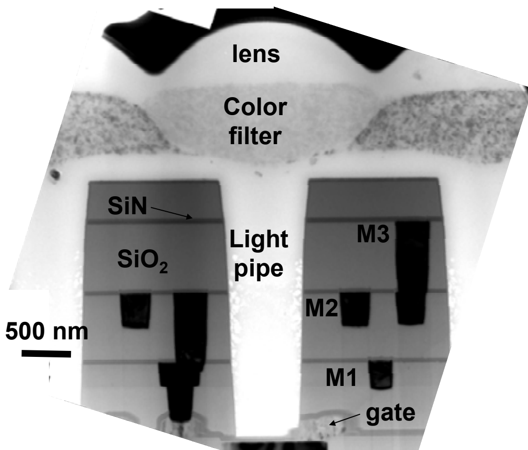

Fig. 11. TEM of sample with non-optimized lightpipe after uHAST

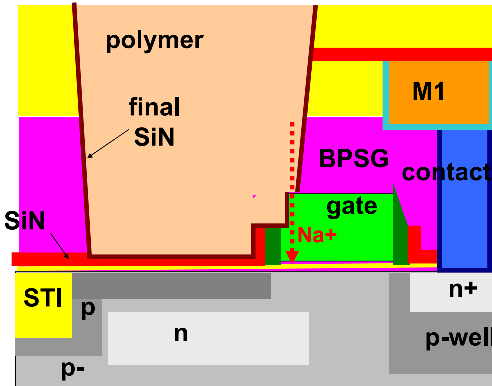

Fig. 12. Schematic of failure mechanism during uHAST stress.

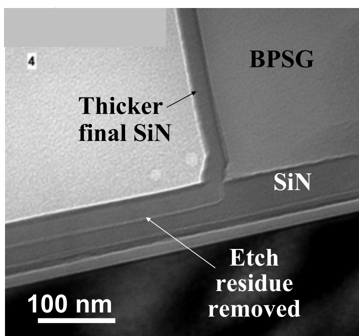

Fig. 13. TEM of optimized lightpipe process.

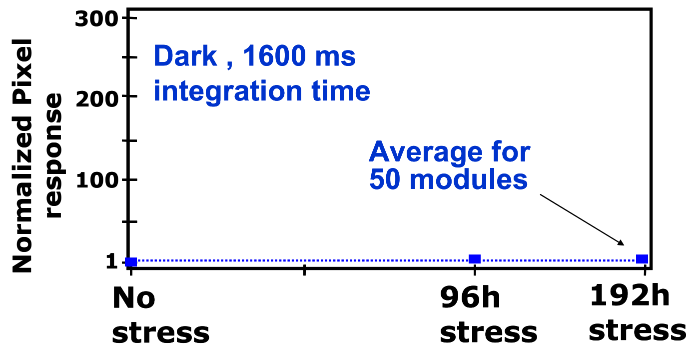

Fig. 14. Mean pixel response in a dark field for parts with optimized lightpipe before and after uHAST stress.

Integrated Processes for Detector Back Illumination*

Richard C. Westhoff†, Robert K. Reich, Andrew H. Loomis, James A. Gregory
MIT Lincoln Laboratory, 244 Wood Street, Lexington, MA USA 02420

Back-illuminated imagers can have high quantum efficiency at ultraviolet and x-ray wavelengths. Most back-illumination (BI) processes have limitations (e.g. fragility of thinned substrates[1], or the presence of epoxy[2], gold[3] or other bonding agents) that limit their applicability and process latitude. For example, these bonding agents limit BI processing at elevated temperature (i.e. ~400°C, hydrogen sintering), resulting in relatively high dark currents. More recently, 3D integration processes based on oxide bonding have addressed some of these issues for thin detector structures[4]. We describe BI processes, based on low-temperature oxide bonding, which can be integrated into the process flow of microelectronics fabs. The BI process faces two main challenges:

1. The need to produce thick (10-75 µm) active layers.
2. The need for high bond yield (~100%), due to the large detector area.

The first requirement makes it difficult for the gases that evolve at the bonded oxide-oxide interface to diffuse out of the structure without causing voids at the interface. This out-gassing occurs in low-temperature oxides (deposited thermally or plasma enhanced) at temperatures between ~275-400°C, and forms large voids at the bonded interface, as shown in Figure 1, which compares an image from a scanning acoustic microscope (SAM from Sonoscan™) to a thru-wafer IR image. The inspections are seen to be equivalent, but the SAM images provide more contrast and better sensitivity, particularly for small voids. The bonded region at the edge of the wafer (~40 mm), suggests that the interface gases could be "vented" by etching trenches in the oxide before bonding. Additionally, annealing the deposited oxide at a temperature above the final sintering temperature should reduce the out-gassing at the interface. The effect of a chemical mechanical planarization (CMP) step after the trench etching process was also investigated.

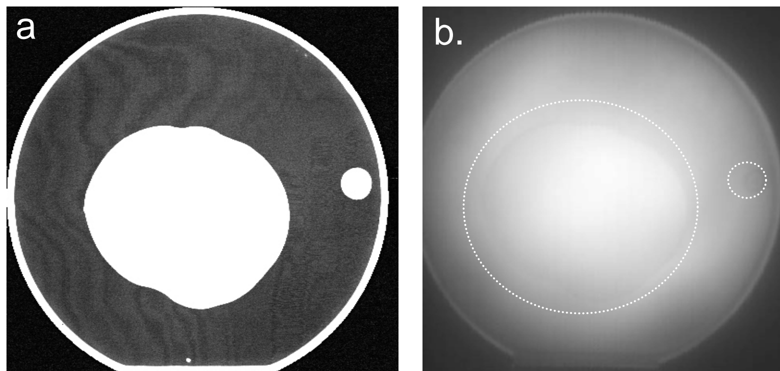

Figure 1. Scanning acoustic microscope (SAM) image (a) and IR transmission image (b) of plasma oxide-thermal oxide bonded wafer pair number 2/16 sintered at 400°C. Large void (white region) forms due to gas evolution at the bond interface during the sinter step.

The initial parameters and results of this experimental approach are summarized in Table I. Wafer pairs included a thermal oxide handle wafer and a device wafer with plasma enhanced chemical vapor deposition (CVD) oxide deposited from silane and oxygen. Since the plasma oxide as deposited is too rough (~6 nm RMS) for bonding purposes, the roughness is reduced to the 0.3-0.4 nm RMS level using CMP of the oxide, smooth enough to enable oxide-oxide bonding. Following CMP, the plasma oxide was annealed at 450°C in nitrogen for 30 minutes. The wafers were then patterned using photoresist and trenches 200 µm wide and 0.5µm deep were etched in the plasma oxide on the device wafers. In some cases a short follow-up, "kiss" CMP was done to remove possible defects caused by the patterning and trench etching.

The experimental results indicate that the absence of the trenches leads to large voids in the wafer center after post-bond sintering (Figure 2), even when the wafers are essentially void free just after bonding. Pre-bond annealing (Figure 3) also appeared to reduce the size of the voids. The effect of the clean and of the kiss CMP after trenching was less significant. On the initial three wafers the combination of trenches and nitrogen annealing before bonding

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† westhoff@ll.mit.edu, 781-981-3282 (voice), 781-981-3433 (fax)

produced bonds that survived sintering without forming large area voids. These bonded wafers also proved capable of withstanding the backgrinding and CMP process to ~60μm thickness without loss of the active layer.

Waf. No.	Device wafer	CMP	Pre-bond N2 Anneal	Trench	Kiss CMP	Clean	H2 Sinter	IR inspection results
2/16	No-pattern	Yes	450°C, 30 min	No	No	RCA-1, No megasonic	400°C, 60 min	5 cm dia. void ctr.
3/17	No-pattern	Yes	450°C, 30 min	No	No	H_2O_2, No megasonic	400°C, 60 min	2 cm dia. void ctr. & edge
5/18	Pattern	Yes	450°C, 30 min	Yes	Yes	RCA-1, No megasonic	400°C, 60 min	1 mm-size void
6/19	Pattern	Yes	450°C, 30 min	Yes	Yes	H_2O_2, No megasonic	400°C, 60 min	2 mm-size voids
10/20	Pattern	Yes	No anneal	Yes	Yes	H_2O_2, No megasonic	400°C, 60 min	5 cm dia. void ctr.
11/21	Pattern	Yes	450°C, 30 min	Yes	No	H_2O_2, No megasonic	400°C, 60 min	2 mm-size voids
12/22	Pattern	Yes	450°C, 30 min	No	Yes	H_2O_2, No megasonic	400°C, 60 min	5 cm dia. void ctr. & edge

Table I. Results of plasma oxide-thermal oxide bonding: effect of pre-bond anneal, trench, kiss-CMP and clean.

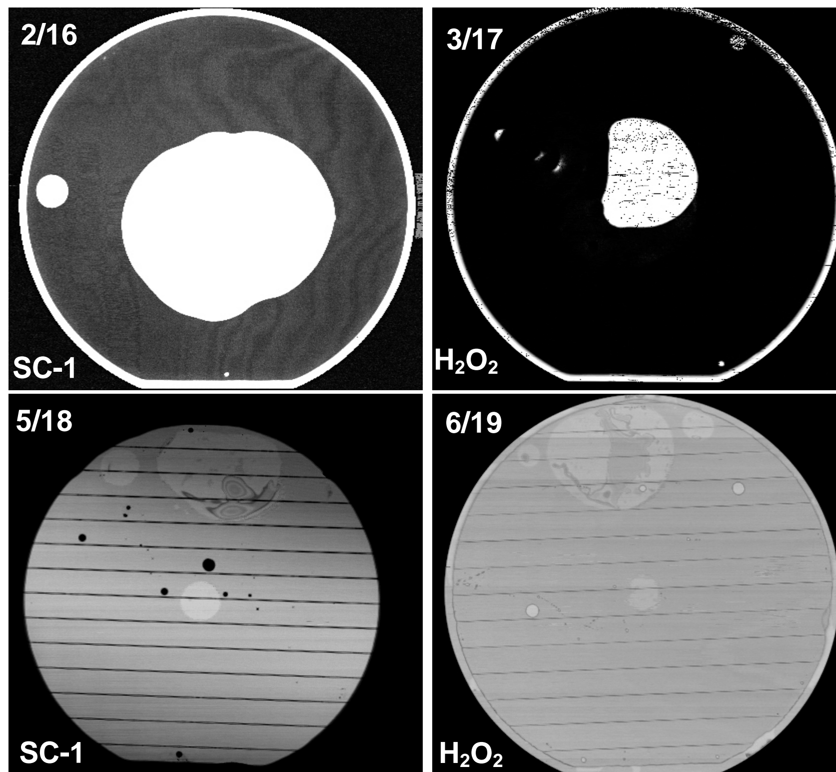


Figure 2. Comparison of SAM images of bonded wafer pairs 2/16 and 3/17 (non-trenched) versus wafer pairs 5/18 and 6/19 (trenched) with different pre-bond cleans. The device wafer from wafer pairs 2/16 and 3/16 have not been thinned while that of wafer pairs 5/18 and 6/19 have been thinned, causing the lighter wafer grey scale in the images. Lines in the image are the buried trenches that be confined in the streets between devices.

The smaller voids were determined (by microscope inspection using an infrared camera) to be caused by particles trapped at the interface. This is illustrated in Figure 4, which shows a void on a wafer, which is traced to a defect at the bond interface at the center of the void. Nearly all the small voids observed in the IR camera inspection were observed to have particles/defects at the center of the voids.

Because of the need to back-illuminate large imager devices, bonding yield is very important. For this reason, the pre-bond cleaning of the wafers was further studied to determine how to reduced particle-caused voids. This study compared RCA-1, RCA-1 & 2 cleans with megasonic energy, to RCA-1 and hydrogen-peroxide cleans without megasonic energy. The results indicated the use of RCA-1 clean followed by the use of megasonic energy were the

largest factors for reducing particulate-voids. RCA-1 only with megasonic energy produced the best results, and produced wafers that were free of small, particle related voids after sintering, as seen in Figure 5.

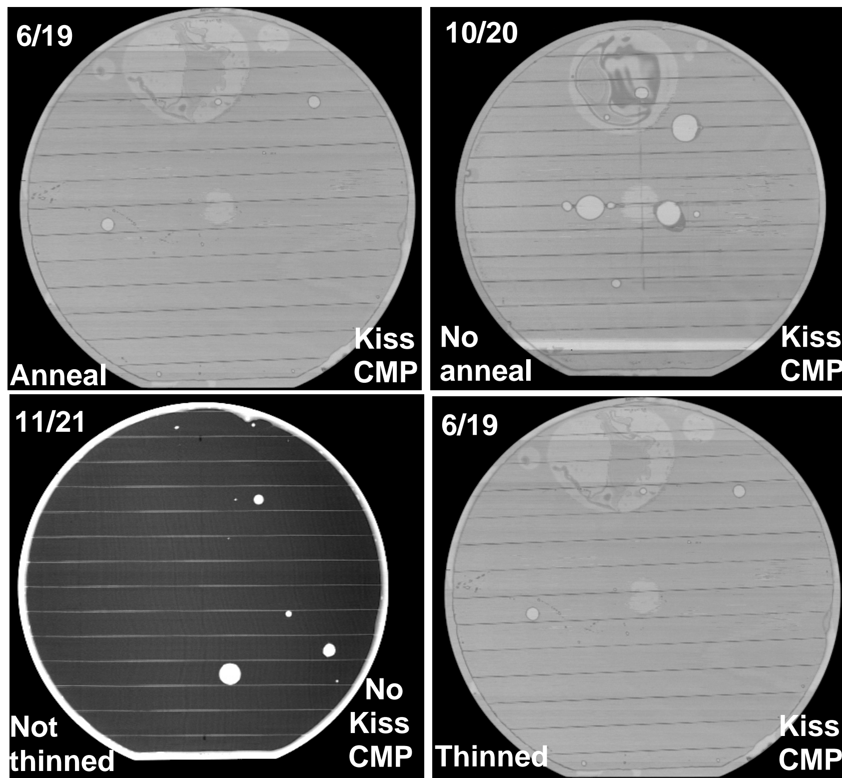


Figure 3: Comparison of SAM images of bonded wafer pairs that received a pre-bond anneal versus non-annealed wafer pairs and wafer pairs with and without a "kiss-CMP" after trenching. The device wafer of wafer pairs 6/19, 10/20 have been back thinned, while that of wafer pair 11/21 has not. Wafer pair 6/19 is shown twice for comparison of bonding with and without "kiss CMP" and with pre-bond anneal.

We have begun this BI process on device wafers with photodiode arrays. The dark current of the photodiodes was first measured in the front-illuminated condition. These device wafers have been oxide-oxide bonded (Figure 6), and back-side thinned to ~50 μm. They received back-side passivation (ion implant/t laser anneal process) followed by back-side bonding to a quartz wafer. The front-side handle wafer will next be removed, and contacts opened for testing. Following BI processing they will be used to test the effectiveness of sintering in reducing dark current in the devices.

We expect to demonstrate a BI process on photodiodes using oxide-oxide bonding shortly. It will first be used for back-illuminating avalanche photodiodes and later for CCD devices.

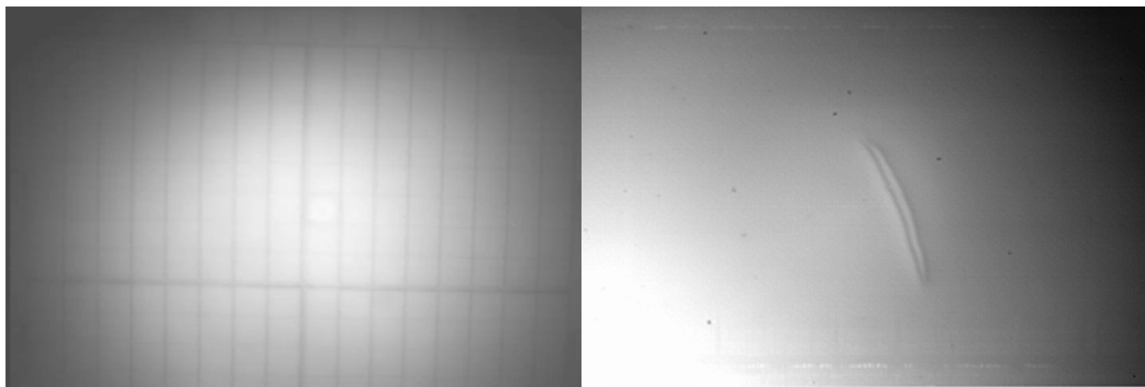


Figure 4. Result of through-wafer microscope inspection using an IR camera of voids to determine their cause. Left image is macroscopic IR image, while right is an IR micrograph of the void area.

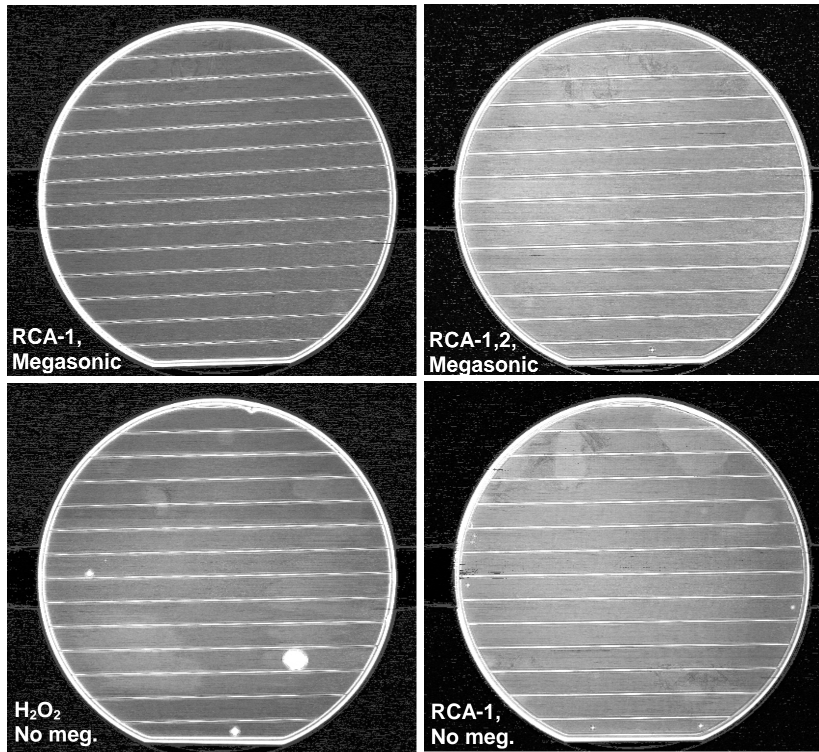
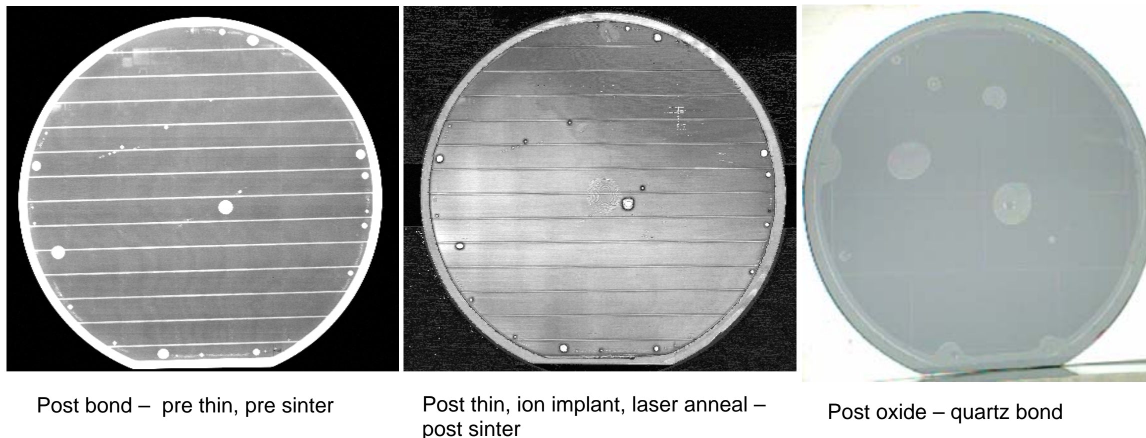


Figure 5. Sample of SAM images comparing various pre-bond cleans of plasma oxide bonded wafers after hydrogen sinter at 400°C. Wafer pairs with RCA-1 clean using megasonic energy are void free, while those using RCA-1 &2, hydrogen-peroxide or RCA-1 without megasonic energy have more voids. For the RCA-1 with megasonic energy, the edges are debonded, and the trenches are visible, but no other voids are observed.



Post bond – pre thin, pre sinter

Post thin, ion implant, laser anneal – post sinter

Post oxide – quartz bond

Figure 6. Scanning acoustic microscope images of a wafer with photodiode array devices bonded to a plasma oxide wafer. Voids are present due to the use of a non-optimized cleaning process, but no large voids are visible. Far right is an optical image of the photodiode wafer back-side after it was bonded to a quartz wafer.

References:

1. S.D. Calawa, B.E. Burke, P.M. Nitishin, A.H. Loomis, J.A. Gregory, and T.A. Lind, J. Vac. Sci. and Tech. B, **20**(3), pp. 1170-73, 2002.
2. Huang, C.M., Burke, B.E., Kosicki, B.B., Mountain, R.W., Daniels, P.J., Harrison, D.C., Lincoln, G.A., Usiak, N., Kaplan, M.A., Forte, A.R., 1989 International Symposium on VLSI Technology System and Applications, pp. 98-10, 1989.
3. Paula Grunthaner, Stythe Elliott, Todd Jones, and Shouleh Nikzad , Nasa Tech Briefs, Apr. 2004
4. V. Suntharalingam et al, "Megapixel CMOS Image Sensor Fabricated in Three- Dimensional Integrated Circuit Technology," IEEE International Solid-State Circuits Conference, p. 356, 2005.

Modeling of the Temporal Pixel to Pixel Noise of CMOS Image Sensors

Cédric Leyris, François Roy, Mathieu Marin

STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex
Phone : +33 (0)4 76 92 61 29 ; Fax : +33 (0)4 76 92 57 32
Email : cedric.leyris@st.com

Abstract— **In small area MOSFET devices widely used in the active part of CMOS image sensors, low frequency noise behavior is increasingly dominated by Random Telegraph Signal noise. For circuit designers, awareness of these single electron noise phenomena is crucial. To design optimal circuits these effects had to be taken into account. This paper presents the investigation of the modeling of the temporal pixel to pixel noise of CMOS image sensors. A model based on Shockley-Read-Hall statistics to explain the distribution of the temporal noise value in a pixel array is presented. This work takes into account RTS noise dispersion through the CDS operation. The distinctiveness of the noise variations is discussed in detail and the proposed mechanisms behind the phenomena are viewed in light of the collected data. Results are compared with experimental data.**

I. Introduction

CMOS imagers are becoming widely used in commercial applications. One subject of interest and of practical consideration is the noise which limits the low light level sensitivity. It is clear that moving towards a more aggressive technology, with smaller feature sizes, will allow the design of smaller pixels. Nevertheless, in order to improve quantum efficiency, the area of the photodiode is kept as larger as possible while using deep submicron transistors. As a result, low frequency noise in MOS transistors is becoming a significant issue for submicron CMOS image sensors. The present trend shows that thermal and 1/f noise are no longer the main contributing noise components in pixel structure transistors. Recent research proved that the Random Telegraph Signal (RTS) induced by the source follower (SF) transistor becomes dominant on the pixel read noise floor [1] [2]. Therefore, the detailed characterization of low frequency noise in advanced CMOS image sensor technologies is of prime importance prior to sensor level sensitivity improvement. RTS noise leads to flickering pixels. These pixels are impacted through different noise levels; the output noise value is distributed in a large noise range. Until now, this noise level distribution in a pixel array has not been clearly taken into account. There has not been a good understanding of this noise distribution in these circuits nor have there been convenient techniques available to simulate and analyze the output noise value distribution. In this work, for the first time, the output noise distribution in pinned 4T CMOS imager sensors is clearly characterized and modeled. We present a model that uses the RTS noise parameters extracted from a single device. A detailed investigation of the model implementation that takes into account RTS noise contribution is carried out in this work. We demonstrate based on a single transistor characterization that our model can lead to the noise distribution behavior of a full pixel array. Simulations are compared with experimental data.

II. Overview of Low Frequency Noise Models

A. Experimental noise characterization

The circuit and the readout-timing diagram of the studied 4T CMOS pixel are presented in the Figure 1. For the experimental noise characterization, the transfer gate is set to low level between the two CDS pulses in order to cancel the dark current noise coming from the photosite.

In the Figure 2 is presented the zoom of a pixel array in low-light level condition showing flickering pixel response due to noise level distribution, these variations are mainly due to RTS noise.

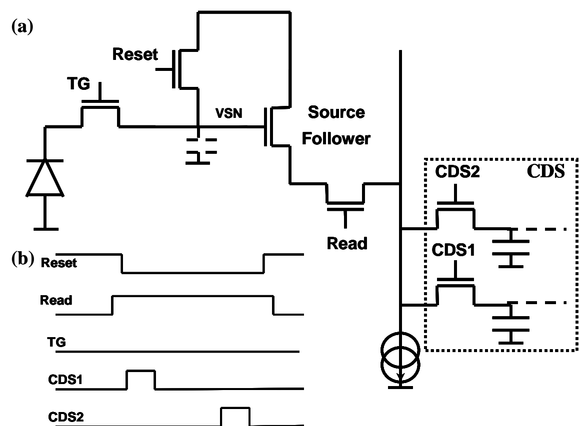


Figure 1: Circuit and readout timing diagram of 4T CMOS Image Sensor pixel. TG is the transfer gate transistor; CDS1 and CDS2 are the hold/sample of the Correlated Double Sampling (CDS).

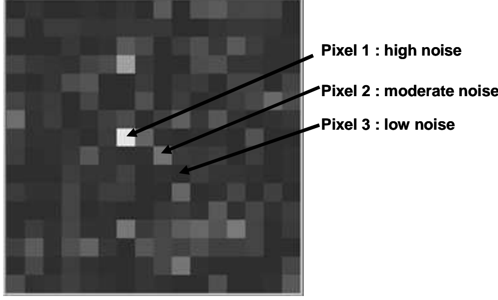


Figure 2: Zoom of a pixel array in low-light level condition showing flickering pixels response due to noise level distribution.

B. Random Telegraph Signal Noise in MOSFET

A current flowing through a solid-state device at fixed biases can be characterized by the occurrence of random fluctuations. The usual associated low frequency noise power spectral density (PSD) often shows a 1/f shape, where f is the frequency. The scaling down of device dimensions can drastically change the shape of the fluctuations in the time domain as well as the corresponding noise PSD and is the result of RTS noise contributions [3]. The classical noise models work well for large-area devices [4], [5], [6]. For small devices, they break down because the number of mobile charge carriers is no longer large and behavior of individual charge carriers becomes visible and significant. Theory predicts that as soon as the number of free carriers in the device decrease far enough, it will be possible to observe behavior of individual carriers. This is in line with experimental data. Nowadays, RTS noise is the dominant noise mechanism in small-area devices, typically with active areas of less than 1 µm². Discrete drain current switching (RTS noise) is generally observed at fixed bias values. RTS is caused by trapping of an individual carrier, due to a single active trap in the oxide, or by a scattering centre in the vicinity of the inversion layer of the device [7]. The associated RTS current noise PSD, $S_{Id}(f)$, or so-called Lorentzian spectra, is characterized by a constant plateau (P) at low frequencies and a $1/f^2$ roll-off at higher frequencies (Figure.3a). Its typical expression is:

$$S_{I_D}(f) = \frac{P}{1+\left(\frac{f}{f_c}\right)^2} = \frac{4A\tau\Delta I_d^2}{1+(2\pi f)^2\tau^2} \qquad (1)$$

Where f is the frequency, f_c the corner frequency ($f_c=1/2\pi\tau$), τ the characteristic time constant of the trap ($1/\tau=1/\tau_e+1/\tau_c$) and A the loading factor related to the trap occupation probability.

The coefficient A can be written as [8]:

$$A = f_t(1-f_t) = kT\left(-\frac{\delta f_t}{\delta E}\right)_{E=E_F} = \frac{\tau_e\tau_c}{(\tau_e+\tau_c)^2} \qquad (2)$$

Where f_t is the trap occupancy probability function, T is the absolute temperature, k is the Boltzmann constant, and τ_e, τ_c the emission and capture times, respectively.

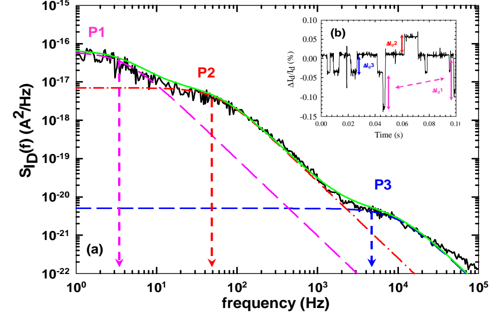


Figure 3: Typical RTS power spectral density (Lorentzian shape) (a) and corresponding relative drain current fluctuations in time domain (b) observed on the source follower transistor before CDS operation. Three traps are active at the same time.

In the time domain, various current levels are present (Figure 3b) [9]. RTS is defined by three parameters: The time spent in the up or high current state (t_1), the time spent in the down or low current state (t_0) and the amplitude ΔI_d. The mean values of t_0 and t_1 are τ_0 and τ_1 and they are defined as the up and down time constants. They usually correspond to an empty or occupied trap site, in other words, the average carrier capture or emission times. It has been demonstrated that the up and down times follow an exponential distribution [10].

RTS parameters show a strong dependency on the operating conditions, i.e. the drain (V_{DS}), gate (V_{GS}) and substrate (V_{BS}) biases and on the temperature T. The trap characteristics directly impact the shape of the noise PSD of the signal.

The relative drain current RTS amplitude can then be calculated assuming that the trapping of an elementary charge in the channel changes the local conductivity [10]. It has been shown that the relative drain current RTS amplitude for a single trap can be approximated by [11]:

$$\frac{\Delta I_d}{I_d} = \eta\frac{g_m}{I_d}\frac{q}{WLC_{ox}}\left(1-\frac{x_t}{t_{ox}}\right) \qquad (3)$$

where g_m is the transconductance, η a fit parameter, x_t the trap depth with respect to the silicon-oxide interface, t_{ox} the oxide thickness, W and L the width and the length of the transistor, respectively.

By combining time and frequency domain measurements, the Lorentzian plateau evolution for a single trap can be obtained by:

$$P = \frac{2f_t(1-f_t)}{\pi f_c}\left[\eta\frac{g_m q}{WLC_{ox}}\left(1-\frac{x_t}{t_{ox}}\right)\right]^2 \qquad (4)$$

The modeling of the analytical noise PSD can be done using three noise contributions: 1/f noise, R.T.S noise and white noise. The input referred noise voltage PSD is calculated as follows:

$$S_{V_g}(f)=\frac{1}{g_m^2}\left(\frac{\alpha}{f}+\sum_{i=1}^{N_t}\frac{\frac{2f_{ti}(m;\sigma)\,(1-f_{ti}(m;\sigma))}{\pi f_{ci}}\left[\eta\,\frac{g_m q}{WLC_{ox}}\left(1-\frac{x_{ti}}{t_{ox}}\right)\right]^2}{1+\left(f/f_{ci}\right)^2}+4kTG_{d0}\gamma\right) \quad (5)$$

where the parameter α is the flicker noise coefficient, for actual SF under the usual biases, this value is often negligible and so can be set to zero; g_m is the transconductance of the MOS transistor; i is the number of R.T.S contributions induced by i active traps at a same time; f_{ti} is the trap occupation probability taking into account the dispersion aspect for these traps; G_{d0} is the output conductance at zero drain bias and γ is a parameter dependent on the device biasing.

Finally taking into account the CDS modeling [12] the temporal noise is obtained using:

$$Noise=\sqrt{\left(\int_{1Hz}^{100MHz}\left[S_{V_{gs}}(f)\left(\frac{1}{Ts}\sum_{k=-\infty}^{+\infty}X\left(f-\frac{k}{Ts}\right)\right)\cdot\left(\frac{1-e^{(-j2\pi Ts)}}{j2\pi f}\right)\cdot\left(e^{(-j2\pi f\tau)}-1\right)\right]df\right)} \quad (6)$$

All of the five model parameters are directly extracted from only one single transistor (i, $f_{ti}(m;\sigma)$, η, x_{ti}, f_{ci}).

III. RESULTS

The equivalent circuit used in our study is given in the Figure 4. It shows a SF configuration used in the pixel circuit of a CMOS active pixel sensor. The input of the SF, Vg, is proportional to the intensity of the light incident on a photodiode. The signal at the output of the SF transistor is sampled using the two switches CDS1 and CDS2. A 100 µs period pulse train (Ts) controls both switches. The switch gate voltages are delayed by 3.5 µs (θ).

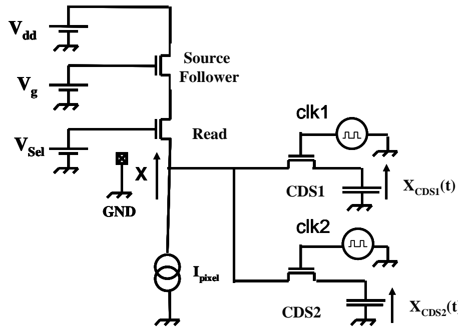


Figure 4: Equivalent Circuit diagram of 4T CMOS Image Sensor pixel used for the modeling of the temporal output simulation.

It has been already shown that an usual noise contribution model (1/f and thermal noise), is not suitable to simulate the output r.m.s. noise from submicron source-follower transistors used in advanced active pixel sensors. This model provides an underestimation of output noise levels (Figure 5) [12]. Then, other noise contribution, namely R.T.S noise, has to be taken into account. With this complementary noise model, theoretical output rms noise values in agreement with experimental ones are obtained.

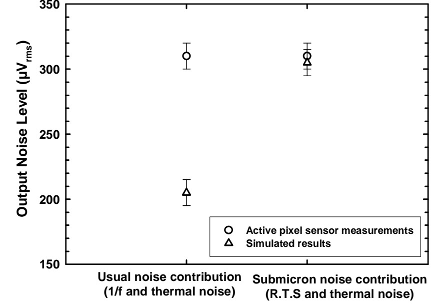


Figure 5: Simulated and experimental output noise values of source follower transistors for an usual noise model (1/f noise and themal noise) and for a noise model including RTS noise.

Nevertheless, the CDS operation acts as a band-pass filter which removes low frequencies (Figure 6). The response of this filter is significantly impacted by variations associated to R.T.S characteristics that strongly depend on design and process considerations. For most of low noise pixels, the RTS noise impact is filter by the CDS. Among all the moderate noisy pixels, the majority exhibit similar noise response. For the noisiest pixels, the RTS noise is not filtered by the CDS.

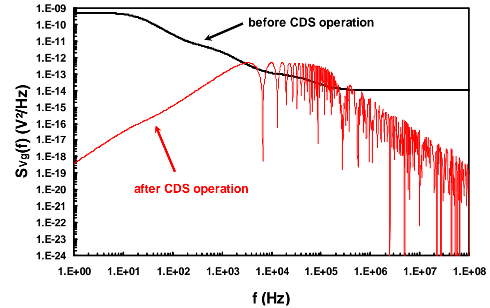


Figure 6: Input source follower noise power spectral density before and after CDS operation taking into account RTS noise.

The experimental dark random noise cumulated population of all pixels is shown in the Figure 7 for various sensors.

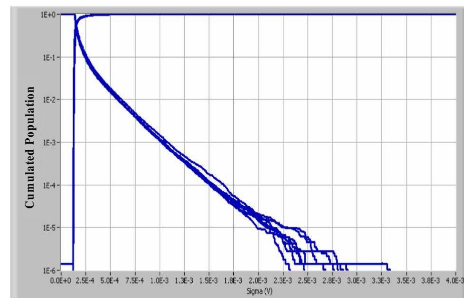


Figure 7: Experimental distribution of temporal noise on several pixel arrays.

The average of this distribution is compared with our model (Figure 8). We can observe that the theoretical noise distribution cumulative population value is in good agreement with experimental ones. Noise levels are in accordance with experimental results.

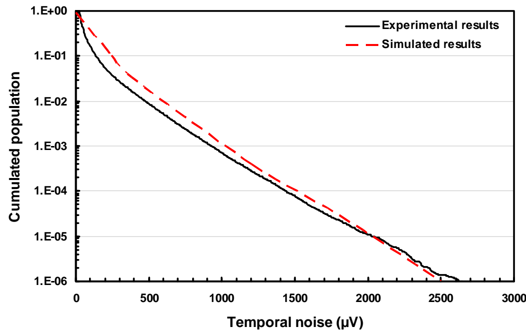


Figure 8: Simulated and experimental temporal noise distribution.

RTS noise characteristics are strongly impacted by design or/and process variation, that is why this model can allow an optimization of these two various aspects. As a result, a gate oxide optimization predicted by this model had been done. Results are shown in Figures 9 and 10.

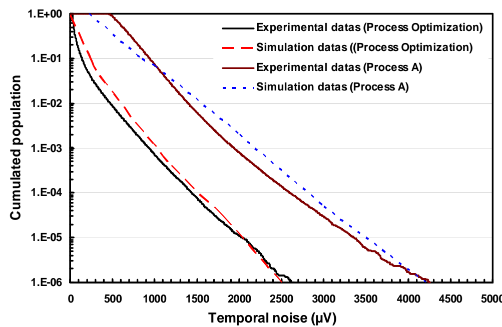


Figure 9: Simulated and experimental temporal noise distribution for two processes. The model takes into account and can lead to a process variation for the optimization of the temporal noise.

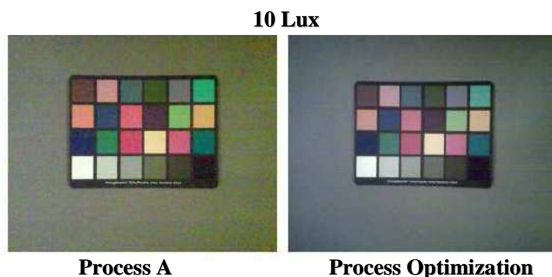


Figure 10: Benefits of process and/or design optimization using temporal noise distribution modeling on CMOS image sensors sensitivity.

IV. CONCLUSION

For the first time, the temporal output is modeled in a full array 4T CMOS image sensors pixels using RTS noise contribution. This model is only based for calibration on a single transistor noise characterization without processing the sensors. The actual sensor read noise is dominated by the SF RTS noise. The output noise distribution modeling is a key point in order to improve the RTS noise impact in CMOS imager by design or/and process optimization. Using this model, noise distribution can be predicted without the use of a full pixel array. For a given image sensor technology this model could allow the determination of a good source follower geometry based on a single transistor characterization in order to improve noise performances.

REFERENCES

[1] X. Wang, P.R. Rao, A. Mierop, A.J.P. Theuwissen, 'Random Telegraph Signal in CMOS Image Sensors Pixels', IEEE Proceedings, IEDM 2006.

[2] C.Leyris, F.Martinez, M.Valenza, A.Hoffmann, J.C.Vildeuil, F.Roy, 'Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels', IEEE Proceedings, ESSCIRC 2006.

[3] F.N. Hooge , IEEE transaction on electron devices, VOL41, pp 1926.

[4] A.L.McWhorter, in R.H Kingston (Ed.), Semiconductor Surface Physics, University of Pennsylvania, Philadelphia, pp 207.

[5] K.K. Hung, P.K. Ko, C. Hu and Y.C. Cheng, "A Physics-Based MOSFET Noise Model for Circuit Simulators ", IEEE transaction on electron devices, VOL 37-, NO 5, pp 1323-1333.

[6] S. Machlup, 'Noise in Semiconductors: Spectrum of a two parameter Random Signal', Journal of applie. Physics, VOL 25, pp 341.

[7] E.Simoens and C.Clays, 'Random Telegraph Signal: a local probe for single point defects studies in solid-states devices', Materials Science and Engineering, B91-92 (2002).

[8] K.S. Ralls,W.J. Skocpol, L.D. Jackel, R.E. Howard, L.A. Fetter, R.W. Epworth, and D.M. Tennant, "Discrete Resistance Switching in Submicrometer Silicon Inversion Layers: Individual Interface Traps and Low-Frequency (1/f?) Noise ", Physical Review Letters, VOL 52, NO 3, pp 228-231.

[9] C. Leyris, A. Hoffmann, M. Valenza, J-C Vildeuil and F. Roy, " Trap competition inducing R.T.S noise in saturation range in N-MOSFETs", Fluctuation and Noise Processing. Proceedings of the SPIE, Volume 5844, pp. 41-51.

[10] M.J Kirton. and M.J Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states, and low-frequency noise", Advances in Physics, VOL 38, NO 4, pp 367-468 .

[11] O. Roux dit Buisson and al, 'Explaining the amplitude of RTS noise in sub micrometer MOSFET's', Solid State Electronics 1992;35(9):1273.

[12] C. Leyris, F. Martinez, M. Valenza, A. Hoffmann, J.C. Vildeuil and F. Roy, "Response of Correlated Double Sampling CMOS Imager Circuit to Random Telegraph Signal Noise", IEEE Proceedings, ICCDCS 2006.

Characterization of the Buried Channel n-MOST Source Followers in CMOS Image Sensors

Xinyang Wang, Padmakumar R. Rao, Albert J.P. Theuwissen
Delft University of Technology, Delft, the Netherlands

ABSTRACT

The performance of CMOS image sensors in a deep sub-micron CMOS process is limited by two factors: 1) The increasing pixel temporal noise floor dominated by the 1/f noise from the pixel source follower (SF) and 2) The decreasing pixel analog swing due to the supply voltage scaling. In this paper, we present the possibility of using a buried channel n-MOST as the in-pixel source follower to reduce noise and enhance the pixel analog swing.

INTRODUCTION

Recent research has proved that the 1/f noise induced by traps located in the silicon silicon-oxide interface of SF gate region becomes dominating in the pixel read noise floor of CMOS image sensors. [1, 2] In modern CMOS processes, the gate area becomes so small; it is possible that there is only one active interface trap, which induces the so call "random telegraph signal" (RTS) noise as shown in Fig 1. Because of the single electron trapping and detrapping during operation, the pixel output after the correlated double sampling (CDS) produces three discrete levels. Our recent study found that this one-trap-induced RTS noise still dominates the pixel temporal noise. [3, 4] Therefore, if an absolute clean gate interface can not be guaranteed, the 1/f or RTS noise will stay dominant.

Previous research showed also that the 1/f noise of p-MOSTs is generally smaller than n-MOSTs because of their natural buried channel. [5,6] Therefore, a very straightforward solution to reduce the 1/f noise is to "bury" the conducting current, i.e. creating a buried channel n-MOST source follower in modern CMOS imager process.

The sensor's saturation level, therefore the dynamic range, is determined by the photodiode full well capacity, conversion gain and the maximum pixel output swing. The absolute output swing can be determined by the following equation:

$$V_{swing} = V_{rst} - V_{FD} - V_{SFth} - V_{col}$$

From which, V_{rst} is floating diffusion (FD) voltage after reset, which is one threshold drop from the pixel power supply regardless the reset mode, V_{FD} stands for the voltage drop due to FD dark current, V_{SFth} is the threshold drop across the SF, V_{col} is the minimum voltage required at the column to bias the current source. The pixel power supply scales with the process. Therefore, the output swing decreases because of the decreasing Vrst. Because the buried channel n-MOSTs are depletion mode devices with negative V_{SFth}, the output swing will therefore be enhanced.

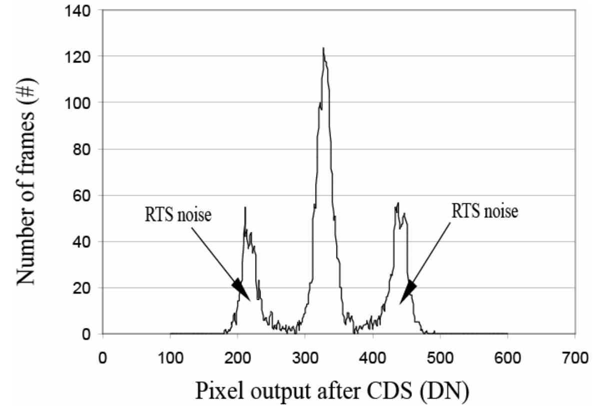


Figure 1. Histogram of dark temporal noise of a RTS pixel

SIMULATION STUDY

Fig 2 plots the cross-section of the buried channel n-MOST device simulated by SUPREM. The original simulation files are supplied by TSMC, describing the standard fabrication steps of an in-pixel SF in 0.18μm CMOS process. An extra implantation step is added to create buried channel n-MOST.

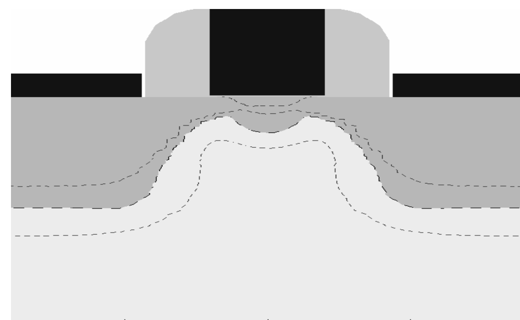


Figure 2. Simulated buried channel n-MOST in TSMC 0.18um CMOS process, the dashed line is the boundary of the depletion region.

As shown in the Fig 2, a fully-depleted gate interface can be achieved at zero volt gate bias condition. The max channel potential and buried depth are determined by the doping energy and dose.

Test structures have been fabricated in TSMC 0.18µm CMOS process with five different buried channel implant energy and dose combinations. Fig 3 is a comparison of the simulated and the measured gate characteristic of the buried channel transistors. As expected, increasing the implantation dose will shift the transistor threshold voltage towards negative. As shown, the extracted threshold voltages are less negative than the simulated ones; the difference is bigger for higher implant doses. Increasing implantation energy will slightly increase the channel depth, however, with the penalty of a large leakage current. Therefore, the implantation dose and energy need to be adjusted carefully to obtain an optimized channel depth and threshold voltage.

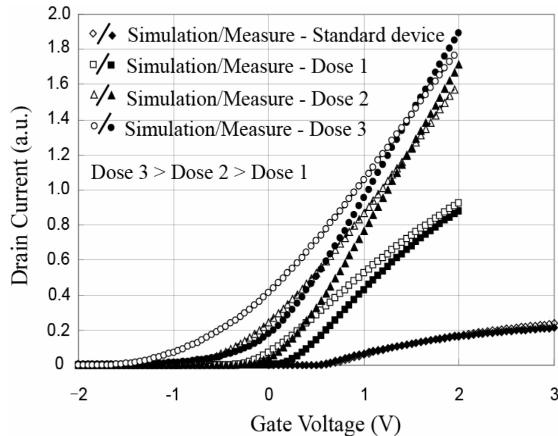


Figure 3. Simulation and measurement of the gate characteristic for different buried channel n-MOSTs, with same implant energy but different doses

MEASUREMENT RESULTS

Both single transistors and pixel test structures were fabricated for measurements and characterizations. Fig 4 is the schematic of the pixel test structure and the column bias circuitry used to measure the pixel output swing. The pixel is a standard pinned 4T design without the row select transistor.

Fig 5 plots the measurement results of the absolute pixel output swing. During the measurement, the reset transistor (RST) gate is tied to the highest voltage of the pixel, i.e. performing hard reset, and the transfer gate is switched off. Therefore, the FD voltage equals the reset transistor power supply. The column bias current is 6uA for all pixels. As shown, because of pixel output swing improves drastically.

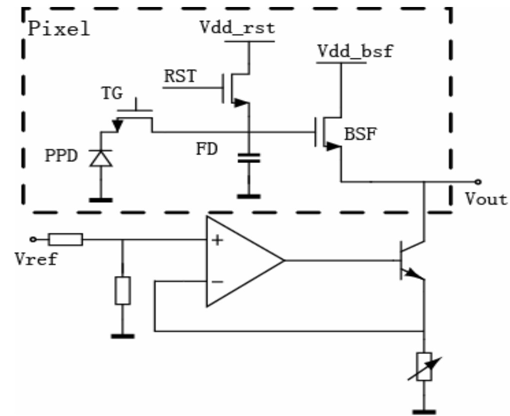


Figure 4. Pixel schematic and column bias circuitry with buried source follower (BSF), reset transistor (RST), transfer gate (TG), pinned photodiode (PPD) and separated power supply to the BSF (Vdd_bsf) and RST (Vdd_rst)

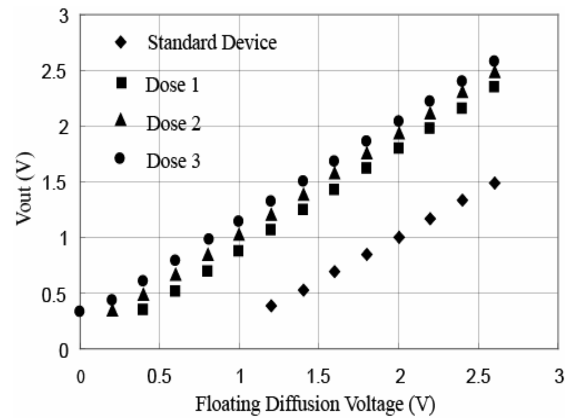


Figure 5. Measurement of the absolute pixel output swing, pixels with standard SF and BSF

Interestingly, from Fig 5, we are also able to observe an improved voltage gain for buried channel device, (>0.9) compare to the standard surface mode device (0.83).

Fig 6 is the 1/f noise measurement setup for single transistors. The DUT is biased as the source follower operation with the drain tied to 3.3V and 6uA conducting current. The gate of the DUT is biased by a normal DC source with a 1Hz filter in order to block all AC components. The drain is tied to a battery power supply. The conducting current is compensated by a battery powered current source. The test devices and the battery are in a sealed box. Fig 7 plots the measured 1/f noise power spectrum density of a surface and a buried channel test device with the same dimensions. We find that the slope of the curves for buried channel devices are normally between -0.6 and -0.8, which indicates a different noise mechanism from the surface origin of the standard n-MOSTs. As shown, the low frequency noise of the buried channel device is significantly

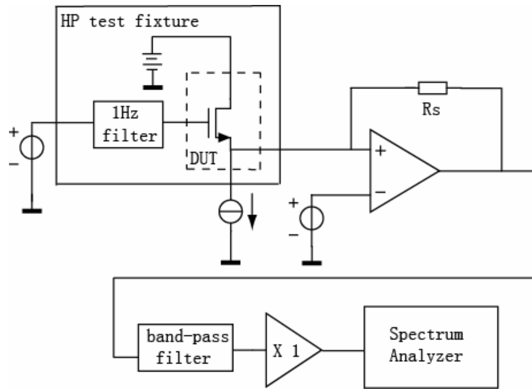


Figure 6. 1/f noise measurement setup for buried / surface channel n-MOSTs under source follower bias condition

reduced. However, the 1/f dominated read noise of CMOS imagers is the product of the 1/f PSD and the CDS transfer function. Therefore, the noise reduction efficiency highly depends on the CDS period as well as the frequency of the crossing point is Fig 7.

Complete image sensor with BSFs was made. The pixel pitch is 7.4µm, with power supply of 3.3V. Fig 8 is the dark random noise measurement histogram. The random noise of each pixel is taken by calculating the standard deviation of the pixel outputs through 20 frames. The measurement is done in complete dark. In order to exclude the dark current shot noise effect, the transfer gate is switched off during two sample and hold periods of the CDS.

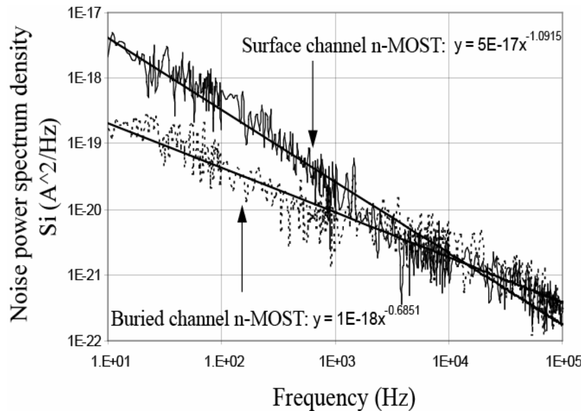


Figure 7. 1/f noise measurement for surface/buried n-MOSTs

The histogram is plotted in linear scale in order to highlight the noise improvement of the majority pixels instead of those “hot” ones. As shown, both the mean and the σ value of BSF pixels’ noise are reduced.

CONCLUSIONS

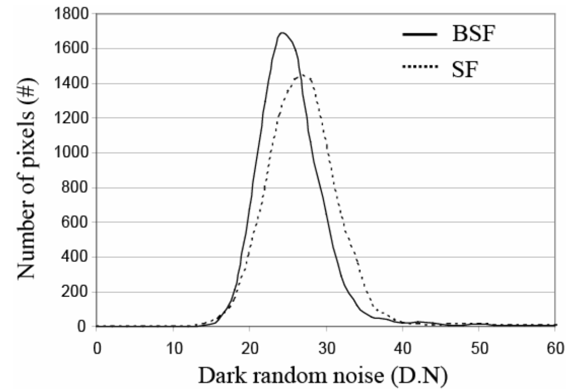


Figure 8.Dark random noise histogram for buried/surface SF pixels

Buried channel n-MOSTs are successfully made through deep sub-micron CMOS process and being characterized regarding their source follower application in CMOS image sensor pixels Because of a ‘buried’ conducting current, the following advantages are reported from the our measurement and characterizations: 1) 1/f noise is significantly reduced. 2) The pixel output swing is enhanced drastically. 3) The SF voltage gain is increased.

ACKNOWLEDGEMENT

The authors would like to thank the CMOS imager group of DALSA BV for their helps on designing the test sensor, and TSMC for their generous offer to make this research possible. This work is sponsored by the Dutch Technology Foundation (STW).

REFERENCES

[1] Bedabrata Pain et.al. “Excess noise and dark current mechanisms in CMOS imagers”, pp145-148, IEEE Workshop on CCDs & AIS, June 2005

[2] Jung Yeon Kim et.al., “Characterization and improvement of random noise in 1/3.2” UXGA CMOS image sensor with 2.8um pixel using 0.13-technology” pp149-152, IEEE Workshop on CCDs & AIS, June 2005

[3] Xinyang Wang et.al. “Random telegraph signal in CMOS image sensor pixels”, pp115-118, IEDM, Dec 2006

[4] Leyris C et.al. “Impact of random telegraph signal in CMOS image sensors for low-light levels”, pp276-379, ESSCIRC, Sep 2006.

[5] L.L.J.Vandamme et.al, “1/f noise in MOS devices, mobility or number fluctuations” IEEE Trans on Electron Device, Vol. 41, pp1936-1945, Nov, 1994

[6] Jimmin Chang et.al, “Flicker Noise in CMOS Transistors from subthreshold to strong inversion at various temperatures” IEEE Trans on Electron Device, Vol. 41, pp1965-1971, Nov 1994

Column Parallel Signal Processing Techniques for Reducing Thermal and RTS Noises in CMOS Image Sensors

Shoji Kawahito and Nobuhiro Kawai
Research Institute of Electronics, Shizuoka University
3-5-1, Johoku, Hamamatsu, 432-8011, Japan
kawahito@idl.rie.shizuoka.ac.jp

Abstract

This paper presents column parallel signal processing techniques for reducing thermal and RTS noises of in-pixel source followers. Noise reduction methods of correlated multiple sampling differential averaging (CMSDA) and histogram-based RTS-noise suppression and averaging (HRNSA) are applied and their effectiveness for RTS noise reduction is demonstrated for large sampling number.

1. Introduction

The pinned photodiode technology greatly reduces the dark current and cancels the kTC noise of CMOS image sensors (CIS's), and as a result, the major interest for low-noise CIS's has been shifted to the noise due to transistors of in-pixel source follower amplifiers. The reduction of anomalously large noise, so-called random telegraph signal (RTS) noise in the source follower is becoming a most important issue for low-light-level applications of the CIS[1][2][3]. We investigate for the first time the effectiveness of column parallel signal processing techniques for reducing the source follower RTS noise.

2. Signal Processing Architectures for RTS and Thermal Noise Reduction

Fig. 1 shows the block diagram of a CMOS image sensor with column-parallel mixed-signal processing circuits for noise reduction. Advanced CMOS technology allows us to integrate sufficient amount of circuits in each column, and sophisticated mixed analog-digital signal processing can be implemented.

The basic idea for the noise reduction is based on multiple sampling for both signal and reset levels of the pixel output as shown in the timing diagram of Fig. 2.

2.1 Correlated Multiple Sampling Differential Averaging (CSMDA)

A simple but effective noise reduction technique using multiple samplings is a correlated multiple sampling differential averaging (CSMDA). Fig. 3 shows pre-amplified CSMDA circuits. The high-gain switched-capacitor (SC) pre-amplifier is very effective for reducing thermal noise reduction if a freeze noise component is cancelled in the next stage [4]. The pre-amplifier output is sampled and digitized for multiple times using an A/D converter for both the reset and signal levels as shown in the timing diagram of Fig. 2. CDS (correlated double sampling) of the sampled reset and signal levels is carried out in digital domain. The operation of the CMSDA can be described as

$$V_{OUT} = \frac{1}{M}\sum_{i=1}^{M}\left(V_S(i) - V_R(i)\right) \quad (1)$$

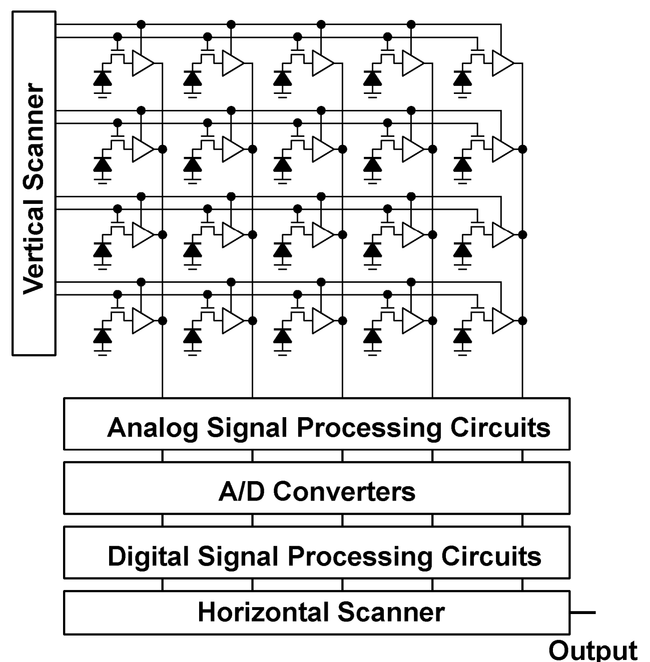


Fig. 1 CIS architecture with Column-Parallel Mixed-Signal Processing Circuits.

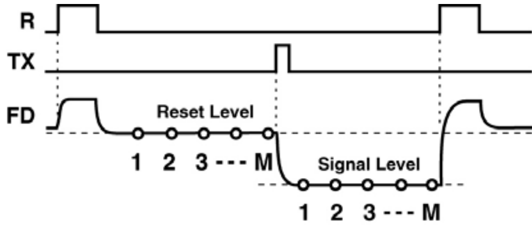


Fig. 2 Timing Diagram of the multiple sampling for both reset and signal levels.

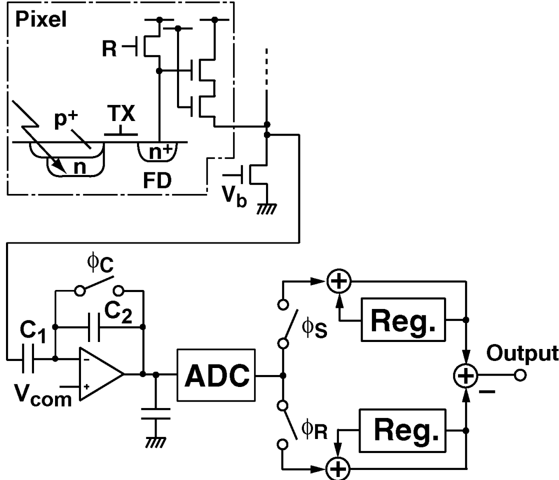


Fig. 3 Pre-amplified CSMDA circuits.

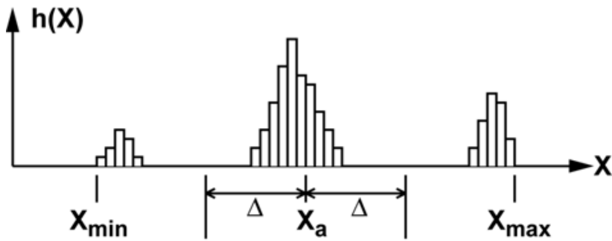


Fig. 4 Histogram of RTS-noise after CDS.

where $V_S(i)$ and $V_R(i)$ are the i -th sample of signal and reset levels of the preamplifier output.

2.2 Histogram-based RTS-Noise Suppression and Averaging (HRNSA)

For suppressing RTS-noise more effectively, a histogram of multiple samples is used. Fig. 4 shows a histogram of RTS-noise in $V_S(i)$-$V_R(i)$, i=1,…,M. If large RTS noise exists, three peaks appear as shown in Fig.4. The right and left peaks are due to the RTS noise and the center peak corresponds to the signal level without influence of the RTS noise. In order to reduce the RTS noise as well as the thermal noise, the following process is carried out. First, the maximum and minimum values in the histogram are detected, and then the average of the maximum and minimum X_m is calculated as

$$X_m = \frac{X_{max} + X_{min}}{2}. \qquad (1)$$

The average is located around the center peak. To estimate the signal level by reducing thermal noise, the average of histogram in the range from X_a - Δ, and X_a + Δ is calculated.

$$Y = \sum_{X=X_m-\Delta}^{X_m+\Delta} h(X)X \Bigg/ \sum_{X=X_m-\Delta}^{X_m+\Delta} h(X) \qquad (2)$$

The range parameter Δ can be chosen, for instance, as 3 times r.m.s. thermal noise amplitude. This signal processing method is called here a histogram-based RTS-noise suppression and averaging (HRNSA). The block diagram of the HRNSA circuits if it is implemented at the column of the CMOS image sensors is shown in Fig. 5.

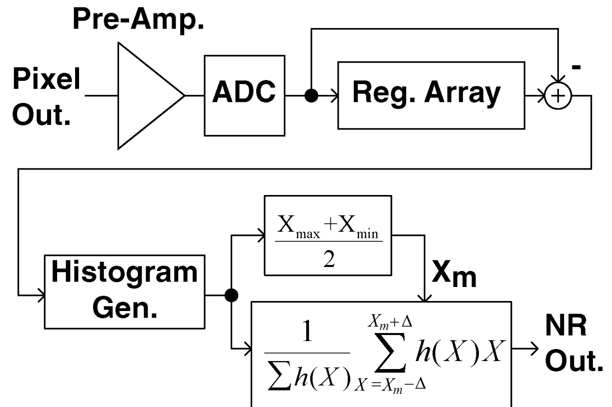


Fig. 5 Pre-amplified HRNSA circuits.

2.3 Analog Implementation of CMSDA.

The CMSDA circuits can also be implemented with an analog switched capacitor integrator. By using polarity inversion in the SC integrator, the function of the difference of multiple samples can be realized.

3. Experimental Results

To measure the noise reduction effect of the CMSDA and HRNSA for the RTS noise, a prototype CMOS image sensor is implemented with 0.18μm pinned-photodiode CMOS technology (Fig. 6). Though this CMOS image

sensor chip has a column parallel pre-amplifier and the CMSDA circuit implemented with an analog integrator, the pre-amplifier output can also be directly monitored through a test port for external processing. The following measurement is carried out with an external processing. The data are obtained by digitizing the pre-amplifier output with a 14-bit ADC at 500ksamples/s.

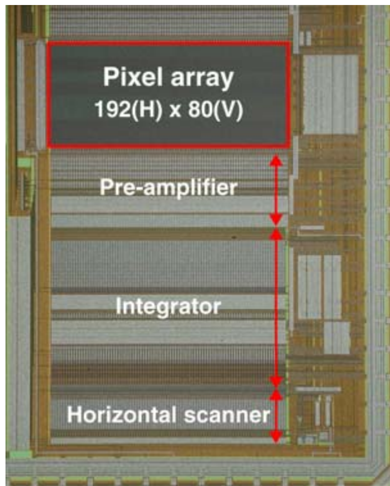
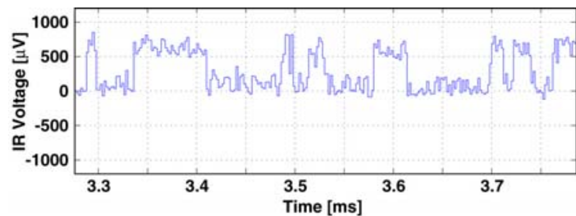
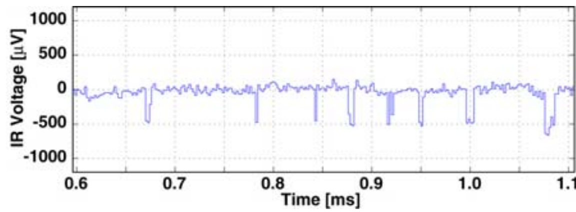


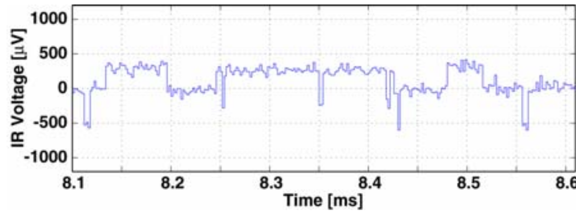
Fig. 6 Implemented Prototype Chip (0.18μm CIS with Pinned Photodiode).



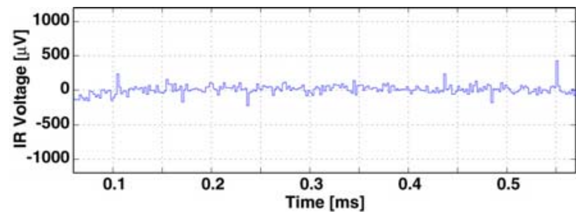
(a) Slow relaxation-time RTS noise



(b) Fast relaxation-time RTS noise



(c) Three level RTS noise



(d) Non-RTS noise

Fig. 7 Measured RTS Noise.

Fig. 7 shows 4 types of pixel source follower noises monitored through the SC pre-amplifier with a gain of 32 under dark condition; fast relaxation-time RTS, slow relaxation-time RTS, three-level RTS, and Non-RTS noises.

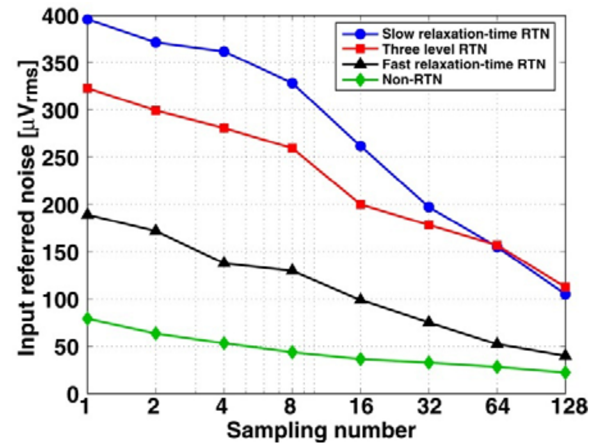


Fig. 8 Effect of the Pre-Amplified CMSDA for Reducing RTS Noises.

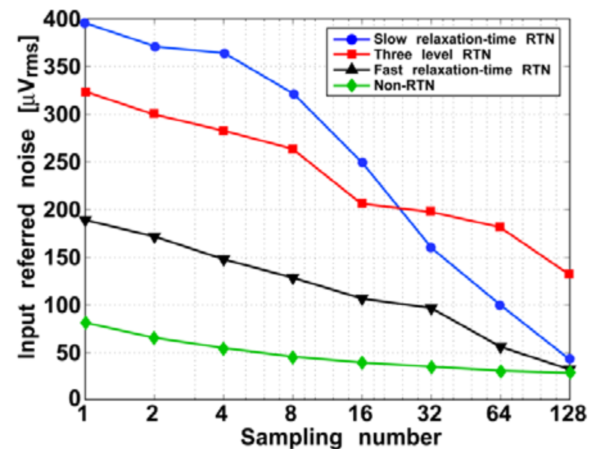
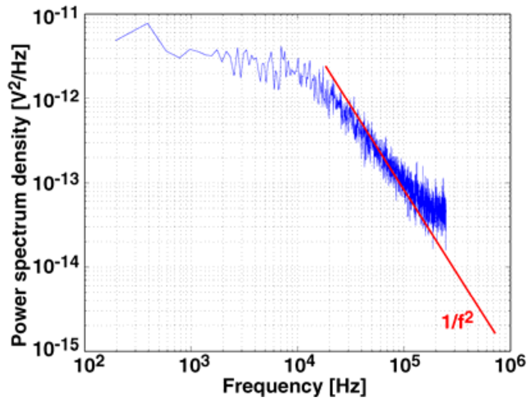
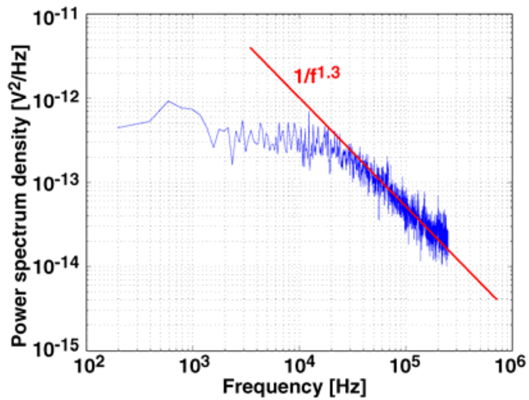


Fig. 9 Effect of the Pre-Amplified HRSNA for Reducing RTS Noises.

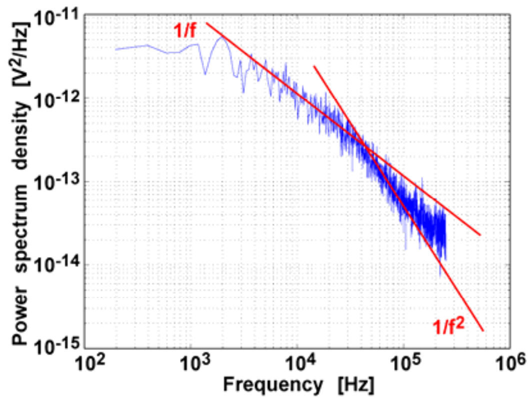
Figs. 8 and 9 show the relationship between the input-referred noise and the number of samplings for 4 different kinds of RTS noise patterns of Fig. 7 for the noise reduction method of CMSDA and HRNSA, respectively. Both methods have a great noise reduction



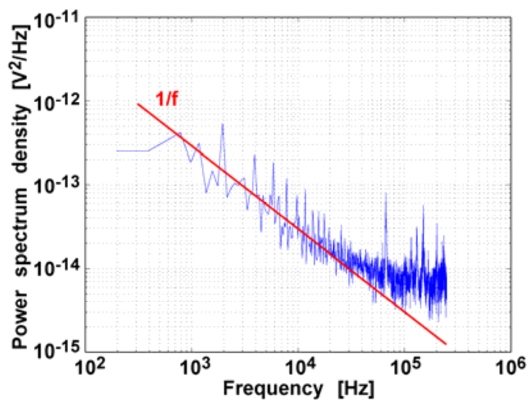
(a) Slow relaxation-time RTS noise



(b) Fast relaxation-time RTS noise



(c) Three level RTS noise



(d) Non-RTS noise

Fig. 10 Spectrum of RTS of Fig. 6

effect for the RTS noise if the number of samplings is large enough. The HRNSA has better performance for slow relaxation-time RTS compared with the CMSDA. Both methods are not so effective for the three-level RTS and non-RTS noise. The reason could be explained with the spectra of these noises shown in Fig. 10. In the RTS-noise of Fig. 7(a) and (b), flat spectrum region extends over relatively higher frequency, while in the noise of Fig. 7(c) and (d), flat spectrum region appears only in low frequency region. The low-pass filtering function or band-narrowing effect in the CMSDA and HRNSA can effectively suppress the noise if the noise spectrum is flat.

4. Conclusions

This paper treats noise reduction methods for thermal and RTS noises of in-pixel source followers and their effectiveness is confirmed with an implemented chip. Because of the relatively large processing time, the signal processing techniques are useful for CIS's with moderate frame speed, in the field of scientific measurements.

ACKNOWLEDGMENTS

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REFERENCES

[1] K. M. Findlater et al., "Source follower noise limitations in CMOS active pixel sensors, Proc. SPIE, vol. 5251, pp. 187-195, 2004.

[2] X. Wong et al., "Random Telegraph Signal in CMOS image sensor pixels, "Tech. Dig., IEDM, 2006.,

[3]M. F. Snoeij et al., "The effect of switched biasing on 1/f noise in CMOS image sensor front-ends, "Proc. IEEE Workshop CCD and AIS, pp. 68-71, June 2005.

[4]N. Kawai, S. Kawahito, "Noise analysis of high-gain low-noise column readout circuits for CMOS image sensors",IEEE Trans. Electron Devices, vol.51, no.2, pp.185-194 ,2004.

Optimization of Random Telegraph Noise Non Uniformity in a CMOS Pixel with a pinned-photodiode

Assaf Lahav[1], Dmitry Veinger, Amos Fenigstein and Amit Shiwalkar[2]

The main advantage of a 4T CMOS pixel (Figure 1a) which incorporates a pinned PD is the low reset noise and ultra low Dark Current (DC). In principle when the transfer of electrons from the PD to the FD is fully optimized, the reset noise can be eliminated completely by the Correlated Double Sampling (CDS) of the Reset and Signal (Figure1b). Moreover, by proper optimization of the diode and Transfer Gate the DC and DC distribution can be reduced significantly. In this case the limiting factor to the image quality in low light becomes the temporal noise associated with the Source Follower (SF) Transistor[1].

In fact, in state of the art sensors the mean value of the SF temporal noise is inherently low enough due to band-pass filter imposed by the CDS operation [2]. The main limit for good image quality in low illumination becomes the non-uniformity associated with this noise. In Figure 2 the cumulative population of two different arrays (each array contains 480x640 2.2um pixels). The first array contains pixel with optimized SF and the second array pixel with standard SF. It can be seen that while both arrays has similar mean temporal noise well below 10e, the distribution (noise non-uniformity) is completely different: for the optimized SF array only 1% of pixels has temporal noise >10e whereas for the STD SF array 10% of the pixels has temporal noise >15e. The wide distribution of temporal noise causes two main problems: in low illumination condition (assuming low dark current as shown in Figure2) it will set a limit for the maximum analog gain which can be applied to the picture before it becomes grainy; in video applications even at high illumination it will cause some pixel to blink in the darker area of the picture.

In order to reveal the nature of this temporal noise non-uniformity and optimize our process and pixel layout we designed an engineering VGA array with 4um pitch. With this array along with is peripheral test board we could measure temporal noise as low as 150uV. Other features for this engineering array where complete control on pixel timing and voltages. For example one can choose quite simply not to open the TG in the read sequence. In that case the CDS operation should result zero with the uncorrelated SF noise; i.e. with this special timing we could distinguish between noise coming from incomplete transfer to the noise coming from the SF.

Several pixels with different designs for their SF where placed on the engineering VGA array in smaller mini-arrays of 150x150 pixels. In Figure 3, the cumulative plots for the temporal noise of three different mini-arrays are shown. The only change between the pixels is the size of SF transistor channel: pixel (a) has W/L of 0.4/0.4 pixel (b) has W/L of 0.8/0.4 and pixel (c) has W/L of 0.4/0.8. The inner frame in figure three shows time distribution histogram of two individual pixels from the miniarray with pixel (a). The dotted line represent "quiet" pixel – pixel which his noise pattern is similar to 90% of array population. The bold line represent "noisy" pixel – pixel which only 0.1% of the population is similar or worse. The "quiet" pixel is clearly showing one main value with some distribution around it. This noise pattern is typical to

[1] Tower Semiconductor LTD, P.O.Box 619 Migdal Haemek, Israel, e-mail:asafla@towersemi.com, TEL:(972)-4-6505063, FAX:(972)-4-6547788
[2] Biomorphic VLSI Inc

standard 1/f and temporal noise of a SF transistor under CDS operation [3]. However it is clearly seen that the noisy pixel is going through three different values. The right and left peaks are separated by the same voltage from the central peak. This is the main characteristic of a Random Telegraph Noise with one trap [4]. The magnitude of the noise – distance between peaks depends on the distance of the trap from the source of the SF (closest to the source highest magnitude). The time constant associated with this noise is in the order of usec or less which indicates low activation energy or very shallow traps.

Returning to cumulative plots of Figure 3, we can see that the number of "noisy" pixels strongly dependent on the SF dimensions. Pixel (b) and pixel (c) has the same area but different W/L however there noise performances are quite different. The number of "noisy" pixels is dramatically reduced when comparing pixel (c) to pixel (b) and (a). Thus the most effective parameter (in a given process) for reducing the number of "noisy" pixels is making the SF longer. This phenomenon can be explained by the segregation of the channel implant (Boron) into the Shallow Trench Isolation (STI) walls which is making the threshold voltage near walls smaller than the threshold voltage at the middle of the channel. This enforces most of the SF current to flow in the vicinity of the interface between the STI walls and transistor gate oxide. Most of the low activation energy (short life time) are located along this interface and the probability to find only one trap is decreasing with channel length.

Finally the importance of the delay between reset read and signal read (designated by τ at Figure 1b) is emphasized by comparing the noise pattern of the two lines plotted for pixel (c) on Figure 3. The bold line is taken with τ=6usec and the dashed line is taken with τ=100usec. It can be seen that increasing τ, increases the temporal noise of all pixels. However the number of "noisy" pixels increases more significantly due to activation of different traps which where masked by the CDS operation for shorter τ.

In this paper we have shown that noise characteristics across the array are very different between "quiet pixels" (mean <10e) and noisy ones. Furthermore it is shown that while the "quiet pixels" exhibit regular 1/f noise typical to small transistors in modern CMOS technology, the "noisy pixels" exhibit Random Telegraph Noise (RTN) pattern with very short time constant. It is shown that for a given process conditions the main parameter for improving the array RTN non uniformity is the channel length of the SF. It is claimed that the single trap responsible for the traping-detraping process is located near the edge defined by the SF active channel, the transistor gate oxide and the shallow trench isolation along the SF.

References

[1] C. Leyris et al., "Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels", Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European, pp 376-379, 2006

[2] Y. Degerli et. al., “Analysis and reduction of signal readout circuitry temporal noise in CMOS image sensors for low-light levels”, IEEE Transactions on Electron Devices, vol. 47, no.5, pp. 949-962, May 2000

[3] Hui Tian et al., "Analysis of 1=f Noise in Switched MOSFET Circuits", IEEE TRANS. ON CIRCUITS AND SYSTEMS—II:, VOL. 48, NO. 2, 2001

[4] M.J Kirton etal. , “Noise in solid-state microstructures: Anew perspective on individual defects, interface states, and low frequency noise”, Advances Physics, VOL 38, NO 4, pp 367-468, (1989)

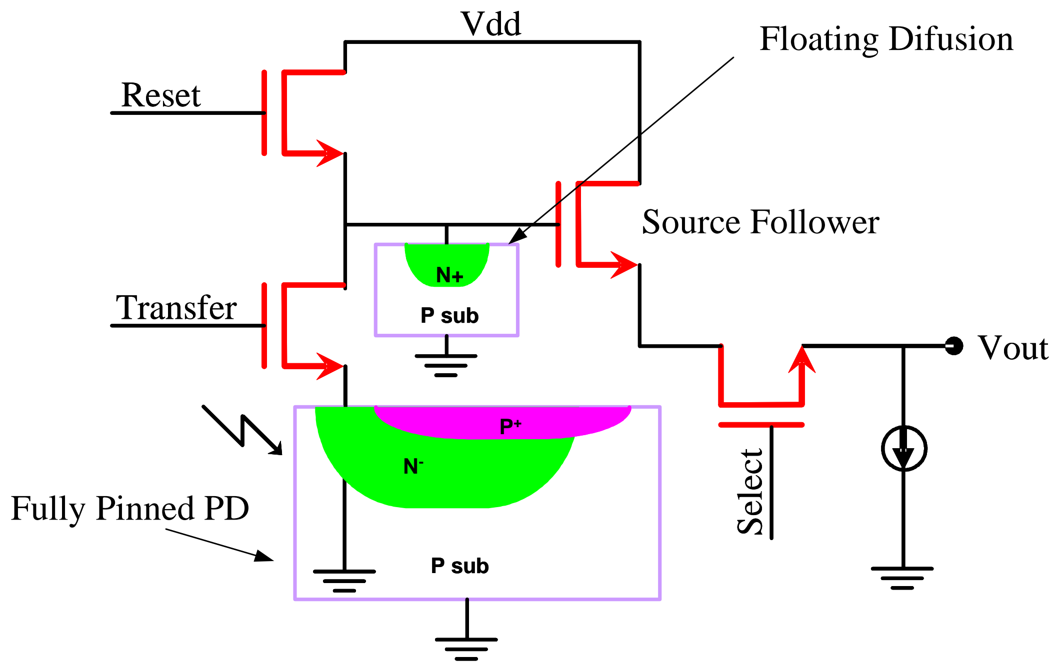

Figure 1(a) – Schematics of a 4T pixel with a fully pinned Photo Diode

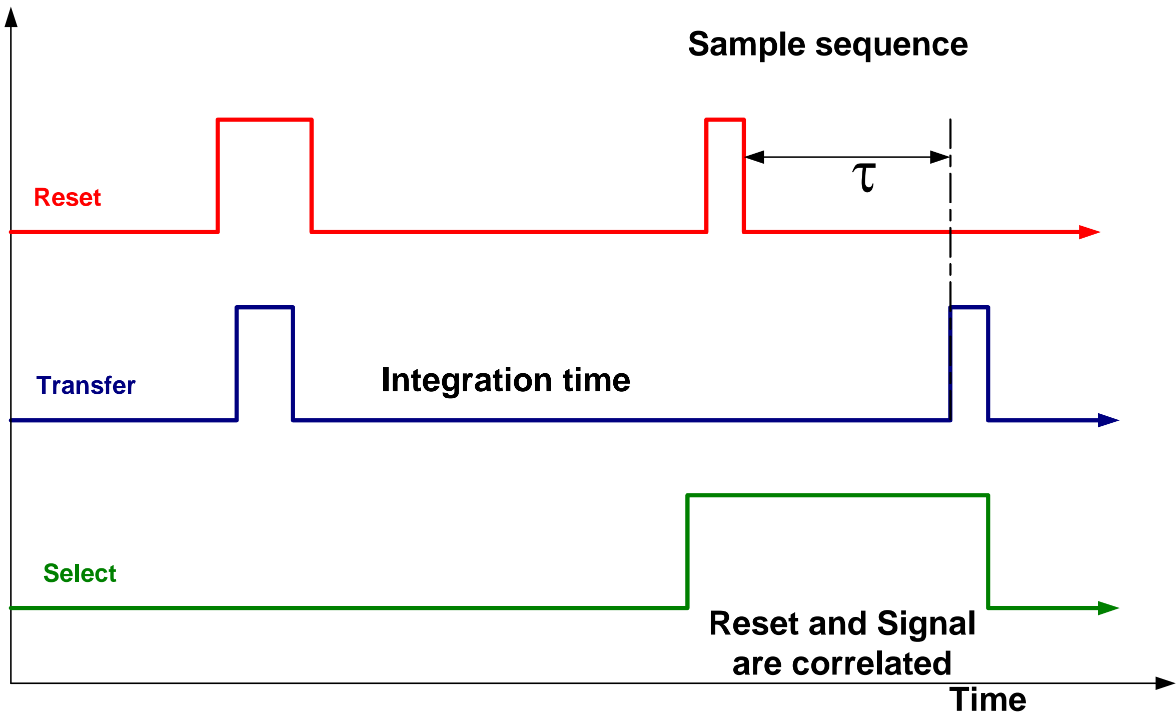

Figure 1(b) – Schematics of a double correlated sampling sequence for a 4T pixel with a fully pinned Photo Diode

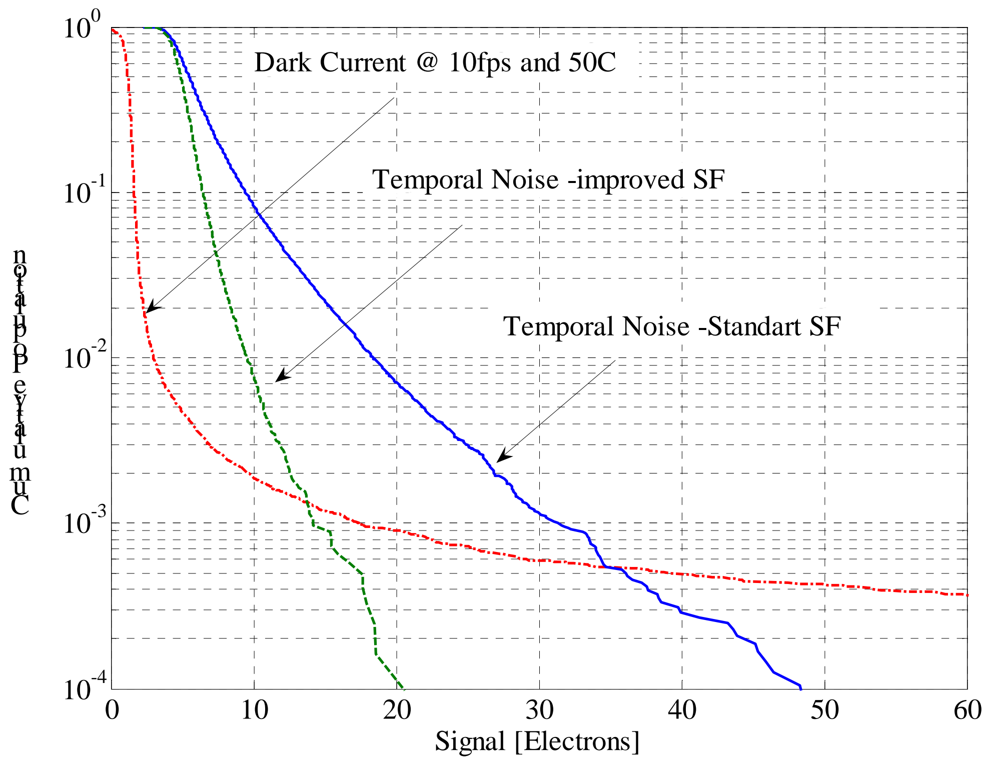

Figure 2 - Distribution of the Dark Current and Temporal noise across a 2.2um pixel array.

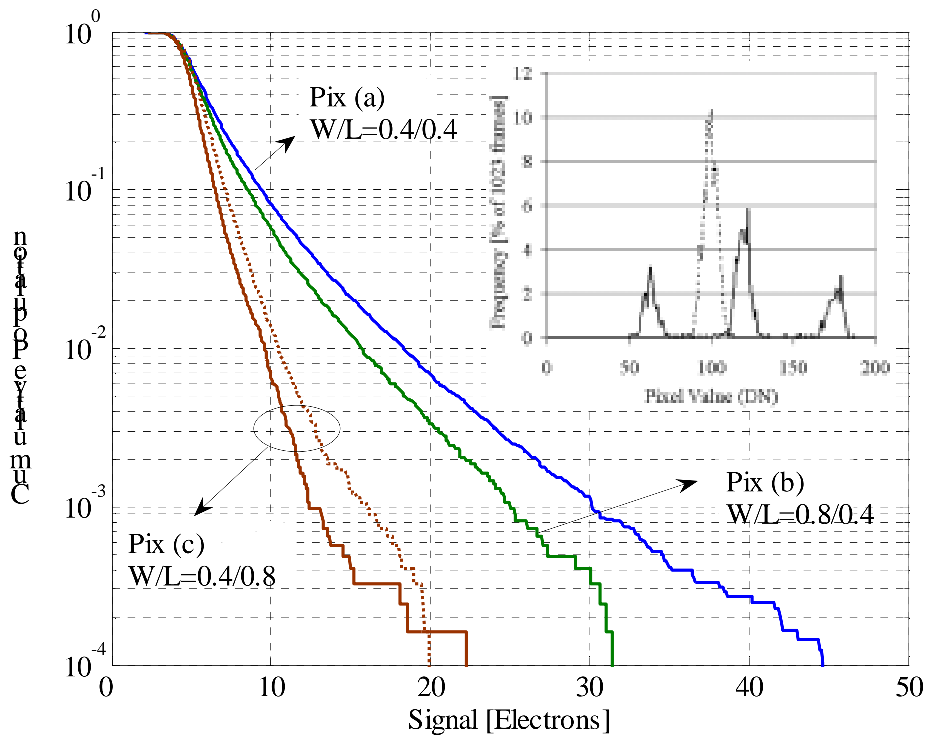

Figure 3 – Distribution of Pixel temporal noise within miniarray of 150x150 pixels for three different SF sizes; inner frame: Occurrence of pixel value (short integration time in dark) in 1023 consecutive frames for typical "quiet" (below 10^{-1} in the cumulative plot) and typical "noisy" pixel (above 10^{-3} in cumulative plot)

Twinkling Pixels: Random Telegraph Signals at Reset Gate Edge

Bedabrata Pain, Bruce Hancock, Chao Sun, and Chris Wrigley
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov

As a result of a significant lowering of dark current in CMOS imager pixels, as well as the introduction of deep sub-μm processes, several secondary dark current sources are becoming detectable, often greatly impacting the spatial distribution of these two metrics. While modal values of dark current have fallen below 50 pA/cm^2, the spatial distribution is far from gaussian – the tail of the distribution easily extending ten times larger than the modal value. There are several reasons for the dark current tail - the presence of isolated metallic impurities, electric field induced dark current enhancements, a distribution of the spatial location of the metallic impurities near the offending junction, hot electron effects being some of the causes [1,2,3].

Usually, the dark current is found to be the results of a stationary statistical process – i.e. repeated measurements yield statistically similar results. In this paper, we report the results from measurements on a 512x512 format imager that had isolated pixels exhibiting non-stationary characteristics. Non-stationarity was observed in form of pixels whose dark current would vary from frame to frame – giving rise to a twinkling effect.

Non-stationary behavior in CMOS imager pixels have been previously reported, and is linked to random telegraph signals (RTS) that are generated within the source-follower channel [4,5,6,7,8,9]. RTS is shown to be a major source of temporal noise in CMOS imager pixels implemented in a deep sub-micron technology [10]. However, in the image sensor we evaluated, the twinkling behavior was not due to RTS in the source-follower, but was directly linked to the sense node dark current.

Figure 1a shows a "3T" pixel schematic and the schematic cross-section of the sense node. It consists of a sense node buffered by a switched source-follower, the source-follower itself being the source of the reset FET. The sense node is reset by momentarily pulsing the reset line (RST) to V_H. During exposure, the reset FET is shut off by returning the reset line to V_L, and charge accumulated on the sense node. The pixels (with 12 μm pixel pitch) were implemented in a 0.15 μm 1 poly 4 metal CMOS process.

To better investigate the twinkling phenomena, we collected data from the twinkling pixels using the timing pattern shown in figure 2. First, the pixel was reset, and the reset signal was sampled. The reset FET was then turned, and its gate was held at V_L=0.5V. The pixel output (corresponding to the sense node potential V_S) was then sampled in regular intervals of 7.8 msec upto a maximum of 2 sec, after which the pixel was reset, and the experiment was repeated.

Figure 3 shows the results of multiple runs of a twinkling pixel near room temperature. Each data point represents the difference between the actual output and the reset level of the pixel for that run. Figure 3 shows several interesting phenomenon. First, for most of the runs (70%), the dark signal accumulations are identical, reaching ~400 mV in 2 sec, corresponding to ~ 0.8 nA/cm^2 leakage current. Secondly, the dark signal evolution is decidedly non-linear in time. Thirdly, during several runs, the dark current accumulation exhibits a completely different temporal dependence. In some cases, it starts off at a high rate, and slows down towards the end of the cycle, and at other times, it makes abrupt transitions in the middle of a cycle.

This seemingly strange voltage change at the sense node makes more sense once we take the derivative of the voltage with time. This yields the sense node leakage current (with appropriate conversion factors applied). Figure 3 shows the extracted leakage current plotted against the sense node differential voltage (0V on the x-axis is equivalent to the diode reset potential of ~1.5V). The resultant graph shows the reverse-bias leakage characteristics of a diode, whose leakage is, on one hand, voltage dependent, and on the other hand, exhibits two distinct states – a low and a high current, with random transitions between one to the other. Modulation of the leakage current due to random transitions manifests as twinkling. About 6% of the pixels were found to exhibit the twinkling behavior.

The high-state leakage current can be modeled as trap-assisted-tunneling (TAT), with the tunneling field being

proportional to the voltage difference between the potentials at the off-state reset gate (V_L) and the sense node (V_S). The extracted dark current fits the model [11]:

$$I_d = I_{fixed} + \alpha \cdot \exp\left[\frac{V_{RST} - V_S - V_L}{V_x}\right]^2$$

where I_{fixed} is the fixed current, α is the proportionality constant, V_{RST} is the reset voltage on the diode, V_L is the reset gate voltage, and V_x is the field-threshold voltage. At low V_S (small back-bias), the dark signal is small and linear, since the field-effect is minimal. But, as V_S increases (the sense node potential is closer to the reset potential), the leakage current increases significantly, and exhibits much larger dependence on the field.

Figure 4 shows the measured dark current (low state) for different bias conditions of the source-follower and sampling times (sampling period is fixed). No difference was found with the variation of sampling times, whereas the difference between the two curves corresponding to two different source-follower bias currents is entirely due to source-follower gain variation. In either case, figure 4 indicates that the source-follower operating conditions have no effect on the sense node leakage, ruling out hot-electron related effects.

The random change in dark current from one state to another can be postulated to be a result of an oxide trap changing its state. When the trap is filled, the net electric field seen by the sense node is smaller, and the dark current is lower. The generation mechanism is more of thermal origin. Conversely, when the trap is empty, the electric field is high, and the dark current is high and is due to trap-assisted-tunneling. Further evidence of this phenomenology comes from the fact that the activation energies of the high and low dark currents are widely different: near mid-gap (0.51 eV) for the low current state, and much lower (0.3 eV) and therefore more field-dependent for the high current state. Since the dark current in the high state depends not on the absolute value of V_s or V_L but on the difference between the two, it is likely that these traps are located in the LDD region of the reset FET, and not at the channel.

The rate of twinkling is also temperature dependent, the transitions slowing down as the temperature is reduced. Figure 5 shows the Arrhenius plot of the capture and emission rates of the bimodal sense node dark current. Data indicates the emission and capture are governed a thermal process with the activation energies being 0.12 eV and 0.39 eV respectively.

The number of twinkling pixels as well as the level of twinkling was reduced by reducing the electric field in the LDD region. With the reduced electric field, the trap state had little effect on the electric field seen by the sense node, resulting in suppression of dark current generation by trap-assisted tunneling, and hence suppression of large changes in dark current. The number of twinkling pixels reduced to less than 0.007% following electric field optimization.

Acknowledgments:

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References:

1. K. Yamaguchi et al., *IEEE Trans. Electron Devices,* vol. 46, pp. 1159-1165, 1999.
2. H. Kwon et al., *IEEE Trans. Electron Devices*, vol. 51, pp. 178-184, 2004.
3. B. Pain et al., *Proc. Workshop on CCD/AIS,*2005.
4. K.M. Findlater et al., *Proc. SPIE*, vol. 5251, pp 187-195, 2004.
5. C. Leyris et al., *Proc. SPIE*, vol. 5844, pp 41-51, 2005.
6. J. Janesick et al, *Proc. SPIE*, vol. 6276, pp. 99-108, 2006.
7. G.V. Groeseneken et al., *IEEE Trans. Electron Devices,* vol. 43, pp. 940-948, 1996.
8. E. Simoen et al, *IEEE Trans. Electron Devices,* vol. 39, pp. 422-429, 1992.
9. Y. Shi et al., *Semicond. Sci. Technol.*, vol 16, pp 21–25, 2001.
10. X. Wang et al., *Tech. Digest Intl. Electron Dev. Meeting*, 2006.
11. G.A.M. Hurkx et al., *IEEE Trans. on Electron Devices*, vol. 39, pp. 331-338, 1992.

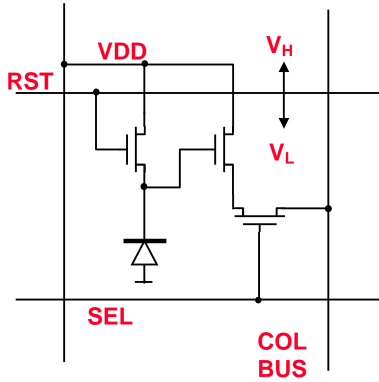

Figure 1a: Pixel schematic

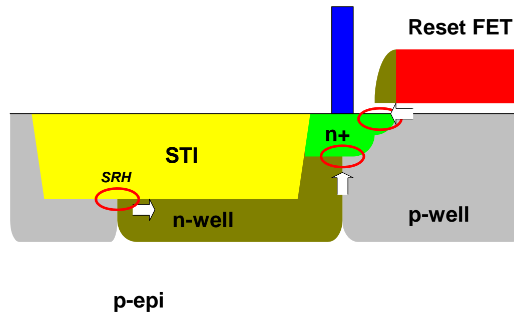

Figure 1b: Schematic cross-section

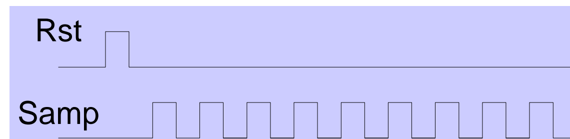

Figure 2: Timing diagram used for data collection

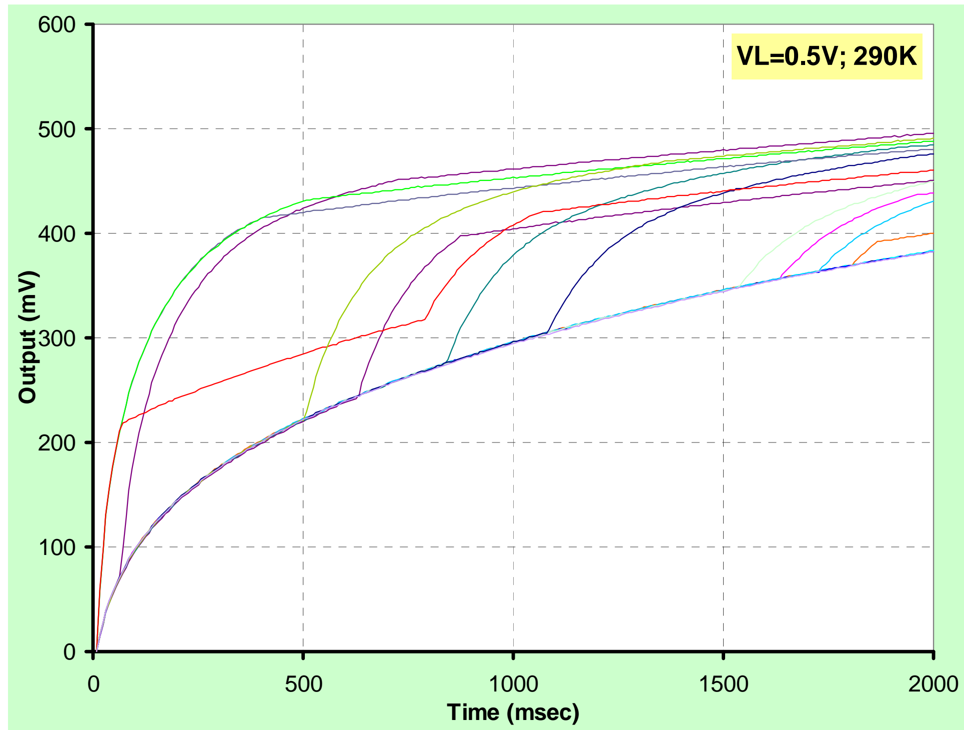

Figure 3: Measured data for two different source followe bias currents

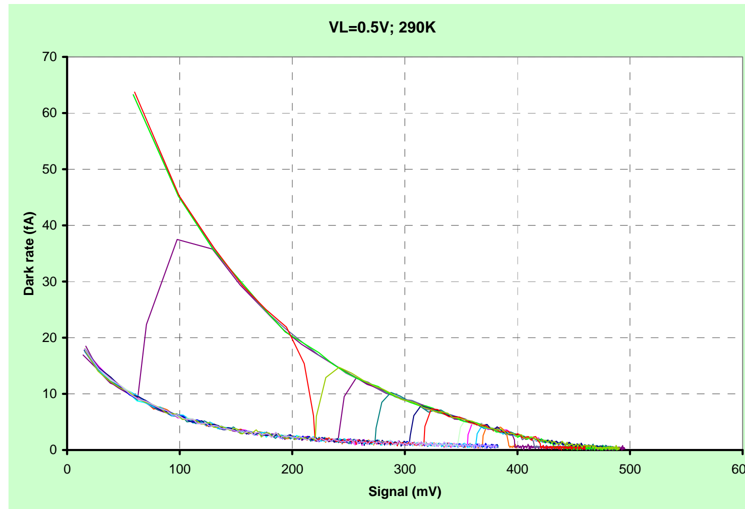

Figure 3: Measured data for two different source followe bias currents

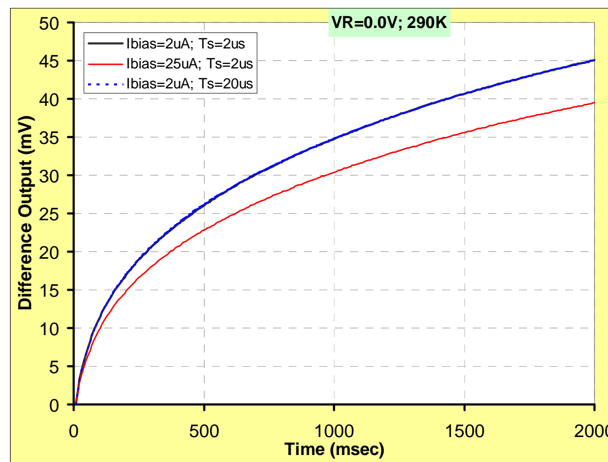

Figure 4: Measured data for different source-follower operating conditions

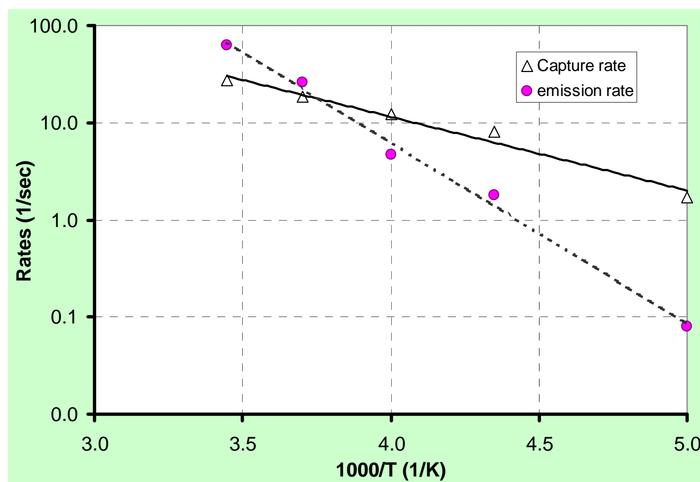

Figure 5: Arhennius plot of capture and emission rates

Evaluation of a Small Negative Transfer Gate Bias on the Performance of 4T CMOS Image Sensor Pixels.

Hyungjun Han, Hongjoo Park, Parker Altice, Woonil Choi, Younsub Lim, Sangjoo Lee, Seok Kang, Jaeyeong.kim, Kwangho Yoon and Jerry Hynecek
MagnaChip Semiconductor Ltd. Hyangjeong-dong, Heungdeok-gu, Cheongju-si, Chungcheongbuk-do, 361-725 Korea; E-mail: hyungjun.han@magnachip.com

I. Introduction.

From the early development of Virtual Phase CCD Image sensors it became well known that the negative bias applied to the CCD gates results in accumulation of holes at the interface [1, 2]. This leads to quenching of the interface states at the Si-SiO_2 interface under the poly-silicon gates and a significant reduction of dark current. In modern 4T CMOS image sensors the similar effect is typically accomplished by placing a suitable p-type doping implant under the transfer gate of the pixel. However, due to very thin gate oxides, which are typically used in today's CMOS image sensors; it is not possible to completely saturate the interface states with holes by using only the implants, since undesirable problems such as the large threshold voltage shift result. For this reason other methods have been developed and are typically used. This paper presents evaluation of application of a small negative bias to the transfer gate of a high performance CMOS image sensor pixel as one possible solution to the problem. The small negative gate bias is easily generated on chip without any difficulty by using simple negative charge pump circuits. A suggested circuit block diagram for the generation of the suitable negative bias on-chip is also shown for completeness. This paper presents data of the negative charge pump effects on the dark current, dynamic range and blooming characteristics. The tested 2 Megapixel imager has 2.2um x 2.2um 2T pixels and operates with 2.8V analog drain bias as is typical in mobile applications. The negative charge pump circuit can provide bias from 0.0V to -0.5V.

II. Motivation for using the negative charge pump.

During formation of pinned photo diode to minimize the dark current, a suitable p-type doping implant is also used under the gate of the charge transfer transistor in order to fill the interface states with holes in this region. The interface potential should be kept close to 0V. However due to the N+ doped poly-silicon gate typically used for this transistor a build in potential difference of approximately Ec – Ev is applied through a very thin gate oxide to this region. As a result a small potential bending occurs at the silicon surface, leading to the depopulation of the interface states of holes and generation of the dark current. Fig.1.0 shows the drawing of the approximate potential profile under the gate. To achieve a flat band condition and repopulation of the interface states by holes and consequently the dark current reduction a negative charge pump is used to apply a small negative bias to the gate.

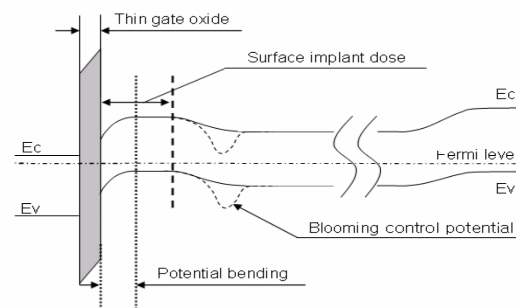

Fig.1.0. Energy band diagram under the charge transfer transistor.

In the CMOS image sensor it is also necessary to take care of the charge overflow to neighboring pixels called blooming. To prevent the blooming effects several approaches are usually used one of them being, for example, a blooming control implant. A dotted line

in Fig.1.0 indicates the energy band diagram where the implant was used. When the negative charge pump is turned on, the potential profile shouldn't significantly change in order to maintain a good blooming control. For a better understanding of the device structure Fig.1.1 shows the drawing of the device cross section under the transfer gate region.

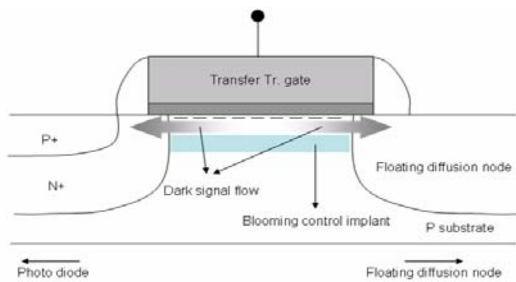

Fig.1.1. Cross section of the transfer gate region showing the interface states generated dark current flow and the blooming control implant location.

A portion of the interface states generated dark current flows into the floating diffusion and remainder flows into the photo diode. When the charge transfer transistor is turned off and a negative bias is applied to the gate holes are accumulated at the interface. This results in a significant reduction of dark current generation. Fig.1.2 shows the block diagram of the on chip negative charge pump circuit.

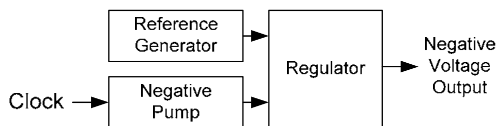

Fig.1.2. Block diagram of on chip negative charge pump circuit.

The circuit consists of the reference generator, negative bias charge pumping circuit and a regulator. The output is used as a ground level Vss-bias of the transfer gate driver-buffer. The resulting low level voltage applied to the gate of the transfer transistor thus becomes negative. The negative voltage range, which the circuit can generate, is from 0V to -0.5V with 0.05V steps.

III. Measurements and results.

Fig.1.3 shows the dark current measurement results. The dark current decreases with the negative charge pump bias. When the bias of -0.5V was applied to the gate, the dark current decreases as much as 37% in comparison to the 0V bias. However at the -0.05V bias a small increase has been noticed, which is not fully understood at this time and is currently being investigated.

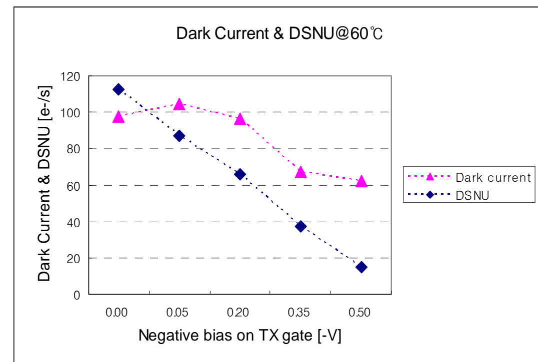

Fig.1.3. Dark current trend as function of the negative charge pump voltage.

Fig.1.4 shows the graph of the dynamic range as function of the negative charge pump bias.

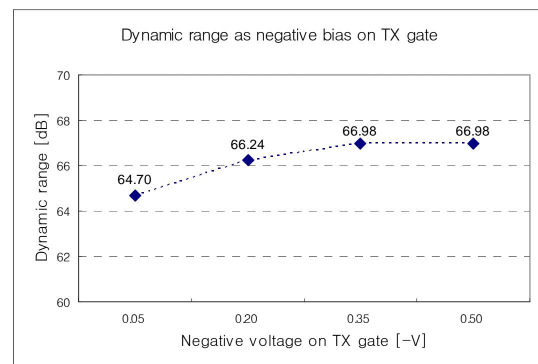

Fig.1.4. Dynamic Range as function of the negative charge pump voltage.

Since the blooming potential level can be affected by the negative gate bias it is necessary to confirm the

blooming performance of the pixel. This is shown in the photographs in Fig.1.5.

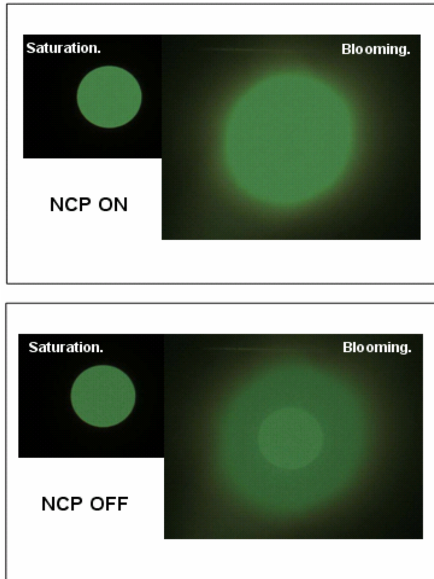

Fig.1.5. blooming image as function of the negative charge pump ON & OFF

An optical fiber was used as a light source for the generation of regular pattern and a module lens was used for the focused image. In case of the negative charge pump being turned off, the light pattern is noticed. The wider spot corresponds to bloomed area. When a lower light intensity is used no blooming pattern is found. With high intensity illumination the image intensity graph shown in Fig.1.6 is measured.

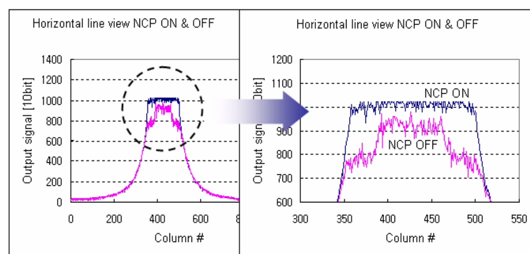

Fig 1.6. Blooming image horizontal view.

When a negative charge pump is turned off the pixel charge output is smaller than the full allowable analog swing voltage of the ADC converter. When the negative charge pump is turned on the blooming pattern could not be clearly recognized due the signal clipping by the ADC. However, when these two graphs are compared the over all shape of the graphs did not change only the output signal has increased. Fig.1.6 is showing the intensity graphs of the horizontal cross section of image in Fig.1.5. For the case of the negative charge pump turned off the signal is clipped off and only the blooming region remains. Concluding from the results shown in Fig.1.5 and Fig.1.6 it can be stated that the blooming control is working correctly. This means that the negative charge pump bias did not significantly affect the potential profile under the transfer gate.

IV. Conclusions

In this paper the effect of a small negative bias of the charge transfer gate on the CMOS sensor performance was evaluated. It was found that a small bias generated by the negative charge pump is useful for decreasing the dark current and increasing the sensor dynamic range. By using the negative charge pump, the blooming barrier was slightly lowered but the blooming characteristic was not significantly changed. The negative charge pump worked up to -0.5V and it showed approximately 37% decrease in dark signal and 0.24V increase of the saturation level.

Acknowledgements:

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References:

[1] A. J. Theuwissen, “The Hole Role in Solid-State Imagers,” IEEE Tr. Electron Devices, vol. ED-53, no. 12, pp. 2972-2979, December 2006.
[2] J. Hynecek, “Virtual Phase CCD Technology,” in IEDM Tech. Dig. 1979, pp. 611-614.

Some thoughts on Diffusion Dark Current

M.M. Blouke
Ball Aerospace & Technologies Corp.
Boulder, CO 80306

1. Introduction

Of the three components of the dark current seen in imagers, the diffusion component is the least understood.[1] This is principally due to the fact that it only makes its presence felt at elevated temperatures. The conventional expression for the diffusion component involves the minority carrier diffusion length which can be quite large and assumes that the substrate extends to infinity beneath the detector. In most sensors this is not the case. So the question is: What is the appropriate expression for the diffusion current given a finite region beneath the detecting element? This paper will derive expressions for the diffusion dark current for a front-illuminated device built on the standard epitaxial material on a low resistivity substrate [2,3] and a thinned, back-illuminated device. The solutions are applicable to both CCDs and CMOS devices.

2. Models

2.1 The front-illuminated device

Figure 1 presents the geometry for a front-illuminated device built on the industry standard p on p+, epitaxial material.[2,3] We take the edge of the depletion region to be the origin. The undepleted epitaxial material (characterized by the parameters diffusion coefficient for electrons, D_{epi}, minority carrier lifetime, τ_{epi}, mobility, μ_{epi} and doping concentration, N_{epi}) is of thickness σ. The substrate material is characterized by D_{sub}, τ_{sub}, μ_{sub}, and N_{sub} and extends to x = t. To find the diffusion current, we must solve the continuity equation in both regions [4,5,6]

$$\frac{\partial n(x)}{\partial t} = \nabla \bullet J_n + G(x) - R(x) = D\frac{\partial^2 \delta n(x)}{\partial x^2} - \frac{\delta n(x)}{\tau} = 0 \qquad (1)$$

The solutions are

$$\delta n_{epi} = A\exp(\gamma x) + B\exp(-\gamma x) \qquad 0 < x < \sigma \qquad \gamma = (D_{epi}\tau_{epi})^{-1/2}$$

and

$$\delta n_{sub}(x) = C\exp(\xi x) + D\exp(-\xi x) \qquad \sigma < x < t \qquad \xi = (D_{sub}\tau_{sub})^{-1/2}$$

Subject to the boundary conditions

1. $\delta n_{epi}(x=0) = -n_{eo} = -\dfrac{n_i^2}{N_{epi}}$ 2. $\delta n_{sub}(x=t) = 0$

and at the epitaxial interface,

3. $\delta n_{epi}(x=\sigma^-) = \dfrac{N_{sub}}{N_{epi}}\delta n_{sub}(x=\sigma^+)$ and 4. $J_{epi}(x=\sigma^-) = J_{sub}(x=\sigma^+)$

Condition 3 comes from the relationship across a hi-lo junction:

$$n_{eo} = N_{epi} = n_{sub}\exp(\frac{qV_{hilo}}{kT}) = N_{sub}\exp(\frac{qV_{hilo}}{kT})$$

Assuming the Fermi level doe not change significantly across the junction, boundary condition 3. results. [7]

After applying the boundary conditions and a little algebra, one arrives at the corrected expression for the front illuminated device:

$$J_{diff} = \frac{qD_{epi}n_i^2}{L_{epi}N_{epi}}\left(1 - \frac{\exp(\gamma\sigma)(K+1)}{(\cosh(\gamma\sigma) + K\sinh(\gamma\sigma))}\right) \tag{2}$$

K is a constant and is given by

$$K = \frac{L_{epi}N_{epi}D_{sub}}{L_{sub}N_{sub}D_{epi}} \tag{3}$$

One can easily convince oneself that as $\sigma \to \infty$, the correction term approaches -1 and the expression for the dark current approaches the classical value. However, as $\sigma \to 0$, the correction term reduces to the value -K. Consequently, the diffusion related dark current reduces to the value appropriate to the substrate material. Figure 2 represents theoretical calculations of J_{diff} based on the above equation using the parameters listed in the Figure. The figure shows that for practical values of the starting material, the diffusion related dark current is reduced below the classical value and is more characteristic of the substrate doping.

2.2 Model for a thinned device

The model for the thinned part is similar to the model for the quantum efficiency of a thinned CCD.[4,5] The thinned device can be modeled as a thinned silicon membrane of thickness t. In the neighborhood of the surface there exists a region of thickness $\Delta=(t-\sigma)$. An electric field exists and acts on carriers in this region; depending on the sign of the field, the carriers are either encouraged to move towards the CCD wells or they are driven towards the back surface where they recombine. The back surface is characterized by a surface recombination velocity.[4-7]

Again the continuity equation must be solved for the two regions: i) the field free region between the depletion edge ($x = 0$) and the edge of the surface region ($x = \sigma$) and ii) the surface region itself. In this case the equation to be solved is

$$D_e \frac{\partial^2 \delta n(x)}{\partial x^2} + \mu_e E_o n(x) - \frac{\delta n(x)}{\tau} = 0 \tag{3}$$

where E_o is zero in the field free region and has some value in the surface region. The solutions for the two regions are:

$$\delta n_1(x) = A\exp(\gamma x) + B\exp(\gamma x) \qquad 0 < x < \sigma \qquad \gamma = (D_e\tau)^{-1/2}$$

and

$$\delta n_2(x) = c\exp(\lambda x) + D\exp(\nu x) \qquad \sigma < x < t \qquad \lambda, \nu = -\left(\frac{\mu_e E_o}{2D_e}\right) \pm \sqrt{\left(\frac{\mu_e E_o}{2D_e}\right)^2 + \gamma^2}$$

The boundary conditions are:

1. $\delta n_1(x=0) = -n_{eo} = -\dfrac{n_i^2}{N_e}$ 2. $J_2(x=t) = -so\,\delta n_2(t)$

3. $\delta n_1(x=\sigma^-) = \delta n_2(x=\sigma^+)$ 4. $J_1(x=\sigma^-) = J_2(x=\sigma^+)$

Applying the boundary conditions and, as before, solving for the diffusion current into the depletion region gives

$$J_{diff} = \frac{qD_e n_i^2}{L_e N_e}\left(1 + \frac{\exp(\gamma\sigma)(\omega - 1) + \frac{\phi}{\gamma}\left(\frac{\lambda + \phi - \omega\gamma}{\lambda + \psi}\exp(-\lambda\Delta) - 1\right)}{\cosh(\gamma\sigma) - \omega\sinh(\gamma\sigma)}\right) \tag{4}$$

where $\phi = \frac{\mu_e E_o}{D_e}$ $\psi = \left(\frac{s_o + \mu_e E_o}{D_e}\right)$ $\Delta = t - \sigma$

and

$$\omega = \frac{(\nu + \psi)\nu\exp(-\lambda\Delta) - (\lambda + \psi)\lambda\exp(-\nu\Delta)}{\gamma((\lambda + \psi)\exp(-\nu\Delta) - (\nu + \psi)\exp(-\lambda\Delta))} \tag{5}$$

Again, as $\sigma \rightarrow \infty$, the expression for the dark current reduces to the conventional form as it should.

Figures 3-5 present theoretical calculations of the behavior of the diffusion dark current based on the current model. Figure 3 shows the dependence of the minority carrier concentration on the electric field in the surface region. Note that neither the direction nor the strength of the field have a significant effect on the minority carrier concentration. Only for fields in excess of -2000 V/cm does the field have a significant effect on the electron concentration. This observation is consistent with the previously developed model for the quantum efficiency of a thinned device which showed that fields of the order 3-6 kV/cm are required to achieve significant QE at short wavelengths. [4, 5] Figure 4 presents calculations based on the above model of the normalized diffusion related dark current as a function of thickness of the device. What the figure demonstrates is that given enough Silicon, the diffusion related dark current will eventually equal the canonical value.

Finally, Figure 5 presents the normalized diffusion dark current as a function of the field in the surface region. Oddly, thinned devices with poor short wavelength QE will tend to have the lowest diffusion related dark current.

References

1. C.K. Kim, “The Physics of Charge-coupled Devices” in *Charge-coupled Devices and Systems*, Ed M.J. Howes and D.V. Morgan (Wiley; New York: 1979)
2. J.R. Janesick, *Scientific Charge-coupled Devices* (SPIE, Bellingham; 2001)
3. A.J.P. Theuwissen, *Solid State Imaging with Charge-coupled Devices* (Klewer Academic Publishers:Delft:1995)
4. M.M. Blouke, “Model of a thinned CCD,” Proc. SPIE, 1439, pp136-143 (1990).
5. M.M. Blouke, W.A. Delamere and G. Womack, "A simplified model of the back surface of a charge-coupled device," Proc. SPIE 1447, 142-155 (1991).
6. A.S. Grove, *Physics and Technology of Semiconductor Devices* (Wiley, New York: 1967).
7. C.G. Fonstad, *Microelectronic Devices and Circuits* (McGraw-Hill, New York, 1994)
8. J.R. Hauser and P.M. Dunbar, ”Minority carrier reflecting properties of semiconductor high-low junctions,” Solid State Electron., **18**, 715-716 (1975).

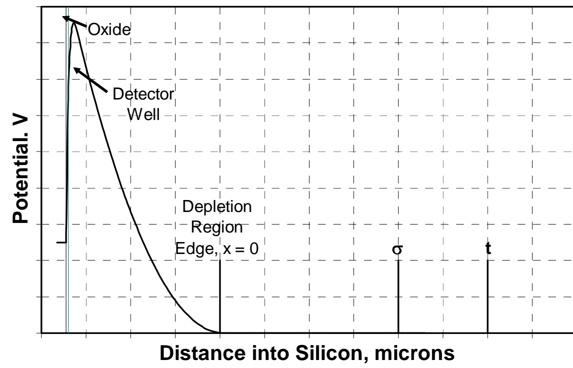

Figure 1. This figure shows schematically the geometry of the configuration. $x = 0$ is at the edge of the depletion region, σ is the location of the hi-lo junction in the case of the front illuminated device and is the location of the front edge of the surface region in the thinned case. t is the location of the back surface of the device.

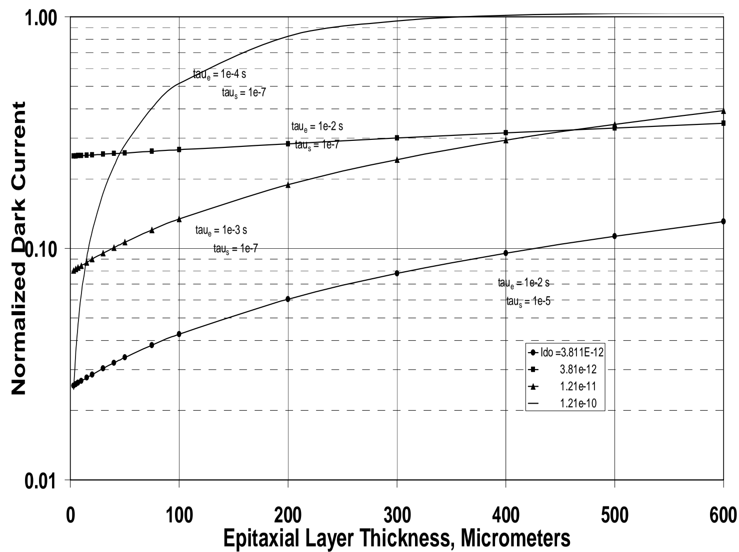

Figure 2. Diffusion dark current as a function of the field free region beneath the pixel.

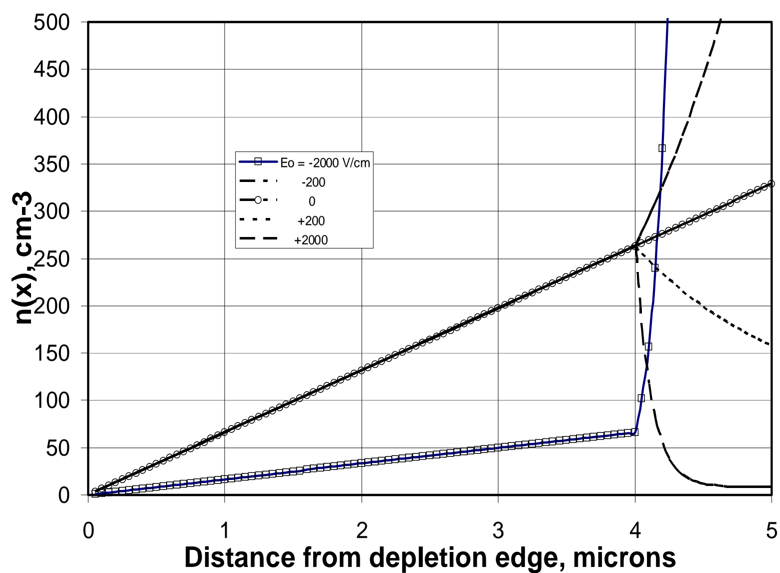

Figure 3. Minority carrier concentration vs distance with the surface field as the parameter.

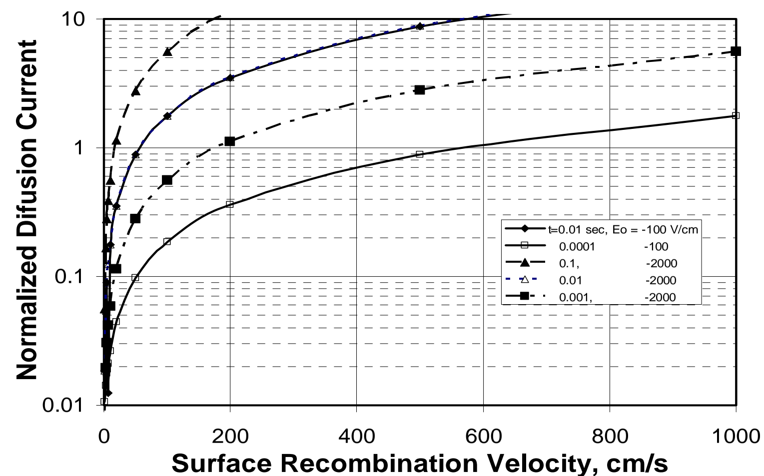

Figure 4. Normalized dark current vs. recombination velocity.

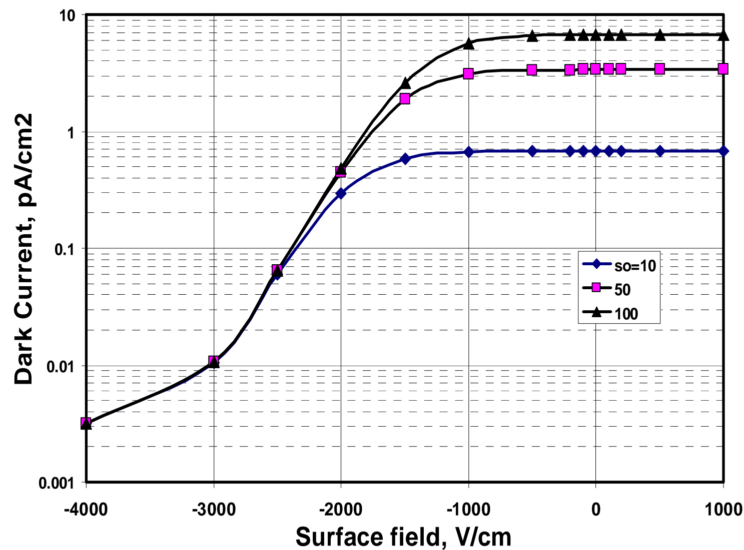

Figure 5. Diffusion related dark current as a function of the surface field with the surface recombination velocity.

Will Avalanche Photodiode Arrays Ever Reach 1 Megapixel?

Edoardo Charbon
Swiss Federal Institute of Technology, CH-1015 Lausanne, Switzerland

Abstract— In this paper the miniaturization and performance potential of solid-state avalanche photodiodes is discussed in the context of large multi-pixel sensors. Technological and design trade-offs are discussed in view of recent advances in CMOS imaging technologies and the emergence of new multiplication based architectures.

I. INTRODUCTION

In the last four decades, solid-state multiplication based photodetectors have gradually evolved from relatively crude devices to the sophistication of today. Almost every imaging technology has one such device and the range of implementations is quite wide [1]. In this context, silicon avalanche photodiodes (APDs), thanks to their relative simplicity and ease of fabrication, have recently attracted significant interest.

There are two main lines of research in silicon APDs: one that advocates the use of highly optimized processes to boost performance and one that proposes to adapt APD design to existing processes to reduce cost and to maximize miniaturization.

In this paper we focus on the latter approach and we discuss how the latest advances in imaging CMOS processes may be used to maximize performance and to boost miniaturization. We also discuss how advanced processes can ensure in-pixel and on-chip processing of ultra-high-speed signals that are typical of single-photon detectors.

II. SINGLE-PHOTON DETECTION AND SILICON APDS

Devices for single-photon detection are realizable in many solid-state and non-solid-state implementations. While an in-depth discussion on the subject is beyond the scope of this paper, we mention here two classes of detectors that are currently the solution of choice in many applications: multichannel or microchannel plates (MCPs) and photomultiplier tubes (PMTs) [2].

A number of solid-state solutions have been proposed as a replacement of MCPs and PMTs using conventional imaging processes. The challenge though has been to meet single-photon sensitivity *and* low timing uncertainty.

To address the sensitivity problem, cooled and/or intensified CCDs, and ultra-low-noise CMOS APS architectures have been proposed. Multiplication of photogenerated charges by impact ionization has also been used in conventional CCDs [3].

Meeting PMT's picosecond timing uncertainty however, to the best of our knowledge, has not been possible in CCD/CMOS imagers, even though uncertainties as low as one microsecond in CCD [4] and a few nanoseconds in CMOS APS [5] have been demonstrated. While CCD streak cameras can achieve a resolution of a few picoseconds, they require a 2D pixel array to resolve a string of photon arrivals. Moreover, long acquisition latency and the added complexity to form and deflect the photoelectron beam make this device unsuitable for miniaturization and low-cost operation.

Sensors based on solid-state APDs have been proposed decades ago to simultaneously achieve high sensitivity and dynamic range, and low timing uncertainty [6]. In APDs, carriers generated by the absorption of a photon in the p-n junction, are multiplied by impact ionization thus producing an avalanche. APDs can reach timing uncertainties as low as a few tens of picoseconds, thanks to the speed at which an avalanche evolves from the initial carrier pair forming in the multiplication region.

An APD is implemented as photodiode reverse biased near or above breakdown, where it exhibits optical gains greater than one. When an APD is biased below breakdown it is known as *proportional or linear* APD. It can be used to detect clusters of photons and to determine their energy. When biased above breakdown, the optical gain becomes virtually infinite. Thus, with a relatively simple ancillary electronics, the APD becomes capable of detecting single photons. The APD operating in this regime, known as Geiger mode of operation, is called *single-photon avalanche diode* (SPAD).

III. APD DESIGN IN STANDARD CMOS PROCESSES

A. Basic Structure Design

There exist two main implementation styles for APDs. The first, known as reach-through APD (RAPD) [7], is a vertical structure, incompatible with planar CMOS processes. The second involves a shallow p or n layer to form high-voltage pn junctions. Cova and others have investigated devices designed in this style since the 1970s, yielding a number of structures equipped with a zone designed to prevent premature edge breakdown (PEB) [8]. An early example of one such structure is shown in Fig. 1.

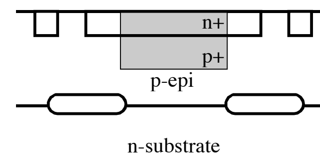

FIG. 1. CROSS-SECTION OF APDS THAT CAN BE FABRICATED IN A PLANAR PROCESS.

More recently, researchers have developed APDs both in linear and Geiger mode using dedicated processes, achieving superior performance in terms of sensitivity and noise. A good example is the work of Kindt [9]. The main disadvantage of using dedicated processes is the lack of libraries that can support complex functionalities and deep-submicron feature sizes, thus limiting array sizes. An interesting alternative is the use of a hybrid approach whereby the APD array and ancillary electronics are implemented in two different processes, each optimized for APD performance and speed, respectively [10].

In 2003 the integration of linear and Geiger mode APDs in a low-cost CMOS process has become feasible [11]. PEB prevention is accomplished forcing the electric field everywhere to be lower than that on the planar multiplication region, where it should be uniform.

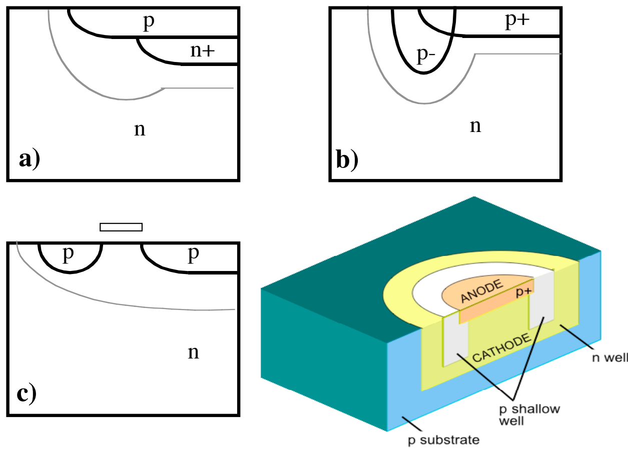

FIG. 2. TECHNIQUES FOR PREVENTION OF PREMATURE EDGE BREAKDOWN (PEB) IN PLANAR PROCESSES.

Fig. 2 shows some of the most used structures. In a) the n+ layer maximizes the electric field in the middle of the diode. In b) a lightly doped p- implant reduces the electric field at the edge of the p+ implant. In c) a floating p implant locally increases the breakdown voltage. With a polysilicon gate one can further extend the depletion region (gray line in the figure). The figure also shows a 3D cross-section of b) including a p-substrate and an n-well isolation.

Modern imaging processes (with or without STI) provide several lightly doped implants at three or more depths. Thus, an optimal layer combination (p+/p-/n-well) generally exists that can yield a good trade-off between timing uncertainty and noise. However, care should be used so as to avoid full depletion of the well and punch-through's between shallow tubs and substrate. Buried layers should also be used with care to prevent punch-through across the n-well.

B. Quenching and Recharge Mechanisms

Linear APDs are multi-photon detectors, when used as charge accumulators. Charges generated at each avalanche are integrated and amplification may not be needed. In single-photon detection mode, fast amplifiers are generally used, adding to jitter and dark noise. SPADs on the contrary can only operate in single-photon mode. This is achieved operating the diode above breakdown by a voltage known as *excess bias voltage*. Upon photon absorption, an avalanche may be triggered involving a sufficient number of charges to be easily detected and thus requiring no further amplification.

SPADs however require mechanisms to quench the avalanche. There exist two main quenching mechanisms: passive and active. In passive quenching the avalanche current is used to drop the voltage across the diode. This is generally accomplished via a ballast resistor placed on the anode or the cathode of the diode, as shown in Fig. 3. Avalanche detection is accomplished measuring the voltage across the ballast resistance (Fig. 3a, b) or the current across a low- or zero-resistivity path (Fig. 3c, d). Pulse shaping may be performed using a comparator (Fig. 3e).

Excess bias voltage equals $|V_{OP}| - |V_{bd}|$, where V_{bd} is the breakdown. The resistances may be implemented in polysilicon [11],[12] or exploiting the non-linear characteristics of PMOS or NMOS devices [13],[14].

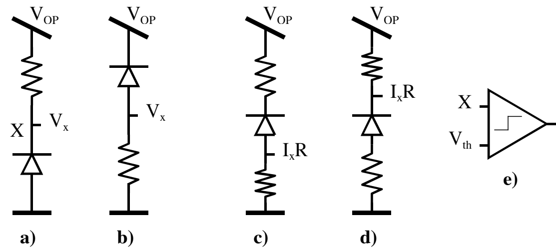

FIG. 3. PASSIVE QUENCHING VARIANTS. VOLTAGE DETECTION MODE (LEFT); CURRENT DETECTION MODE (RIGHT).

In active quenching mode, the avalanche activates an active device to stop it. The literature on the subject is extensive. In [15] some of the existing schemes can be found. Other authors have recently revisited the issue [16].

After quenching, the device enters another phase known as recharge. During this phase the photodiode bias voltage must return to the pre-avalanche state as quickly as possible. Again, there are passive and active schemes to achieve recharge. The simplest approach is shown in Fig. 3. The diode will automatically recharge to V_{OP} via the ballast resistance. The recharge, in this case, follows the RC exponential, where R is the equivalent quenching resistance and C the total parasitic capacitance at node X.

In active recharge schemes, the photodiode is forced to the initial state generally via a fast switch controlled by a current sense amplifier. Even though these schemes are attractive, they usually require extra complexity to a pixel, thus potentially hindering miniaturization.

The quenching and recharge times are collectively known as *dead time*. Dead time in passive quenching/recharge methods is potentially longer than in their active counterparts. However, the advantage of a reduced dead time in large array may be preempted by limited speeds of pixel readout schemes.

C. The Importance of Miniaturization

The first SPAD implementations in 0.35μm CMOS technology have demonstrated fully scalable pixels at a pitch of 25μm. However, for a realistic Mpixel sensor realization, this limit should be further reduced.

Pixel miniaturization has other benefits too. The reduction of anode and cathode areas, in SPADs generally reduces the *dark count rate* (DCR), i.e. the average frequency of spurious pulses in the dark [11]. It also reduces parasitic capacitance at node X (Fig. 3), thus possibly reducing dead time. In addition, the number of carriers involved in an avalanche is also reduced, thus

decreasing the probability of carrier trapping and, consequently, of afterpulsing. Finally, fewer carriers involved in impact ionization will cause smaller photon emission, hence causing less interference with other pixels.

IV. Achieving Miniaturization

A. Pixel Miniaturization

The first ingredient towards pixel miniaturization in a given process is the simplest possible avalanche detection mechanism. One possible solution consists of shifting V_{OP} to VDD, and ground to a negative voltage V_P^+. Hence, node X (Fig. 3) can be made vary between VDD and ground, thereby enabling the replacement of a relatively large comparator by a simple properly designed inverter [11], [12]. Fig. 4 shows an example of one such detector.

The second ingredient is the reduction of feature size through processes that represent a good compromise between available layers, doping profiles, and design rules. Particularly important factors are the well-to-well minimum distance, the doping levels in the multiplication regions, and the level of defects in the lattice.

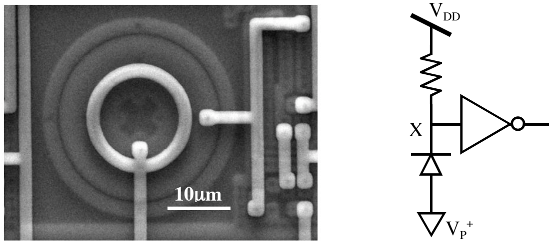

Fig. 4. Photomicrograph of a SPAD implemented in CMOS technology. A guard ring surrounds the anode for PEB prevention.

The third ingredient is the readout scheme. In general, simpler pixel-level processing enables smaller sizes but it may have an impact on performance. Alternatively, more pixel parallelism may impact pitch.

B. Pixel Sharing

Due to the need for independent quenching and recharge in a SPAD array, the level of sharing cannot be pushed unless one accepts time-sharing as well. This scheme however may not be appropriate for photon-starved applications. For low photon-count, time-resolved applications it is possible for an entire pixel array or column to share high-resolution time discriminators at a cost of a higher sensor complexity.

C. Readout Techniques

APDs can potentially be read out using a conventional scheme similar to CMOS APS architectures. SPADs on the contrary, generate a digital pulse for each detected photon. To avoid missing photon counts, a pixel-level counter or time discriminator can be used [17],[18]. However, large counters are not desirable due to the fill factor loss and/or extra time required to perform a complete readout. A partial solution to this problem is the reduction of the counter resolution (ultimately 1 bit), requiring more frequent readouts and/or lower saturation. Another solution is to access every pixel independently but sequentially using a digital random access scheme [12],[13].

In low-light-level (LLL) applications, an alternative approach may be used known as *event-driven* readout [19],[20]. In this readout scheme, the column is organized as a digital bus. When a photon is detected, the corresponding pixel takes ownership of the bus, sending timing related information as well as the ID of the pixel generating such information to the exterior of the array.

An alternative approach for non-LLL situations is the use of a *latchless pipeline* scheme. In this approach, the absorption of a photon causes the SPAD to inject a digital signal onto a delay line that acts as an ultra-fast conveyor belt [21]. This method allows detection of photons simultaneously on a column even though some restrictions apply on the timing of the optical setup. Fig. 5 shows the photomicrograph of chip implementing this readout style.

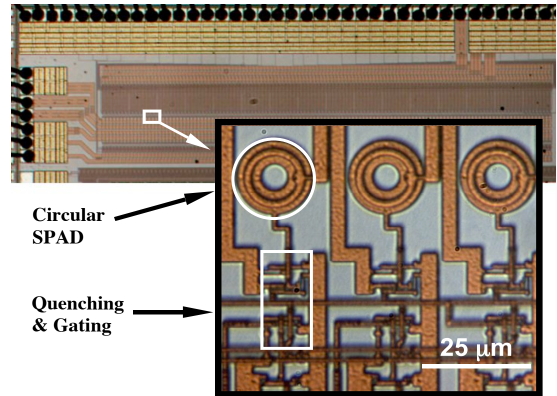

Fig. 5. Photomicrograph of a single-photon Detector with latchless pipeline readout.

V. Performance Issues in Large APD Arrays

CMOS APDs are characterized by means of the same parameters of conventional photodiodes, except for an optical gain higher than one. APDs operating in Geiger mode on the contrary require a specific set of parameters.

A. Fill Factor

Due to the geometry of guard rings for PEB prevention, in SPADs the fill factor may be as low as 1%. Using modern readout techniques, fill factors of up to about 9% have been demonstrated [21]. We have also demonstrated a fill factor reclaim ratio of 15 using commercial microlense arrays [22].

B. Dead Time

In passive quenching/recharge devices dead time is generally dominated by the recharge time, about 30-50ns, and it varies a few percentage points across the array as a function of temperature and process variability. This results in mild saturation non-uniformity and time variability.

C. Time Uncertainty or Jitter

In integrated SPADs jitter is limited from below by geometry and process technology considerations. In arrays of significant size, jitter generally degrades from 50ps to as much as several hundreds of picoseconds due to electrical path and electrical supply ripple. Techniques derived from memory design, such as non rail-to-rail readout and shielding should be exploited.

D. Photon Detection Probability (PDP)

The sensitivity is characterized in SPADs by the photon detection probability (PDP) and it is the overall probability that an impinging photon triggers a digital pulse. Detailed physical models for PDP and its mechanisms can be found

in [11]. PDP is dependent on temperature and excess bias voltage. A good pixel-to-pixel uniformity is generally observed. Based on on-going research, we expect that deep-submicron SPADs achieve up to 40-50% PDP. In more advanced deep-submicron processes, the multiplication region will move to the surface and will be thinner. Thus, sensitivity in shorter wavelengths will be reinforced. Fig. 6 plots PDP as a function of wavelength for two CMOS technologies. In the inset PDP uniformity is shown [14].

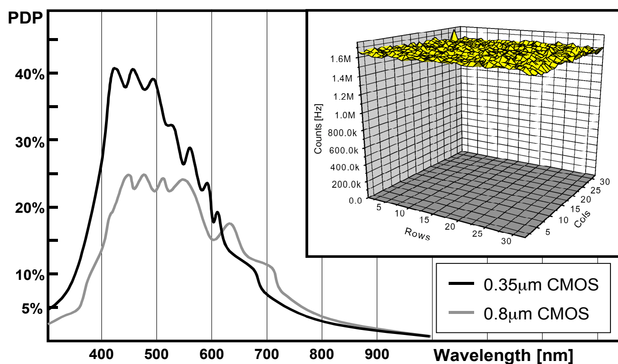

FIG. 6. PHOTON DETECTION PROBABILITY (PDP) AS A FUNCTION OF IMPINGING RADIATION WAVELENGTH.

E. Dark Count Rate

As mentioned earlier, DCR is a function of detector area. It is also a function of temperature and excess bias voltage. On a large chip, DCR may vary widely from a minimum of a few Hertz to a few kilohertz. Generally, noisy pixels are less than 1% of the array, depending upon the distribution of traps across the chip and the overall quality of the process. Hence, it is always a good practice to foresee means to shut off pixels either temporarily or permanently, depending on applications.

F. Afterpulsing

Afterpulses are the result of secondary avalanches related to earlier photon detections. The mechanisms behind afterpulsing are well understood and the literature on the subject is extensive [11]. In active recharge schemes, a minimum recharge time needs to be allocated to allow for single-photon detectors to recover from an avalanche, thus keeping afterpulsing probability below a threshold. Fewer impact ionizations and fewer traps can reduce this time.

G. Crosstalk

Crosstalk can be optical and electrical. In optical crosstalk, luminescence released by an avalanche elsewhere may cause avalanches. In electrical crosstalk, a carrier generated elsewhere may trigger avalanches. The techniques for preempting optical crosstalk include optical shields between pixels [6]. Electrical crosstalk is strongly reduced insulating the multiplication region, for example, with a well (Fig. 2). The drawback of this approach is the reduction of fill factor and/or the increase of overall pitch.

VI. CONCLUSIONS AND ACKNOWLEDGMENTS

In the near future optical sensors might look increasingly like memories; pixels like single-photon detectors, thus generating increasing interest in linear and Geiger-mode APDs [23]. Yet, despite recent advances, integrated APD technology still lags behind CCD and CMOS APS. This paper addresses those issues and technological solutions for high-density APD arrays.

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REFERENCES

[1] E. Charbon, “Will CMOS Imagers Ever Need Ultra-High Speed?”, *IEEE International Conference on Solid-State and IC Technology*, Vol. 3, pp. 1975-1980, Oct. 2004.

[2] J. McPhate, J. Vallerga, A. Tremsin, O. Siegmund, B. Mikulec, A. Clark, “Noiseless Kilohertz-frame-rate Imaging Detector based on Microchannel Plates Readout with Medipix2 CMOS Pixel Chip”, *Proc. SPIE*, Vol. 5881, pp. 88-97, 2004.

[3] J. Hynecek, “Impactron – A New Solid State Image Intensifier”, IEEE Trans. on Electron Devices, Vol. 48, N. 10, pp. 2238-2241, Oct. 2001.

[4] T. G. Etoh *et al.,* An Image Sensor Which Captures 100 Consecutive Frames at 1,000,000 Frames/s, *IEEE Trans. on Electron Devices*, Vol. 50, N. 1, pp. 144-151, Jan. 2003.

[5] G. Patounakis, K. Shepard, and R. Levicky, “Active CMOS Biochip for Time-Resolved Fluorescence Detection“, IEEE Symposium on VLSI, pp. 68-71, June 2005.

[6] R.H. Haitz, “Studies on Optical Coupling between Silicon p-n Junctions”, *Solid-State Electronics*, Vol. 8, pp. 417-425, 1965.

[7] R.J. McIntyre, “Recent Developments in Silicon Avalanche Photodiodes”, *Measurement*, Vol. 3 N.4, pp. 146-152, 1985.

[8] S. Cova, A. Longoni, and A. Andreoni, “Towards Picosecond Resolution with Single-Photon Avalanche Diodes”, *Rev. Sci. Instr.,* Vol. 52, N. 3, pp. 408-412, 1981.

[9] W.J. Kindt, “Geiger Mode Avalanche Photodiode Arrays for Spatially Resolved Single Photon Counting”, Ph.D. Thesis, Delft University Press, ISBN 90-407-1845-8, 1999.

[10] B. Aull *et al.*, “Geiger-Mode Avalanche Photodiodes for Three-Dimensional Imaging”, *Lincoln Laboratory Journal*, Vol. 13, N. 2, pp. 335-50, 2002.

[11] A. Rochas, “Single Photon Avalanche Diodes in CMOS Technology”, Ph.D. Thesis, Lausanne, 2003.

[12] C. Niclass, A. Rochas, P.A. Besse, and E. Charbon, “A CMOS Single Photon Avalanche Diode Array for 3D Imaging”, *IEEE ISSCC*, pp. 120-121, Feb. 2004.

[13] C. Niclass and E. Charbon, “A Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging”, *IEEE ISSCC*, pp. 364-365, Feb. 2005.

[14] C. Niclass A. Rochas, P.A. Besse, and E. Charbon, “Design and Characterization of a CMOS 3-D Image Sensor Based on Single Photon Avalanche Diodes”, *IEEE JSSC*, Vol. 40, N. 9, Sep. 2005.

[15] S. Cova, M. Ghioni, A. Lacaita, C. Samori, F. Zappa, “Avalanche Photodiodes Quenching Circuits for Single-Photon Detection”, *Applied Optics*, Vol. 35, N. 12, pp. 1956-1976, 1996.

[16] J. Richardson, R. Henderson, and D. Renshaw, “Dynamic Quenching for Single Photon Avalanche Diode Arrays”, to appear, *Intl. Imaging Sensor Workshop*, June 2007.

[17] E. Charbon, “Techniques for CMOS Single Photon Imaging and Processing”, *IEEE ASICON*, Oct. 2005.

[18] D. Stoppa *et al.*, “A CMOS 3-D Imager based on Single Photon Avalanche Diode”, to appear, *Trans. Circuits and Systems I*, 2007.

[19] C. Niclass, M. Sergio, E. Charbon, “A Single Photon Avalanche Diode Array Fabricated in Deep-Submicron CMOS Technology”, *Design Automation & Test in Europe* (DATE), Mar. 2006.

[20] C. Niclass, M. Sergio, E. Charbon, “A 64x48 Single Photon Avalanche Diode Array with Event-Driven Readout”, *European Solid-State Circuits Conference* (ESSCIRC), Sep. 2006.

[21] M. Sergio, C. Niclass, E. Charbon, “A 128x2 CMOS Single Photon Streak Camera with Time-Preserving Latchless Pipeline Readout”, *IEEE ISSCC*, pp. 120-121, Feb. 2007.

[22] Süss MicroOptics, http://www.suss-microoptics.com

[23] E. Fossum, “What To Do With Sub-Diffraction-Limit (SDL) Pixels? A Proposal for a Gigapixel Digital Film Sensor (DFS)”, *IEEE Workshop on CCDs and Advanced Image Sensors*, pp. 214-217, June 2005.

A CMOS Single-Photon Avalanche Diode Sensor for Fluorescence Lifetime Imaging

Fausto Borghetti, Daniel Mosconi, Lucio Pancheri, David Stoppa
FBK-irst, Centre for Scientific and Technological Research
Via Sommarive 18, I-38050, Trento, Italy
Phone: +39 0461-314531, Fax: +39 0461-314591
Email: {borghetti, mosconi, pancheri, stoppa}@itc.it

***Abstract* — This contribute describes the design and preliminary characterization of a 16x16-pixel array based on Single Photon Avalanche Diodes (SPADs), fabricated in a standard high-voltage 0.35μm CMOS technology, and aimed at the analysis of fluorescence phenomena. Each pixel integrates a SPAD combined with an active quenching circuit and a voltage comparator for the digital conversion of the avalanche event. The sensor features a minimum detectable photon density of 10^8 photons/cm^{2}s, with a maximum dynamic range of over 120dB. Detection of fluorescence light has been demonstrated with a 160ps time resolution over a 100ns observation window.**

I. INTRODUCTION

We have assisted, recently, to a growing interest in fast, portable and low-cost biological test equipment. However, existing systems are aimed at research applications mainly, featuring excellent performance but not suitable to be used in handling, self-test diagnostics. Among the many methods used for biological testing, optical detection is the most common. In particular, fluorescence lifetime imaging is an investigation tool of paramount importance in molecular biology and medicine, allowing the mapping of many cell parameters and the detection of pathologies or DNA sequencing [1]. A typical fluorescence lifetime experiment [2] uses a pulsed or modulated laser to excite the fluorescent markers (fluorophores) and the emitted light is revealed by means of intensified CCD cameras or photomultipler tubes [3] in order to achieve the required time-resolution and light sensitivity. The performance of these laboratory instruments is excellent but they are expensive and bulky. On the contrary, high accuracy time resolution can be achieved exploiting SPADs. The feasibility of SPADs in conventional CMOS technology, as recently demonstrated [4]-[10], opens the way to the realization of low-cost and high-performance fully integrated systems for high sensitivity imaging.

In this paper we propose the integration, at the pixel level, of a SPAD, an active quenching circuit and a voltage comparator for the digital conversion of the detected photon. The pixel array can be addressed using different operation modes which allow using of the sensor for various applications (2D imaging, 2D phase-imaging, single-point range finder, Time-Correlated-Single-Photon-Counting).

To validate the operation principle, a test chip consisting of a 16x16-pixel array has been fabricated in a HV 0.35-μm CMOS technology. The sensor features a minimum detectable photon density of 10^8 photons/cm^{2}s, with a maximum dynamic range of over 120dB. Time-resolved measurements of fluorescence light have been successfully demonstrated. In the following sections, the pixel read-out circuit will be described, the overall chip architecture and the SPAD characteristics will be presented and selected experimental results will be shown.

II. MEASURING TECHNIQUE

The adopted measuring technique, based on a time-gated detection method and the system setup are sketched in Fig. 1.

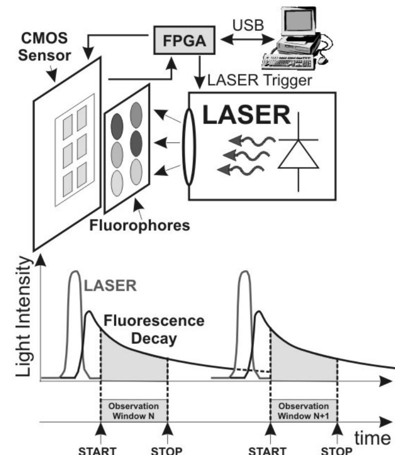

Figure 1: System setup and measuring technique.

An FPGA module, interfaced to a PC via USB, provides all the digital control signals required by the sensor and triggers a pulsed laser (FWHM=80ps) which illuminates the biological sample containing the fluorophores. The adopted measuring technique is based on a time-gated detection method, where the light signal is detected by using two or more observation windows. Each window has an externally programmable time width and can be delayed with respect to the trigger of the laser pulse by a user-defined time value. The time offset between the laser pulse and the beginning of the observation window offers the possibility of suppressing unwanted background signals like scattering and auto-fluorescence. This improves the signal-to-background ratio when the light intensity is measured.

The measurement starts setting the first observation window synchronized with the laser trigger. If an avalanche event is generated within this window it will be detected by the in-pixel event counter. The measurement is then repeated for a programmable number of times (N_P) so that a significant statistical population can be obtained. After that, other N_P measurement cycles are performed by using time delayed observation windows. At the end of the full measurement it is possible to sketch a histogram reporting the number of detected events within each observation window.

III. Pixel Architecture

The schematic cross section of the implemented SPAD and the pixel circuit schematic are shown in Fig. 2. The pixel consists of a SPAD, a reset transistor Mp1, a voltage comparator (INV1) for the avalanche event detection and a voltage buffer (BU1) for the 5V-to-3.3V conversion.

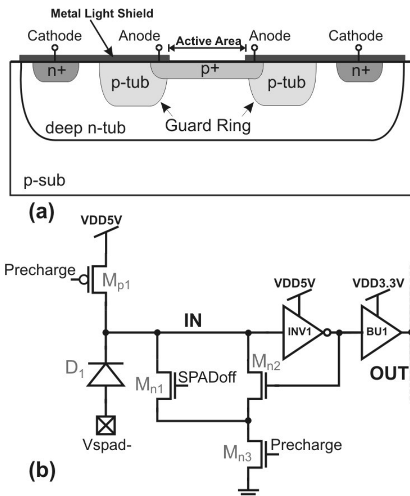

Figure 2: (a) SPAD cross-section and (b) pixel schematic.

The geometry of the SPAD is square to optimize the area occupation, but the corners are smoothed so as to avoid electric field peaks at the junction corners.

Edge breakdown is prevented by means of a guard-ring surrounding the p+ implantation obtained using the special p-tub layer which is available inside a deep n-tub in high voltage processes.

The active area is defined by means of an optical window opened in the metal light shield only in correspondence with the region where avalanche multiplication occurs.

The cathode of the SPAD is connected through an active recharging circuit to VDD5V, and the biasing above the breakdown voltage $|Vb| \approx 28$ V of the SPAD is assured by means of the external line Vspad- biased at a very negative voltage.

The feedback loop, consisting of INV1 and Mn2, realizes an active quenching mechanism, able to force the input node to ground as soon as an avalanche event is detected. In so doing only the first avalanche event is detected while rejecting possible after-pulses. At each clock cycle an active low Precharge pulse biases the SPAD in the breakdown region so that the detector is ready to detect photons. Each observation window starts at this moment (OUT is pulled down by the voltage comparator). When a photon is absorbed by the SPAD, the avalanche is triggered and the node *OUT* is pulled up.

IV. Chip Design and Architecture

The overall chip architecture is sketched in Fig. 3.

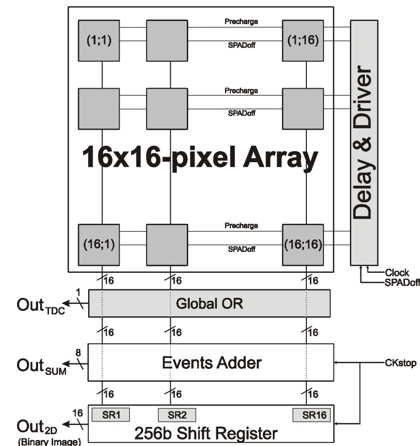

Figure 3: Sensor architecture.

The 16x16-pixel array can be addressed by using three different operation modes externally set up by the user:

- 2D-mode: at the end of the observation window (rising edge of the Ckstop signal), each pixel can be read out serially by means of the 256b shift register to obtain a binary image at each measurement cycle (Out_{2D}).
- 1D-mode: as an alternative, the pixel array can operate as a single big-pixel, simply adding together all the events obtained from each single pixel (Out_{SUM}).
- TCSPC-mode: with a logical OR operation of all the pixel outputs (Out_{TDC}), it is possible to identify the

first avalanche event and use its arrival time information with an external time to digital converter, in order to obtain a Time Correlated Single Photon Counting (TCSPC) measurement.

The microphotograph of the fabricated sensor, where the main functional blocks have been evidenced, is shown in Fig. 4.

Figure 4: Chip micrograph.

V. EXPERIMENTAL RESULTS

Preliminary experimental results, as obtained from electro-optical characterization of on-chip test structures, are summarized hereafter. The SPAD dark count, as obtained from a 20x20μm^2 test structure at room temperature, is shown in Fig. 5, while Fig. 6 reports the measured spectral dependence of Photon Detection Probability (PDP).

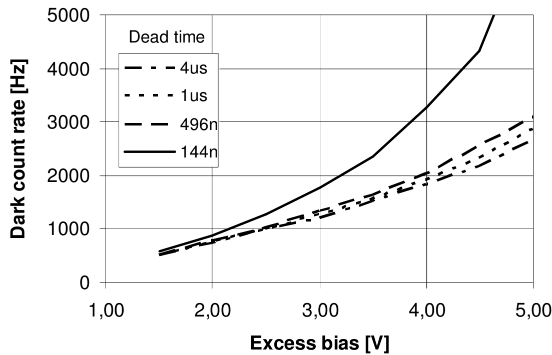

Figure 5: SPAD dark count as a function of the bias voltage and for different dead time values.

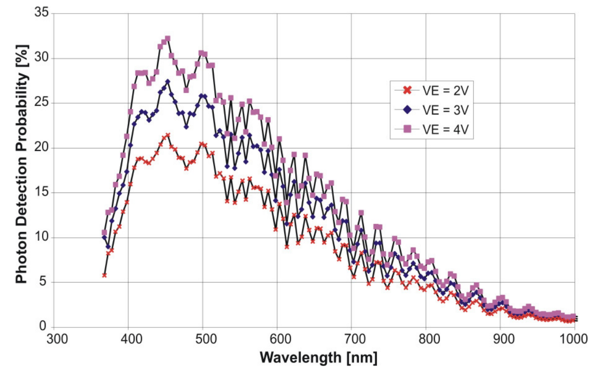

Figure 6: SPAD Photon Detection Probability for different values of the excess bias voltage.

A characterization of the number of counts as a function of optical power density has been performed on a dedicated electro-optical bench (see Fig. 7), demonstrating the high dynamic range capability of the proposed sensor.

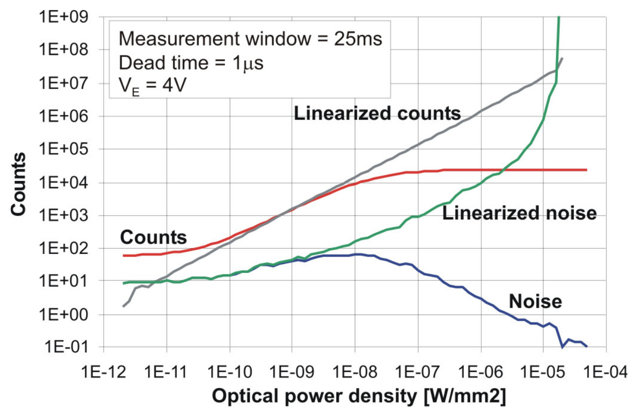

Figure 7: Sensor power responsivity curve. The number of signal counts and noise are shown.

The timing resolution has been measured using a pulsed semiconductor laser (λ=480nm) with 80ps pulse width and a TCSPC instrument. The resolution measured on a 20-μm SPAD at 5V excess bias is 160ps FWHM and 550ps FWM/100 (**Error! Reference source not found.**).

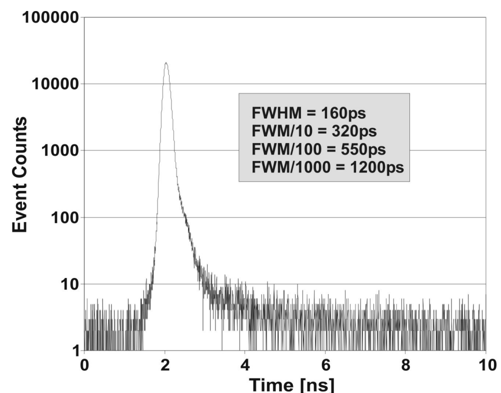

Figure 8: System time resolution.

Finally, the measurement of fluorescence decay curves, as obtained from a CdSe/ZnS quantum dot fluorophores (Evident Technologies), considering different sample concentrations is shown in Fig. 9. For this measurement the observation windows width is 10ns and the time shift is 61ps.

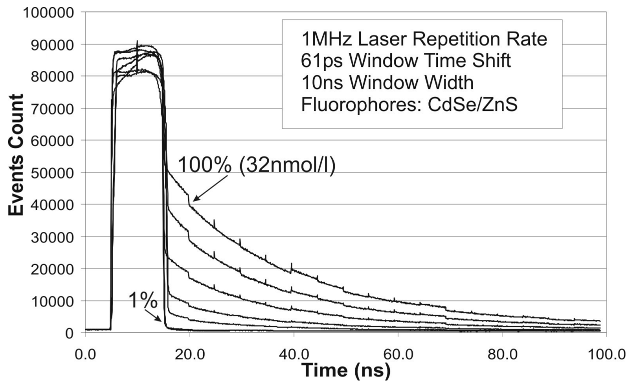

Figure 9: Measurement of fluorescence decay curves with different sample concentrations.

To prove the validity of the proposed approach, a comparative measurement of fluorescence decay obtained with our sensor, using internal time-gated detection, and coupled to a commercial TCSPC module (PicoQuant PicoHarp 300) is shown in Fig. 10.

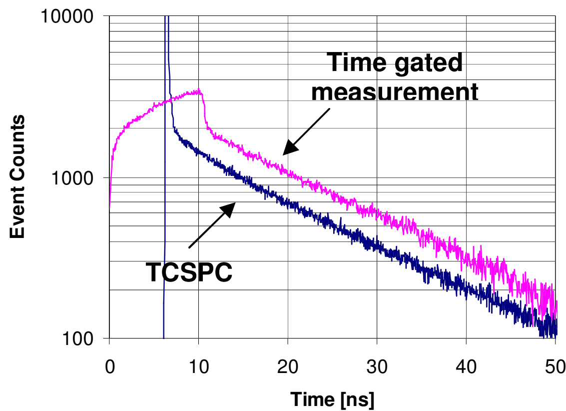

Figure 10: Comparative measurement of fluorescence decay with our sensor using internal time-gated detection and coupled to a commercial TCSPC module (PicoQuant PicoHarp 300).

The main chip characteristics are summarized in Table I.

TABLE I. PERFORMANCE OF THE DEVELOPED SPAD SENSOR.

Technology	0.35µm, 3.3V HV CMOS (2P-4M)
Pixel dimensions	100µmx100µm
Fill factor	30%
Array size	16x16-pixel
Die size	2.660 x 2.740 mm^2

VI. CONCLUSIONS

A pixel architecture implementing a SPAD detector and dedicated read out circuitry for fluorescence lifetime measurements has been presented. Each pixel allows for single photon detection and measures the number of events generated within a user-defined observation window. A preliminary test-chip, consisting of a 16x16-pixel array, has been fabricated in a high-voltage 0.35-µm CMOS technology allowing the measurement of photon densities as low as 10^8 photons/cm^2s. Time-resolved measurements has been demonstrated by detecting fluorescence decay curve of commercially available reference fluorophores.

ACKNOWLEDGMENT

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REFERENCES

[1] R. Cubeddu, D. Comelli, C. D'Andrea, P. Taroni, G. Valentini, "Time-resolved fluorescence imaging in biology and medicine", J. Phys. D: Appl. Phys., no. 35, R61-R76, 2002.

[2] J. R. Lakowicz, "Principles of Fluorescence Spectroscopy", 2nd edn., Springer-Verlag, New York, 1998.

[3] M. Straub, S. W. Hell, "Fluorescence lifetime three-dimensional microscopy with picosecond precision using a multifocal multiphoton microscope", Appl. Phys. Lett. vol. 73 (13), pp. 1769-1771, 1998.

[4] A. Rochas et al., "Low-Noise Silicon Avalanche Photodiodes Fabricated in Conventional CMOS Technologies", IEEE Trans. on Electron Devices, Vol. 49, No. 3, pp. 387-394, March 2002.

[5] C. Niclass, A. Rochas, P.-A. Besse, E. Charbon, "Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes", Solid-State Circuits, IEEE Journal of Vol. 40, No. 9, pp. 1847-1854, 2005.

[6] F. Zappa, S. Tisa, A. Gulinatti, A. Gallivanoni and S. Cova, "Monolithic CMOS detector module for photon counting and picosecond timing", IEEE Proc. of ESSDERC, pp. 341-344, 2004.

[7] S. Tisa, A. Tosi and F. Zappa, "Fully-integrated CMOS single photon counter" Optical Society of America - Optics Express, Vol. 15, No. 6, pp. 2873-2887, 2007.

[8] B. F. Aull et al., "Geiger-Mode Avalanche Photodiodes for Three-Dimensional Imaging", Lincoln Laboratory Journal, Vol. 13, No. 2, pp. 335-350, 2002.

[9] D. Mosconi, D. Stoppa, L. Pancheri, L. Gonzo, A. Simoni, "A Single-Photon Avalanche-Diode 3D Imager", IEEE Proc. of ESSCIRC, pp. 487-490, 2005.

[10] D. Stoppa, L. Pancheri, M. Scandiuzzo, L. Gonzo, G.-F. Dalla Betta, A. Simoni, "A CMOS 3-D Imager based on single photon avalanche diode", IEEE Trans. on Circuits and Systems I, Vol. 54, No. 1, pp. 4-12, 2007.

A TOF range image sensor with an ambient light charge drain and small duty-cycle light pulse

Tomonari Sawada [1], Shoji Kawahito [1], Masakatsu Nakayama [1], Kana Ito [1], Izhal Abdul Halin [1], Mitsuru Homma [2], Takeo Ushinaga [2] and Yasunari Maeda [3]

[1]Shizuoka University, 3–5–1, Johoku, Hamamatsu, Shizuoka, 432–8011 JAPAN
[2] Sharp Corporation, Tenri, Nara, JAPAN
[3] Suzuki Motor Corporation, Hamamatsu, Shizuoka, JAPAN

***Abstract*— This paper presents a TOF range image sensor with an ambient light charge drain and small duty-cycle light pulse. Under the same optical energy consumption of light source, the charge drain and small duty-cycle for the gate control pulse more effectively reduce the influence of ambient light than that of using a 50% duty pulse or a sinusoidal modulation. The effect of the ambient light charge drain is analyed and confirmed with an experiment. A prototype CMOS range image sensor with the spatial resolution of 336×252 pixels and the pixel size of 15×15μm^2 is implemented in a 0.35μm 2-ploy 3-metal standard CMOS process The range resolution of 5.0mm is achieved with a light pulse width of 25ns at 30frames/s.**

***Index Terms*— Time-of-Flight, TOF, range image sensor, ambient light charge drain**

I. Introduction

3-D imaging systems can be used in a variety of applications such as automobile, robot vision systems, security and so on. Many kinds of range finding methods have been proposed for 3-D measurements. TOF range imaging is one of 3-D image capture methods. The range L is determined by sensing the roundtrip time of flight of light and is given by $L = cT_d/2$, where $c = 3\times10^8$ m/sec is the speed of light and T_d is the roundtrip time of flight of light. Recently, many TOF range image sensors have been reported [1], [2], [3], [4]. A method of the TOF range imaging uses a sinusoidal modulated light pulse [1]. In this method, the pixel driving frequency must be increased for achieving higher range resolution. This method uses a range calculation method with reduced influence of ambient light. However, there is no effect for reducing the ambient light charge itself. This paper presents a TOF range image sensor with an ambient light charge drain and small duty-cycle light pulse. A small duty-cycle light pulse is effective for increasing the range resolution without increasing the pixel operation frequency, while suppressing the influence of ambient light by draining the ambient light charge during the off-state of the LED.

II. Sensor Design

A. Pixel structure

Fig.1 shows the pixel layout and the cross-sectional views of x-x' and y-y' directions. A pixel structure of the sensor employs single layer polysilicon gates on relatively thick oxide. Using these single layer polysilicon gates, the sensor achieves high-speed charge transfer like a CCD which is essential for TOF range imaging and can divide signal charge into two floating diffusions (FD) depending on delay time (x-x' direction). In the photodetector region of the pixel, high-speed photo response is achieved by using a lightly-doped p-epitaxial layer on a highly doped p-type substrate. A single additional mask only is used to create an n-type buried layer which prevents the Si-SiO$_2$ interface traps from causing charge transfer delay. A pixel structure of the sensor has a function of ambient light induced charge reduction (y-y' direction). Compared with our previous design [5], the potential profile near the n$^+$ drain region is changed and size of $\mathrm{TX_{CD}}$ gate is enlarged to improve performance of the ambient light charge draining. The potential peak point of the n-type buried layer is changed to deeper side in the substrate for reducing the effect of Si-SiO$_2$ interface traps.

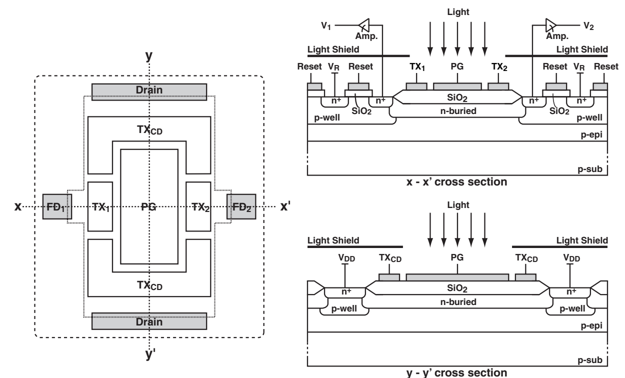


Fig. 1. Pixel layout

B. Timing diagram

Fig.2 shows the timing diagram of the pixel with a small duty-ratio light pulse. The duty-ratio R_D is defined as $R_D = T_P/T_C$, where T_P is the gate pulse width and T_C is the cycle. Using $\mathrm{TX_1}$, $\mathrm{TX_2}$ and $\mathrm{TX_{CD}}$ gates, charge in phases A and B due to mostly signal light pulse is transferred to two FD nodes and charge in phase C due to mostly ambient light

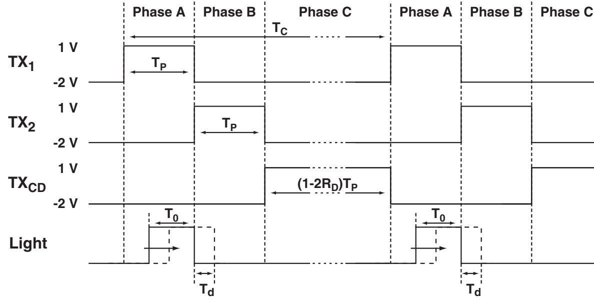


Fig. 2. Timing

is drained. The difference of the amount of charge between the two FD nodes reflects the time-of-light of light pulse. The operation in phase C is for ambient light charge drain. Under the same optical energy consumption of light source, the operation in phase C in this structure more effectively reduces the influence of ambient light than that of using a 50% duty pulse or a sinusoidal modulation. Furthermore, the instantaneous power of the LED can be increased to a value higher than the maximum ratings of the DC operation of the LED if a small duty-cycle pulse is used. This leads to an economical use of the LED.

III. Influence of Ambient light to range resolution

A. Range Estimation

Fig.3 shows the pixel potential profile. The charges generated in phases A, B and C are transferred to FD_1, FD_2, and drains, respectively. The same procedure is repeated for M times during accumulation time, then the TOF pixel output voltages V_{OUT1} and V_{OUT2} are given by

$$V_{OUT1} = V_1 + V_{A1} = \frac{MI_{ph}(T_0 - T_d)}{C_1} + V_{A1} \qquad (1)$$

and

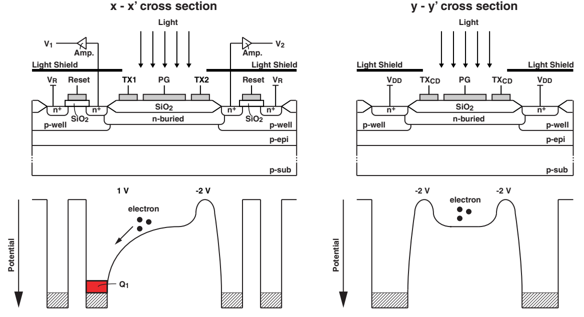
$$V_{OUT2} = V_2 + V_{A2} = \frac{MI_{ph}T_d}{C_2} + V_{A2} \qquad (2)$$

where I_{ph} is the photocurrent induced by the received light pulse, T_0 is the light pulse width, V_{A1} and V_{A2} are the voltages of ambient light components in phases A and B, and C_1 and C_2 are the capacitances of FD_1 and FD_2, respectively. The ambient light components are obtained by mearsuring V_{OUT1} and V_{OUT2} without the signal light pulse. From Eq.(1) and Eq.(2), T_d is given by

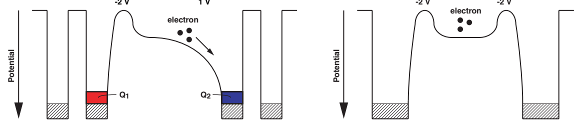
$$\begin{aligned} T_d &= \frac{V_{OUT2} - V_{A2}}{V_{OUT1} - V_{A1} + V_{OUT2} - V_{A2}} T_0 \\ &= \frac{V_2}{V_1 + V_2} T_0 \end{aligned} \qquad (3)$$

, if $C_1 = C_2$. The range from the sensor to the object, L, is given by

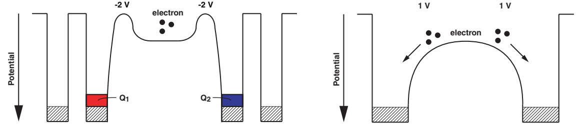
$$L = \frac{1}{2} c T_d = \frac{1}{2} c \frac{V_2}{V_1 + V_2} T_0 \qquad (4)$$



(a) Phase A



(b) Phase B



(c) Phase C

Fig. 3. Pixel Cross Sections and Potencial profiles

B. Range Resolution order Ambient illumination

Range resolution could be estimated by considering the variance of Eq.(4) which is written as

$$\begin{aligned} \sigma_L^2 = &\left(\frac{\partial L}{\partial V_2}\right)^2 \sigma_{V_2}^2 + \left(\frac{\partial L}{\partial V_{12}}\right)^2 \sigma_{V_{12}}^2 \\ &+ 2\left(\frac{\partial L}{\partial V_2}\right)\left(\frac{\partial L}{\partial V_{12}}\right)\sigma_{V_2 V_{12}} \end{aligned} \qquad (5)$$

where V_{12} is the sum of V_1 and V_2, $\sigma_{V_2}^2$ and $\sigma_{V_{12}}^2$ are the variance of V_2 and V_{12}, respectively. The covariance $\sigma_{V_2 V_{12}}$ equals to $\sigma_{V_2}^2$, since V_1 and V_2 are not correlated. From Eq.(4) and Eq.(5), the range resolution is given by

$$\sigma_L^2 = \left(\frac{cT_0}{2}\right)^2 \left(\frac{\overline{V_2}}{\overline{V_{12}}}\right)^2 \left\{\frac{\overline{V_{12}} - 2\overline{V_2}}{\overline{V_{12}}}\left(\frac{\sigma_{V_2}}{\overline{V_2}}\right)^2 + \left(\frac{\sigma_{V_{12}}}{\overline{V_{12}}}\right)^2\right\} \qquad (6)$$

Noise sources such as fixed pattern noise (FPN), thermal noise, dark current and photon shot noise (PSN) degrades range resolution. The PSN caused by ambient light illumination is unavoidably added during signal accumulation and remain in the signal components even if ambient light cancellation is done. Circuit readout noise, N_R from the output source follower, column FPN canceling circuits and output buffer amplifiers are also superimposed on the signal. This noise component is doubled to take the doubling effect of readout

noise power into account if two neighboring frame readouts are taken for subtracting ambient light generated electrons. Ambient light generated electrons or simply ambient noise, N_A is constant. The electrons which are not transfered to drain in phase C is given by $(1-R_A)(1-2R_D)N_A$, where R_A is the ratio of ambient light charge drained and that transferred to FD_1 at the next phase A. By considering these noise sources and their amounts, $\sigma_{V_2}^2/\overline{V_2}^2$ and $\sigma_{V_{12}}^2/\overline{V_{12}}^2$ are given by

$$\left(\frac{\sigma_{V_2}}{\overline{V_2}}\right)^2=\left(\frac{\sigma_{N_2}}{\overline{N_2}}\right)^2=\frac{\overline{N_2}+K_C\left(R_D\overline{N_A}+\overline{N_R}^2\right)}{\overline{N_2}^2} \quad (7)$$

and

$$\left(\frac{\sigma_{V_{12}}}{\overline{V_{12}}}\right)^2=\left(\frac{\sigma_{N_{12}}}{\overline{N_{12}}}\right)^2$$
$$=\frac{\overline{N_{12}}+K_C\left[\{2R_D+(1-R_A)(1-2R_D)\}\overline{N_A}+2\overline{N_R}^2\right]}{\overline{N_{12}}^2} \quad (8)$$

respectively, where N_1, and N_2 are the numbers of electorons in FD_1, and FD_2, respectively, N_{12}=N_1+N_2, and K_C is a factor of the noise increase due to ambient light canceling. If ambient light canceling is used, K_C=2, and otherwise K_C=1. By substituting Eq.(7) and Eq.(8) into Eq.(5), the standard deviation of range, or range resolution is expressed as

$$\sigma_L=\frac{1}{2}cT_0\left(\frac{1}{\overline{N_{12}}}\right)^2\sqrt{\begin{aligned}&\overline{N_{12}}^2(\overline{N_2}+K_CR_D\overline{N_A}+K_C\overline{N_R}^2)\\&+\overline{N_2}^2\left[\overline{N_{12}}+\{2R_D+(1-R_A)(1-2R_D)\}K_C\overline{N_A}\right.\\&\left.+2K_C\overline{N_R}^2\right]-2\overline{N_2N_{12}}(\overline{N_2}+K_CR_D\overline{N_A}+K_C\overline{N_R}^2)\end{aligned}} \quad (9)$$

For the worst case where $\overline{N_2}=\overline{N_{12}}/2$, Eq.(9) reduces to

$$\sigma_L=\frac{1}{4}cT_0\frac{1}{\sqrt{\overline{N_{12}}}}\times\left(\sqrt{1+\frac{\{2R_D+(1-R_A)(1-2R_D)\}K_C\overline{N_A}+2K_C\overline{N_R}^2}{\overline{N_{12}}}}\right) \quad (10)$$

If N_A is small, the range resolution depends mainly on the light pulse width and the number of accumulated signal electrons, and is simplified to

$$\sigma_L\simeq\frac{1}{4}cT_0\frac{1}{\sqrt{\overline{N_{12}}}}\sqrt{1+K_C\frac{2\overline{N_R}^2}{\overline{N_{12}}}} \quad (11)$$

IV. Measurement Results

A prototype CMOS range image sensor with the spatial resolution of 336×252 pixels and the pixel size of 15×15μm ^{2} is implemented in a 0.35μm 2-ploy 3-metal standard CMOS process and tested using an array of near-infrared LEDs with the wavelength of 870nm.

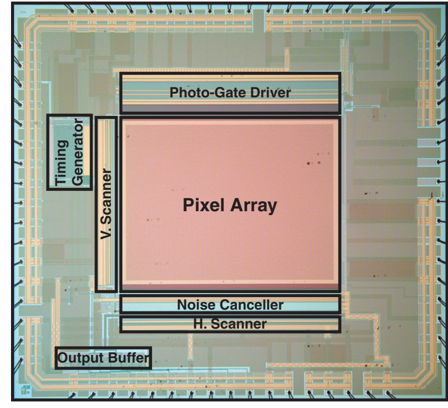


Fig. 4. Photomicrograph of the prototype sensor chip

A. Sensitivity to the Delay time T_d

Fig.5 shows the pixel outputs of V_1 and V_2, the difference V_1-V_2, and the sum V_1+V_2, as a function of delay time T_d. The difference of the two sensor outputs varies linearly with respect to T_d, but the sum V_1+V_2, is almost unchanged in phase A and B. In phase C, the outputs of V_1 and V_2 are reduced, showing the effectiveness of ambient light charge draining.

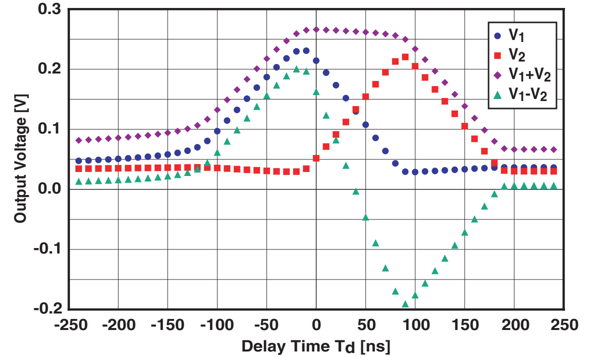


Fig. 5. Pixel Outputs versus the Delay Time T_d

B. Efficiency for Ambient light charge draining

To measurement the efficiency for ambient light charge draining, the TOF sensor is illuminated by an array of near-infrared LEDs with the wavelength of 870nm as a DC source of ambient light. In the total ambient light electorons of N_A, $R_A(1-2R_D)N_A$ is drained, the residual electorns are transferred to FD_1. Therefore, the output voltages are given by

$$V_{A1}=G_C\{(1-R_A)(1-2R_D)N_A+R_DN_A\} \quad (12)$$
$$V_{A2}=G_CR_DN_A \quad (13)$$

where G_C is the conversion gain of pixel. From Eq.(12) and Eq.(13), R_A is expressed as

$$R_A=1-\frac{V_{A1}-V_{A2}}{(1-2R_D)V_{A2}} \quad (14)$$

In the implemented TOF sensor, R_A is measured to be 89.7%.

C. Range Resolutiion

Figs.6 and 7 show the results of range resolution versus signal intensity under no ambient light. The light pulse delay was set such that V_1 equals to V_2 in order to measure the worst case resolution. The solid line is the calculated values using Eq.(11) where N_R is 75 electrons. The minimum range resolution at 30frames/sec and the light pulse width of 25ns is 5.0mm. The range resolution is improved by a factor of $\sqrt{N}$ for averaging of Ntimes. The resolution at 3frames/sec, which corresponds to the averaging of 10times is 1.7mm.

Fig.8 shows the result of range resolution versus signal intensity measured at 30frames/sec. In the curve measured under ambient light, ambient light canceling is carried out. The ambient light components are measured without signal light, and averaged 100 times to reduce the noise. The solid line are the calculated values using Eq.(10) and Eq.(11). The light pulse delay is set to measure the worst case resolution. The range resolution at high signal intensity approximates to the range resolution under no ambient light. The range resolution at low signal intensity is deteriorated by the influence of ambient light.

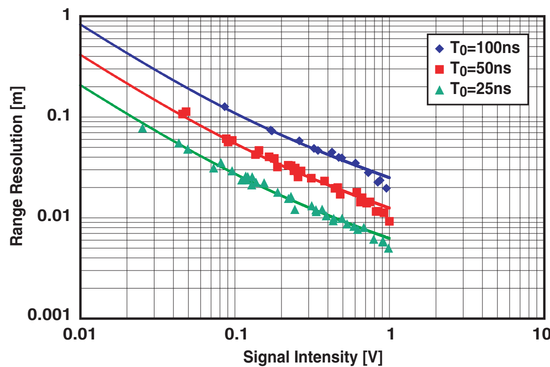


Fig. 6. Range Resolution (30frames/sec)

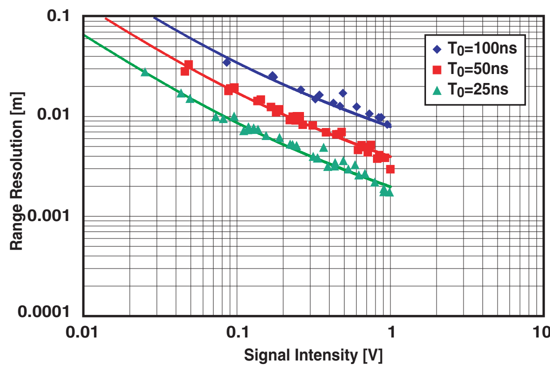


Fig. 7. Range Resolution (3frames/sec)

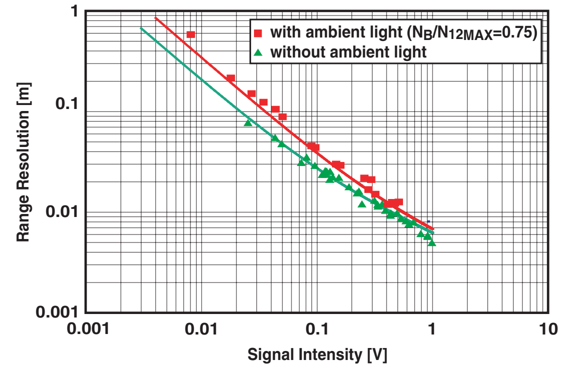


Fig. 8. Range Resolution with Ambient Light for T_0=25ns (30frames/sec)

V. Conclusion

In this paper, the design, analysis of the influence of ambient light to range resolution and implementation of a TOF range image sensor with an ambient light charge drain and small duty-cycle light pulse have been presented. The theoretical model of the range resolution under the influence of ambient light relativery well agrees with the experimental results.

Acknowledgment

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References

[1] B. Büttgen, et al., ”High-Speed and High-Sensitive Demodulation Pixel for 3D-Imaging”, SPIE Proceedings of the SPIE, pp. 22-33, 2006
[2] R. Miyagawa, et al., “CCD-Based Range-Finding Sensor”, IEEE Trans. ED, 1997
[3] D. Stoppa et al., “A 50x30-pixel CMOS Sensor for TOF-based Real Time 3D Imaging”, IEEE Workshop CCD&AIS, pp.230–233, 2005
[4] C. Niclass et al., “A Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging”, IEEE ISSCC, pp.364–365, 2005.
[5] I. Abdul Halin, et al., “A CMOS Time-of-Flight Range Image Sensor with Gates on Field Structure”, IEEE Sensors, pp.141–144, 2005.

Dynamic Quenching for Single Photon Avalanche Diode Arrays

Justin Richardson[1,2], Robert K. Henderson[1], David Renshaw[1]
[1]The University of Edinburgh, Institute for Integrated Micro and Nano Systems, Edinburgh, U.K.
[2]STMicroelectronics Imaging Division, Edinburgh, UK

SUMMARY

We propose the use of dynamic circuits for quenching avalanche events in single photon avalanche diode (SPAD) arrays. Two area-efficient, circuit solutions are presented in 0.35μm CMOS technology. These circuits contain no passive elements and consume shoot-through current only at triggering instants. The resulting reduction in power consumption and supply noise is essential to formation of large imaging arrays of SPADs.

I. INTRODUCTION

The quest for low-cost, high-performance SPAD arrays with integrated on chip signal processing for both time correlated and uncorrelated applications is now being driven by emerging markets such as biotechnology, automotive and 3D-imaging. Demand for increased accuracy and time resolution is shifting the focus of research from passive to active detector quenching mechanisms. This is due to the requirement that the two primary noise sources in single photon imaging systems, dark count rate (DCR) and pulse jitter be minimized. The former results in false triggering or arrival events while the latter causes ranging errors in 3D imaging systems. Both noise sources require averaging which is expensive in die area and processing speed.

Quenching is the process of halting a detector's avalanche breakdown and priming the device ready for the next photon arrival, and may be done passively[1], actively or a hybrid approach[3-8]. Active quenching employs feedback to improve system linearity due to the reduction of after-pulsing probability as well as reducing power consumption and crosstalk[3]. Quenching circuits with passive elements suffer from static consumption during quenching which is particularly undesirable for a large imaging array.

In this paper we present two circuits which exhibit purely dynamic power consumption ensuring reduced supply noise and SPAD self-heating effects. In the solutions presented here the detector is effectively isolated from the supply, thus reducing the potential for nonlinearities introduced by variations in excess bias voltage or inter-device crosstalk

II. QUENCH CIRCUITS

Various integrated quench circuits are proposed in the literature:
Most quenching solutions attempt to minimize the avalanche current duration due to self heating, afterpulsing probability and crosstalk issues [3].
A passive quench approach is employed in [2] using a MOS transistor for compactness. Passive quenching suffers from long recharge time. Such methods consume power for the duration of this period, and therefore can suffer self heating effects and longer dead times. In large uncooled detector arrays this may dramatically increase DCR.
References [3],[5] discuss hybrid approaches for larger single detectors, utilising a passive quench resistor and monostable based active quench/reset control. This circuit would be unsuitable for large arrays due to decreased fill factor and power consumption.
References [4], [5] [6] begin to introduce the concept of using the basic CMOS thyristor [2] in a SPAD based detector concept, with logic control being done externally. Again a hybrid quench approach is used.
Reference [7] utilises a passive/active quench hybrid with fixed built in delay active reset, although the active reset path uses some passive components so may suffer from higher power consumption.
Reference [8] has no passive elements and a feedforward active avalanche control, but consumes static current for the duration of the breakdown pulse and requires external logic for precharging.
Most work on integrated quench circuits apart from [1,6] addresses single detector systems. In general these are unsuitable for arrays of detectors with fully integrated readout and programmable active quench mechanisms where low power consumption and high fill factor is of primary concern.

III. OPERATION

The quench circuit proposed in this paper is based on a CMOS thyristor delay cell approach[3], the basic building block of which is shown in Fig. 1.

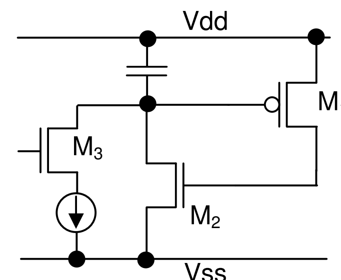

Figure 1: CMOS Thyristor Delay Cell

Referring to Fig. 2, the power supplies are *Vop* at the magnitude of the reverse breakdown voltage of the SPAD structure, and *Vdd* of magnitude of the excess reverse

breakdown (*Ve*) voltage selected to satisfy photon detection probability (PDP) and dark count rate (DCR) specifications. Under quiescent conditions *midpoint* and *Vcathode* nodes are high impedance and power consumption is minimized. When the detector fires the positive feedback loop of M_1 and M_4 promotes the discharge and clamps the SPAD cathode to 0V. A delay time later the latched condition is reset via the dominant drive strength PMOS M_3 and disabled through NMOS M_2. Capacitive elements are MOS gates thus providing a purely CMOS transistor solution. Simulation results are shown in Fig. 3.

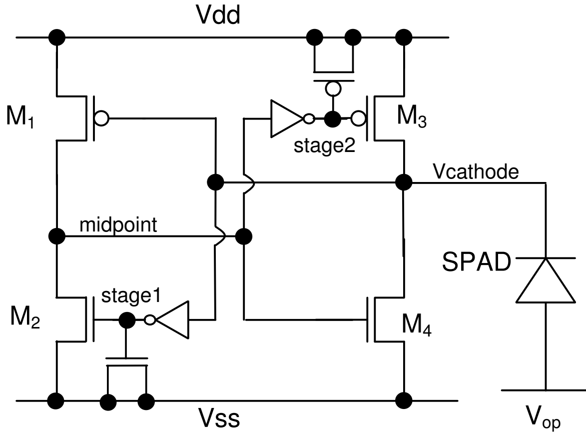

Figure 2: Dynamic Quench Circuit A

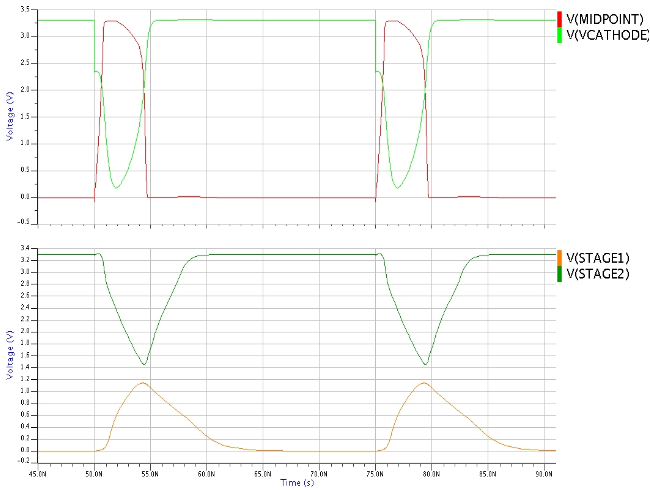

Figure 3: Simulation Results for Circuit A: two consecutive detector firings.

Alternatively, Fig. 4 shows a development of Fig. 2, still using the feedforward principle but employing an unbalanced threshold inverter delay chain which provides a well defined quench pulse duration but a fast subsequent reset. Using such a scheme also provides opportunity for integrating enable/disable and global pulse duration adjustment functions via the introduction of appropriate logic and current starved inverters respectively.

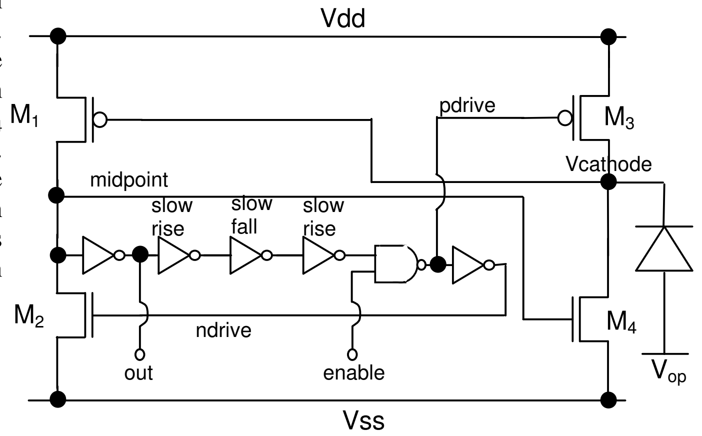

Figure 4: Dynamic Quench Circuit B

Simulation results for circuit B are given in Fig. 5. The circuit operation has been verified over all process corners from -30 to +70°C.

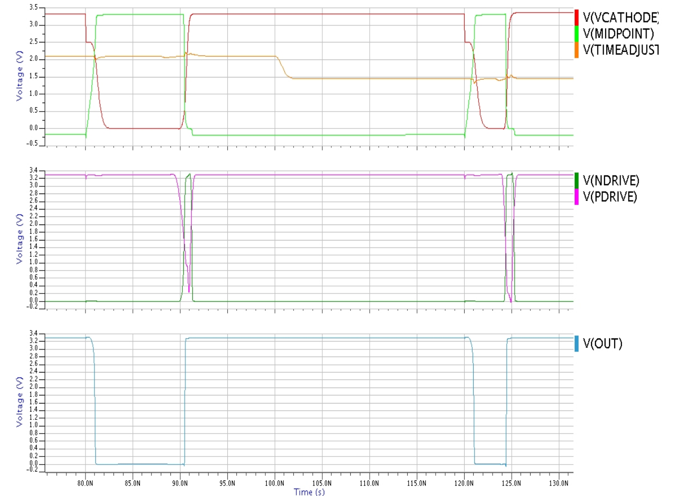

Figure 5: Simulation Results for Circuit B: two detector firings with different quench times

IV. Effects of Leakage

We omit a quench resistor altogether relying on the dominant subthreshold leakage of PMOS M_3 over NMOS M_4 to maintain the SPAD at a high potential between avalanche events (~8:1 width). Similarly, the M_2/M_1 sizing relationship (2:1 width) contributes to correct quiescent potential on node *midpoint* so avoiding erroneous leakage induced triggering. The charge injection on the *Vcathode* and *midpoint* nodes via control signals *pdrive*/*ndrive* respectively is also in the correct sense to provide gate overdrive on the M_4 pull-down and M_1 pull-up devices to minimize sub-threshold leakage in those devices and thus promoting the correct dominant current path. This must be maintained over process corners and temperature. Should the conditions be violated DCR will increase at ~20Hz/pA of unbalance, for our detectors.

Note there is a device sizing trade off between the thyristor feedforward loop delay and the creation of the correct leakage relationships.
A tabulated performance summary is shown in Table 1.

Technology	0.35µm 4ML CMOS
Transistor Count	20T
Area	130µm^2
Supply Voltage	1.7 - 3.6V
Power Consumption	60µW average @ 25MHz firing rate.
Quench duration	2 – 30ns
Arming (enable) Time	300ps
Feed fwd trigger time	100 - 500ps

Table 1: Circuit B Performance Summary

V. Circuit Implementation

A current starved inverter chain is used for the purposes of tuning the quench delay time. The basic slow rise-fast fall cell used in the delay generator is shown in Fig. 6.

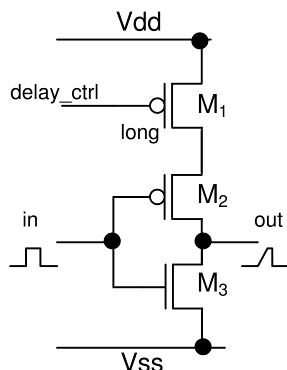

Figure 6: Slow Rise-Fast Fall Current Starved Inverter Cell

The control signal delay_ctrl is used to vary the duration that the SPAD stays in its avalanched state, and hence can be used to set the resolution of event counting in time uncorrelated photon counting mode. It is also known that the quench duration and SPAD afterpulsing are related [3] and so this may be traded off against PDP.

Power Consumption

Disregarding the SPAD recharge consumption, circuit B standalone consumes an average of 60µW from a 3.3V supply at a detector firing rate of 25MHz. This is comparable to passively quenched systems with the advantage of reduced local heating effects plus in built gating and logic output levels.

Layout

The area of circuit B is approximately 130µm^2, and is designed such that large arrays of detectors/quenchers may be formed by abutment, allowing distribution of power supplies and 'global' control signals.

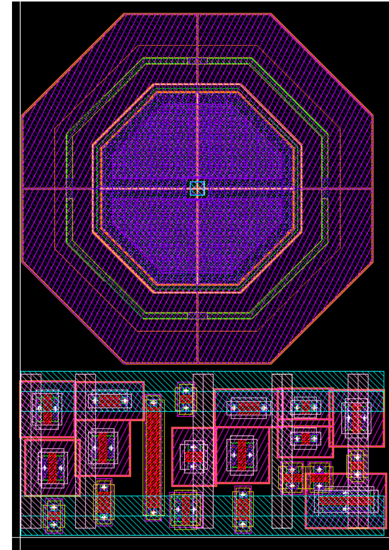

Figure 7: Layout of Circuit B plus Detector

VI. Conclusions

We have reported two novel SPAD active quenching circuit solutions exhibiting advantages over conventional passive/hybrid element approaches, enabling VLSI with detector arrays and on-chip processing for improved performance single photon counting systems.

References

[1] Niclass, Rochas, Besse, Charbon: 'Design and Characterisation of a CMOS 3-D Image Sensor Based on Single Photon Avalanche Diodes'. IEEE JSSC, Vol 40, No. 9, Sept 2005.
[2] G.Kim, M.Kim, Chang, W.Kim: 'A Low Voltage Low Power CMOS Delay Element'. IEEE Journal of Solid State Circuits, Vol 31, No7, July 1996.
[3] Zappa, Ghioni, Cova, Samori, Giudice: 'An Integrated Active-Quenching Circuit for Single Photon Avalanche Diodes'. IEEE Transactions on Instrumentation and Measurement, Vol 49, No. 6, Dec 2000.
[4] Zappa, Giudice, Ghioni, Cova: 'Fully Integrated Active Quenching Circuit for Single Photon Detection'. ESSCIRC 2002.
[5] Tisa, Zappa, Labanca: 'On-chip Detection and Counting of Single Photons'. IEEE Electron Devices Meeting, 2005.
Layers'. ISSCC 2006 Session 16, 16.9.
[6] Aull et al: 'Laser Radar Imager Based on 3D Integration of Geiger Mode Avalanche Photodiodes with Two SOI Timing Circuit
[7] Rochas, Pauchard, Monat, Matteo, Trinkler, Thew, Ribordy: 'Ultra Compact CMOS Single Photon Detector'. Proceedings of SPIE, Vol 6372 2006.
[8] Mosconi, Stoppa, Pancheri, Gonzo, Simoni: 'CMOS Single-Photon Avalanche Diode Array for Time Resolved Fluorescence Detection'. SSCC 2006, ESSCIRC 2006.

A Compact, Low voltage Electron Bombarded Array

S. Nikzad[1], T.J. Jones[1], Michael E. Hoenk[1], Chris Martin[2], Steve Kaye[2], Patrick Morrissey[2]
[1]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109
[2]California Institute of Technology, Pasadena, CA

Low light level imaging applications will depend on detectors with high quantum efficiency (QE), high dynamic range, and stable response. In addition detectors often need to be compact, low power, and robust. Electron-bombarded arrays including electron-bombarded CCDs (EBCCDs) benefit from the mature and high quality silicon imaging technology, and they can provide high efficiency and photon counting capabilities. Of the photoemissive devices, EBCCDs have been reported to have the highest QE. However, their drawback is in the bulky design, use of a magnet to bend electrons, and high voltage requirements. The NASA vision of smaller, lower cost, and more frequent missions mandates the miniaturization of instruments. The compactness and improvement of devices can be a mission-enabling factor. Other fields of observation can also greatly benefit from a compact image intensifier.

A new electron-bombarded CCD (EBCCD) design will be discussed. Key elements of this design are its low-voltage (<1 keV) and proximity-focus mode of operation which does not require a bending magnet. The new design permits a lighter instrument that does not require high voltage supplies. We use a thinned, delta-doped silicon array for detecting low-energy electrons in a compact, magnet-free configuration with a semitransparent cathode. For preliminary measurements Cesium-Iodide photocathodes were paired with the electron detector array. We will present the configuration, spectral discrimination, and sensitivity of our electron bombarded imaging array and we will discuss alternate photocathode approaches that require no cesiation.

Dr. Shouleh Nikzad
Mail Stop 302-306
Jet Propulsion Laboratory
4800 Oak Grove Dr.
Pasadena, CA 91109-8099
(818) 354-7496
(818) 393-4540
email: Shouleh.Nikzad@jpl.nasa.gov.

Figures

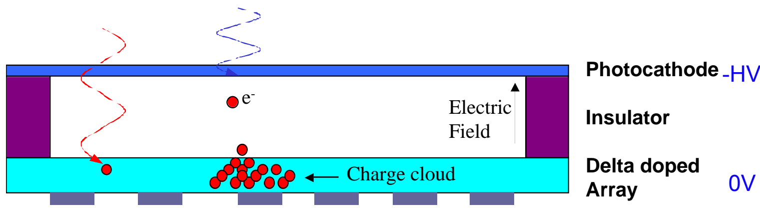

Figure 1. Schematic diagram of a proximity focused low voltage (~1 keV) electron bombarded CCD or CMOS array. The low voltage operation is enabled by direct detection of low energy electrons with a delta-doped array.

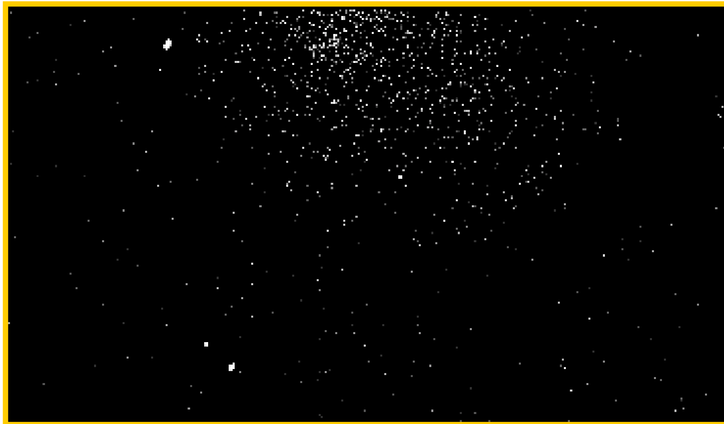

Figure 2. Discrimination against out of band events showing individual UV events.

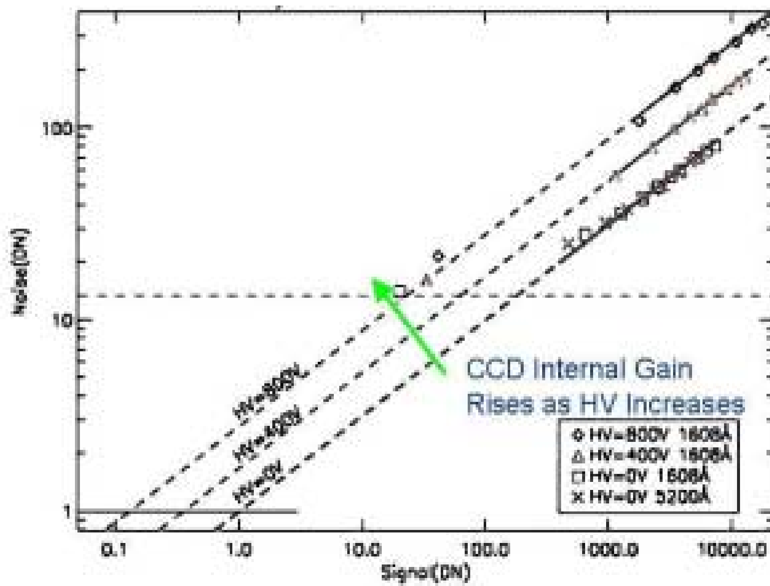

Figure 3 Measured gain as a function of acceleration voltage using photon transfer technique.

High Sensitivity Color CMOS Image Sensor with WRGB Color Filter Array and Color Separation Process Using Edge Detection

Hiroto Honda[*1], Yoshinori Iida[*1], and Yoshitaka Egawa[*2]
[*1] Corporate Research & Development Center, Toshiba Corporation
[*2] Semiconductor Company, Toshiba Corporation

ABSTRACT

We have developed a CMOS image sensor with a novel color filter array (CFA) where one of the green pixels of the Bayer pattern was replaced with a white pixel. A transparent layer has been fabricated on the white pixel instead of a color filter to realize over 95% transmission for visible light with wavelengths of 400-700 nm. Pixel pitch of the device was 3.3 um and the number of pixels was 2 million (1600H x 1200V). By introducing the Bayer-like White-Red-Green-Blue (WRGB) CFA and by using the low-noise color separation process, signal-to-noise ratio (SNR) was improved. Low-illumination SNRs of interpolated *R*, *G*, and *B* values have been increased by 6dB, 1dB, and 6dB respectively, compared with those of the Bayer pattern. The false color signals at the edge have been suppressed by newly developed color separation process using edge detection. This new CFA has a great potential to significantly increase the sensitivity of CMOS/CCD image sensors with digital signal processing technology.

1 INTRODUCTION

A basic trend toward smaller pixels for CMOS image sensors allows a huge number of pixels (more than 10M pixels), but causes decrease of the photodiode area, resulting in decrease of incident photon number.

Moreover, in case of color CMOS image sensors, the color filter loses as much as 2/3 of incident energy.

Conventionally, the pixel area consists of 2 x 2 'unit blocks' that include two green pixels diagonally, one red pixel and one blue pixel (as expressed in Fig.1). This layout of the color filter array (CFA) is called 'Bayer pattern' [1]. The reason why twice as many green pixels are placed as red and blue pixels is that the human eye is most sensitive to green and the green pixel represents the luminance signal of the incident image. As for the YUV color space, luminance signal Y is expressed as follows:

$$Y = 0.59G + 0.30R + 0.11B \qquad (1)$$

Here *G*, *R*, and *B* mean output digital value of green, red, and blue signals, respectively.

Since luminance signal *Y* depends greatly on *G*, Bayer layout has twice as many green pixels as red or blue pixels. However, the need for higher signal-to-noise ratios (SNRs) of red and blue signals is growing.

We developed a CFA including 'white pixels' and the pre-digital low-noise signal processing to process the output values from the CFA, which realize higher SNR of *R*, *G*, and *B* signals compared with the Bayer pattern [2].

2 BAYER-LIKE WRGB COLOR FILTER ARRAY

Figure 1 shows the Bayer layout and the newly developed Bayer-like WRGB layout. In a 2 x 2 unit block one of the two green pixels was replaced with a 'white' pixel. The red, green, and blue pixels have a color filter layer (colored resin film) over the passivation layer.

For the 'white' pixel, a transparent resin film was fabricated instead of a color filter to realize high transmission of visible light with wavelengths of 400-700 nm.

The white pixel was introduced because the incident light is not lost compared with a green pixel.

The reason why 'WRGB' CFA was adopted is that the color representation is maintained by having primary color pixels. Moreover, for complementary CFAs, a reduction is caused in SNR due to subtraction operation during the color conversion [3].

Microlenses are fabricated on each pixel.

The pixel pitch of the device is 3.3 um and pixel number is 1600x1200 (2 megapixels).

Fig. 1. 2 x 2 unit pixel blocks of the Bayer Pattern (left) and the newly developed the Bayer-like WRGB Pattern (right).

Figure 2 shows the spectral sensitivity of each color pixel of WRGB CFA device. The white pixel has higher spectral sensitivity than any of the color pixels in the wavelength of 400-700nm.

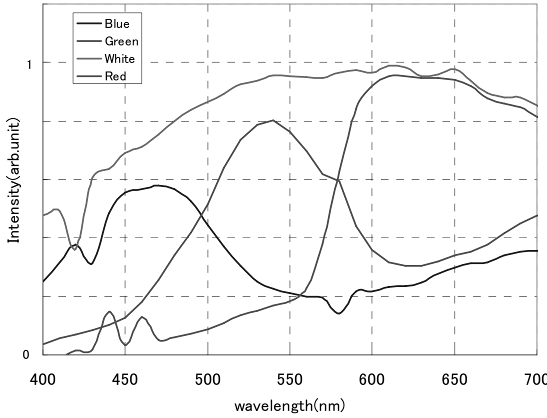

Fig. 2 Spectral sensitivity of each pixel in the Bayer-like WRGB CFA.

3 DIGITAL SIGNAL PROCESSING

3.1 Low-noise color separation process

Since the signal from the white pixel has much luminance information but no color information, we have developed a low-noise color separation process to separate *W* signal value into *R*, *G*, and *B* signal values by referring to color information of the red, green, and blue pixels surrounding the white pixel, as shown in Fig. 3. In detail, we calculated the 'color ratio' of the *G* signal value to the sum of the average of *R*, *G*, and *B* signal values: $G_{average}/(R_{average}+G_{average}+B_{average})$.

For example, $R_{average}$, $G_{average}$ and $B_{average}$ are made of the average values from two red pixels, four green pixels, and two blue pixels surrounding the white pixel, respectively. More pixels can be referred to for calculating each average value to decrease random noise in the color ratio. Next, we multiplied the signal value of the white pixel by the color ratio calculated previously, as follows:

$$R_w = W \times \frac{R_{average}}{(G_{average}+R_{average}+B_{average})} \quad (2)$$

$$G_w = W \times \frac{G_{average}}{(G_{average}+R_{average}+B_{average})} \quad (3)$$

$$B_w = W \times \frac{B_{average}}{(G_{average}+R_{average}+B_{average})} \quad (4)$$

where R_w ,G_w , and B_w are newly obtained color signal values at the white pixel. In equation (2)~(4), *W* value stands for luminance and the color ratio part stands for chrominance.

This process assumes that the chrominance is homogeneous in the region of 3 x 3 pixel area when the color reference region is 3 x 3 pixel area. However, since luminance signal is obtained from the single white pixel, luminance resolution is not degraded.

Afterwards, the pixel interpolation process was performed with both the *R*, *G*, and *B* 'raw' signals and the newly obtained *Rw*, *Gw*, and *Bw* signals. Interpolation was performed by averaging the same-color signals in the region of each 3 x 3 pixel area.

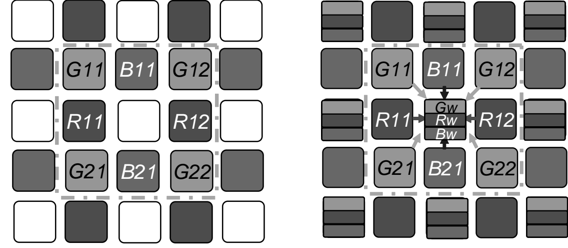

Fig. 3. Concept of the low-noise color separation process (5 x 5 pixel block of the WRGB CFA).

3.2 Edge detection process

The assumption that the chrominance is homogeneous in the color reference region is not correct for the high spatial frequency image. Therefore false color signal appears at the edge after the color separation process.

Edge detection was carried out in the 3 x 3 pixel area surrounding the white pixel, prior to the color separation process. Horizontal edge detection was performed by comparing (*G11+B11+G12*) with (*G21+B21+G22*), as shown in Fig. 4. If the difference between the two sum values is over the threshold value, horizontal edge is detected around the white pixel. Vertical and diagonal edges around the white pixel are also detected.

If an edge is detected, the color separation process is not performed. Instead only a green signal value is generated from white signal value. To coincide the sensitivity of the white signal with that of green signals, white signal value is multiplied by the coefficient α, obtained from the neighboring color ratio.

By branching off the signal process at the edge, we can suppress the false color signal due to the color separation process.

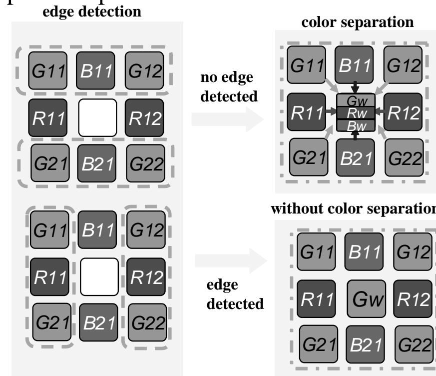

Fig. 4. Color separation process with edge detection.

4 Results

4.1 SNR improvement in low illumination

We took raw data of the Macbeth chart® illuminated by halogen lamp with the color temperature of 6000K, by the image sensor chips with Bayer CFA and Bayer-like WRGB CFA. By using the neutral density (ND) filter (1/512), illumination was controlled to be 3lux.

For the WRGB-CFA data, *Rw*, *Gw* and *Bw* signals were calculated at each white pixel by the low-noise color separation process without edge detection.

For the data of both of the CFAs, interpolation was carried out by using the same-color-signal values in the 3 x 3 pixel block to calculate the *R*, *G*, and *B* values at every pixel. Figure 5 shows low-illumination SNR comparison between the Bayer CFA and WRGB CFA devices. SNR was calculated by using the average and dispersion of values in the grayscale square of interpolated Macbeth images.

SNRs of *G*, *R*, and *B* were increased by 1dB, 6dB, and 6dB, respectively, for the WRGB CFA image. SNR increase of *G* is because of higher sensitivity of a white pixel than a green pixel, and the SNRs of *R* and *B* increased because of doubling of the effective *R* and *B* pixel number.

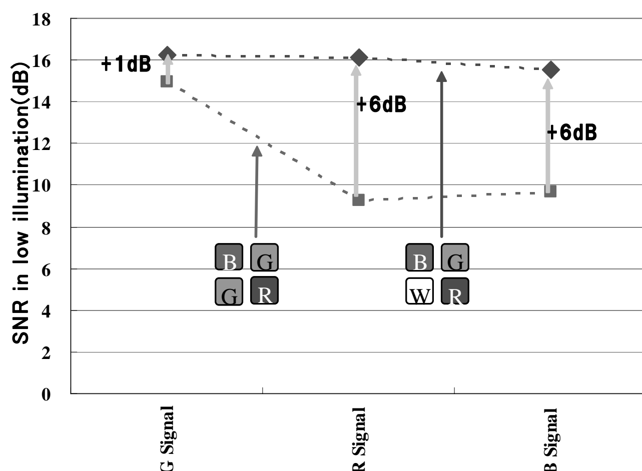

Fig. 5. Low illumination SNR comparison between the interpolated signal of the Bayer CFA and that of the Bayer-like WRGB CFA.

4.2 Color Representation

The Macbeth chart image and the color vector are shown in Fig. 6. Raw data was taken by both the Bayer CFA sensor and the WRGB CFA sensor under high illumination condition.

For the WRGB CFA data, the color separation process and interpolation by using the same-color value of 3 x 3 pixel block were performed. The color vector was obtained from the third line of the Macbeth chart.

Since Bayer-like WRGB CFA has three primary-color pixels and the low-noise color separation process is based on the chrominance signal calculated by using the pure *R*, *G* and *B* values, color could be represented by WRGB CFA without any problem.

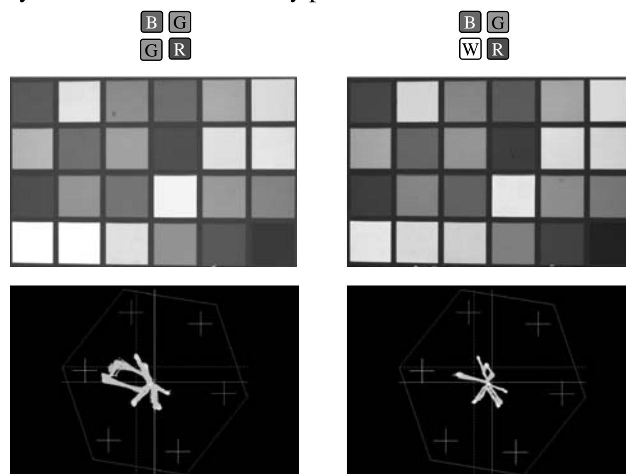

Fig. 6. Macbeth chart comparison between the Bayer-CFA sensor and the WRGB-CFA sensor, taken under a high illumination condition where halogen lamp (6000K) was illuminated onto the reflection-type Macbeth chart.

4.3 Resolution

The Circular Zone Plate (CZP) response was simulated. Color separation and interpolation were performed for the black-and-white CZP image. Figure 7 shows RGB color images after interpolation. Strong color moiré appears at the Nyquist frequency. This is because blue pixel and newly obtained *Bw* effective pixel form vertical lines at intervals of 2 columns after the color separation. After the interpolation and the RGB image synthesis, bright blue moiré pattern appears.

On the other hand, by using edge detection, the CZP response of the WRGB layout (Fig. 8) has become comparable to that of the Bayer layout (Fig. 9).

Figure 10 shows the comparison between the edges of Bayer CFA, WRGB CFA without edge detection, and WRGB CFA with edge detection. False color signal due to the color separation has been suppressed by using the edge detection.

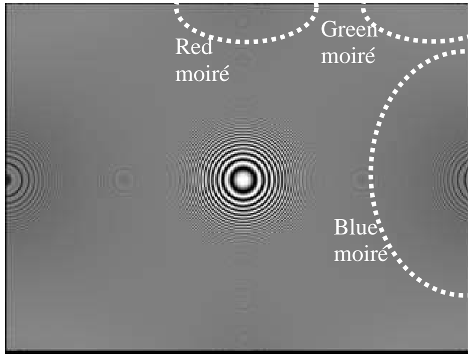

Fig. 7 Circular zone plate response of the WRGB layout without edge detection.

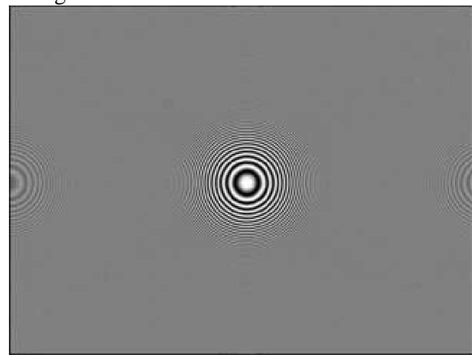

Fig.8 Circular zone plate response of the WRGB layout with edge detection.

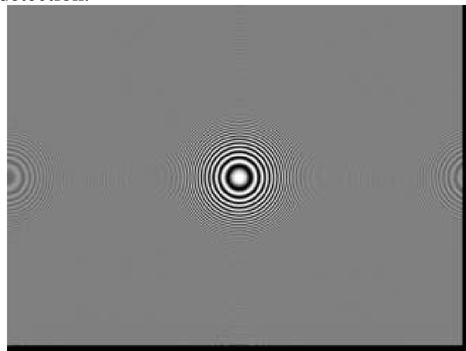

Fig. 9. Circular zone plate response of the Bayer layout.

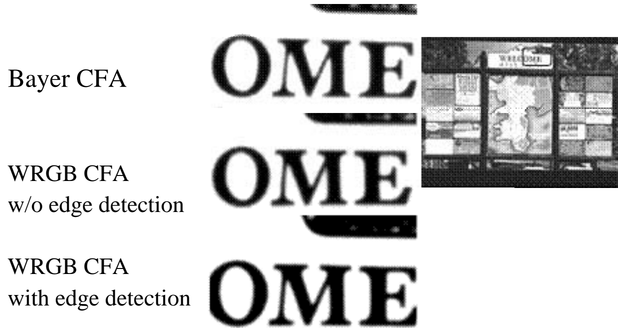

Fig. 10. Comparison between the edges of Bayer CFA, WRGB CFA without edge detection, and WRGB CFA with edge detection.

5 CONCLUSION

We have fabricated a CMOS image sensor with the Bayer-like White-Red-Green-Blue (WRGB) color filter array.

By introducing high-sensitivity white pixel and by using the low-noise color separation process, signal-to-noise ratios (SNRs) have been improved. Low illumination SNRs of the interpolated R, G, and B signal values were increased by 6dB, 1dB, and 6dB respectively, compared with those of the Bayer pattern.

There was no degradation of either resolution or color representation for the interpolated image.

The false color signals at the edge have been suppressed by newly developed color separation process using edge detection.

The issue of the color representation at the edge, where white signal value is regarded as green signal value, is to be solved by improving the color separation algorithm.

This new color filter array has a great potential to significantly increase the sensitivity of CMOS/CCD image sensors with digital signal processing technology.

ACKNOWLEDGEMENTS

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REFERENCES

1. B. Bayer, “Color imaging array”, United States Patent, No. 3, 971,065,1976.
2. H. Honda et. al., “A novel Bayer-like WRGB color filter array for CMOS image sensors”, Electronic Imaging 2007, 2007 (to be published).
3. J. Nakamura, “Image sensors and signal processing for digital still cameras, pp. 62-63; 226-232, 2006.

IR/Color Composite Image Sensor with VIPS(Vertically Integrated Photodiode Structure)

Jeong-Ho Lyu, †Seok Choi, Jae Heon Choi, †Jung Hyun Nam, and †Jin Bok Jung

†Miru Data System Co., Ltd.
Maru LSI Co., Ltd.,
5F, Changhwa B/D, 1005-5, Yeongtong-dong, Yeongtong-gu, Suwon, Korea
TEL: +82-31-205-5786, FAX: +82-31-205-5784
E-mail: jlyu@marulsi.com

Abstract

The CMOS image sensor having VIPS(Vertically Integrated Photodiode Structure) was fabricated for the first time. By adding the high energy(~3MeV) ion implantation to the conventional CIS(CMOS Image Sensor) process, it was verified that the deep photo diode was successfully formed under the normal photodiode on a pixel. And it was observed that this image sensor can detect the visual image and near IR(Infra Red) image at the same time and distinguish the two images.

I. Introduction

It has several advantages for the image processing to obtain separate information of visible range and near IR range at the same time[1], especially in the surveillance system. For example, one can differentiate the patterns from the heated object or from the object which has a different IR absorptivity. Also, the IR cut filter which is implemented on the top of the lens can be removed from the commercial area image sensors. The NIR range below 1.1μm can be detected in the Silicon image sensors. But using the normal photodiode structures or layered photodiode, there is no way to distinguish the IR signal with the R,G, B signal[2], [3].

In this paper, the image sensor which can detect the near IR range is successfully integrated with the image sensor for the visible range detection using the conventional Si CMOS process. Though the basic idea of this structure was already patented[4], we combined it with the most advanced active pixel technology with on-chip color filter and it was realized practically on Si wafer for the first time. From this sensor which is called VIPS(Vertically Integrated Photodiode Structure), it is observed that the information about the visible range and IR range can be obtained simultaneously within a frame separately.

II. Design and Fabrication of the Sensor

As shown in Figure 1, the maximum wavelength that can be detected by Si CMOS type image sensor is about 1.1μm(λ_c cutoff wavelength) which corresponds to the band gap energy of Si. The absorption coefficient from 1.1μm to 1.5μm is almost zero. The absorption in the region longer than 1.5μm is well explained in the literature[5]. Also, considering the black body radiation of this λ_c, it will determine the temperature of the heated object that can be measured by Si CMOS image sensor. From the Figure 1, the minimum temperature is around 600K. To detect and differentiate the signal of the longer wavelength, the depth of the photodiode for IR signal should be deeper and wider than the normal photodiode. Figure 2 shows the schematic cross-section of VIPS. Compared to the normal image sensors, the pixel for the IR detection is added and the photo diode is located under the normal pixels. And the color filters for the R, G, B selection can be used as the normal color image sensors because the IR light can penetrate these filters. Because of this array type, the resolution of IR image will be a quarter of visible image. The depth and the width of the photo diode determine the spectrum range of detection. To measure the longer wavelength, the deeper and the wider photo diode should be implemented. But there is a limitation of the ion implantation with the Si CMOS process. Therefore the trade-off between the detectible range of light and the process compatibility should be considered carefully. In conventional Si CMOS process, the maximum projected range by the high energy ion implantation is about 2~3μm. Because the depth of normal photo diode is about 0.5μm, two different photodiodes can be integrated vertically and well isolated each other. In Figure 3, there is a pixel layout that we have fabricated. For normal area sensors, the Bayer pattern was used for a color filter formation. Already mentioned earlier, the IR pixel is located among the four normal pixels. And this IR pixel also have the TG(Transfer Gate) signal and the RG(Reset Gate) signal as same as the normal pixel. And the symmetry is maintained with the normal pixel array. In this paper, we have used the 4-transistor type normal image sensors which consists of TG, RG, SG(Source follower Gate), Sx(Source follower selection switch). Based on the pixel architecture and the array, the full chip was fabricated as in Figure 4. The total effective array number of active pixel is

640×480 for VGA operation. Each pixel size is 7.5μm ×7.5μm. The left vertical driver is for the operation of the vertical line of normal pixel array and the right vertical driver is for the IR pixel array. The operation of each vertical scanner can be selected by applying the synchronous signal separately and it will operate as a switch between IR image and visible image. The horizontal scanner is shared between two types operation. The output data from the each pixel is converted to the 10bit digitized data through the columnar ADC. The left and right vertical scanner should not operate at the same time, because the vertical signals are connected to each other to reduce the area consumption. In Figure 5, simplified circuit diagram of full chip is shown.

To fabricate VIPS, 0.25μm Si CMOS standard technology with 1 poly and 3 metal was used. In this technology, the operation voltage is 5.0V, 3.3V for IO. And 0.25μm design rule was applied to the pixel design. For the logic design, 0.5μm design rule was used. In Figure 6, the process flow is summarized. Compared to the conventional CMOS process, deep NW(NWell) process is just added to form the deep photo diode for IR range. This deep NW is implanted with phosphorous ion as high as the energy of 3MeV. In Figure 7, the simulation result of the potential profile in the photo diode is shown. The peak of the normal photo diode is near the 0.4μm and the peak of the deep NW is located about 2.7μm depth and the depletion region is reached to the 4μm almost. After the ion implantation of photodiode, TG, RG ion implantation was followed to adjust the threshold voltage of transfer transistor and reset transistor. Then the remaining processes – gate patterning, source/drain formation, silicidation, contact formation and the 3 metal process are similar to the standard CMOS process. For the color area image sensor, the color filter process to make the R, G, B pattern was done on the metal 3 layer. Figure 8 is the photograph of the packaged chip after fabrication.

III. Results

The doping profile was investigated by SIMS as shown in Figure 9. Boron doping concentration on the surface area is about 6×10^{18} cm^{-3}, it was formed to prevent the injection of the defect from the surface dangling bond. And the background Boron doping concentration is about $2\times10^{15}cm^{-3}$. In case of Phosphorous doping profile, there are two peaks. The peak at the left side is for the visible range photodiode and the peak in the right side was formed from the process of deep NW with high energy ion implantation. Considering the background doping concentration of Boron and the peak doping concentration of Phosphorous, it can be confirmed that the double photo diode is well established. To take the image from this chip, the test board was configured as in Figure 10. In Table 1, the characteristics of R, G, B pixels of VIPS image sensor was summarized. The responsivity can be enhanced by the optimization of the floating diffusion area. The thermography characteristic was investigated as shown in Figure 11 with the variation of the target temperature. The IR pixel signal that was taken at 823K shows bright image of the hot zone from the hot plate in Figure 11(b). Because the thermal radiation can not penetrate the IR-cut filter, there is a dark area at the bottom of the image. As the temperature of the target is decreased, the signal becomes weak. And below 670K, it is not easy to detect the output signal as in Figure 11(c). It can be said that the temperature detection limit of the sensor is about 623K which is expected from Figure 1. Also, R, G, B pixels can detect the thermal radiation with lower thermal responsivity than that of IR pixels.

In Figure 12, there are three images which were captured without IR cut filter at three different modes - RGB only, IR only, and composite mode. In RGB mode, the thermal radiation(~773K) of the hot plate is not yet shown. But in IR mode, there is a bright white region on the hot plate as in Figure 12(b). Also, this hot zone is appeared in the composite mode image with the mixed RGB and IR signals of Figure 12(c). In this image, the R, G, B, IR signal can be modified by using the 3×4 color correction matrix. Also, if the images of Figure 12(a) and (b) are processed, it is possible to recognize the object along the different IR absorptivity.

IV. Conclusion

The Silicon CMOS image sensor having vertically integrated photodiode structure was successfully fabricated for the first time using the standard 0.25μm CMOS technology and it was observed that this sensor can differentiate the IR signal from the visible signal. Using this sensor, the thermography characteristic was investigated and the detectible limit was measured.

REFERENCES

[1] B. J. Hosticka, et al., "CMOS Imaging for Automotive Application," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 173-183, Jan. 2003.

[2] D. L. Gilblom, S. K. Yoo, "Infrared and ultraviolet imaging with a CMOS sensor having layered photodiodes," *SPIE/ISA Electronic Imaging*, Jan. 2004.

[3] R. Lyon, P. Hubel, "Eyeing the Camera: Into the Next Century", *IS&T/TSID 10th Color Imaging Conf., Proc.,* pp. 349-355, 2002.

[4] W. N. Carr, "Multi-Spectrum Photodiode Devices," US patent, 4,238,760, Dec. 9, 1980.

[5] W. Spitzer and H. Y. Fan, "Infrared Absorption in n-Type Silicon," *Physical Review*, vol. 108, no.2, pp.268-271, Oct. 1957.

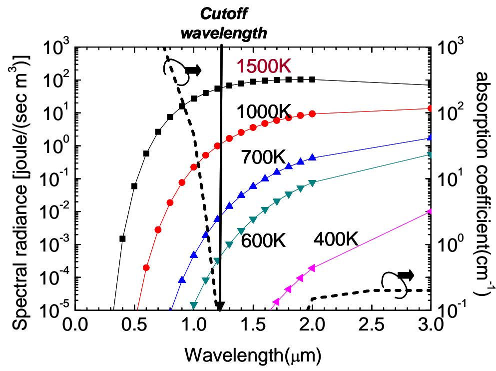


Fig. 1. Calculated Spectral radiance and absorption coefficient from the literature[4] along the wavelength.

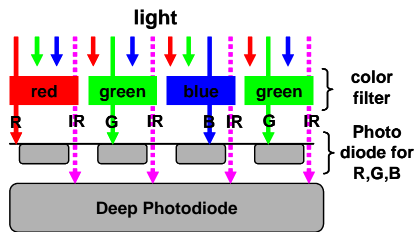


Fig. 2. Schematic cross-section of VIPS and the range of visible wavelength.

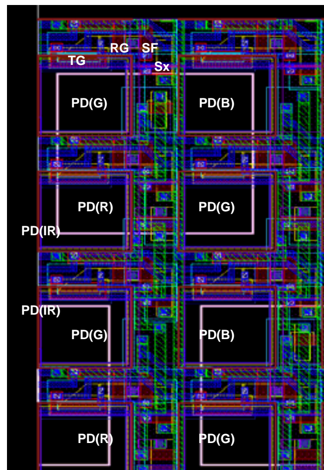


Fig. 3. Layout of pixel array.

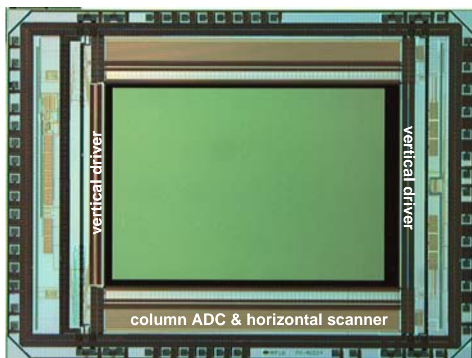


Fig. 4. Microphotograph of VIPS image sensor.

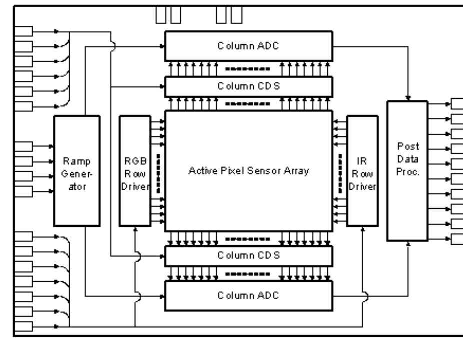


Fig. 5. Schematic circuit diagram of the area image sensor.

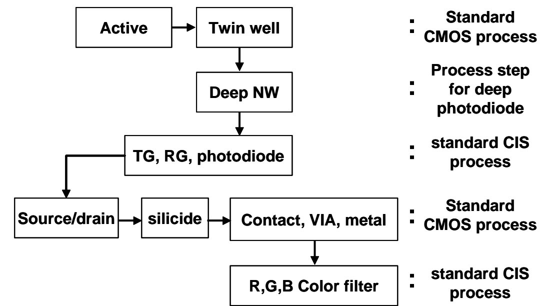
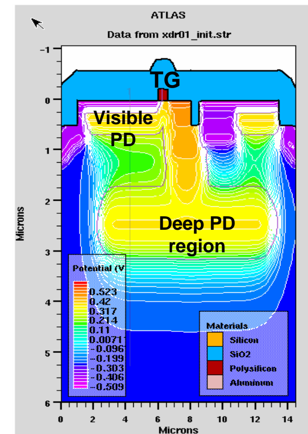


Fig. 6. Summarized process flow.



(a) 2-dimensional potential profile

Fig. 7. Simulated vertical potential profile of the pixel architecture.

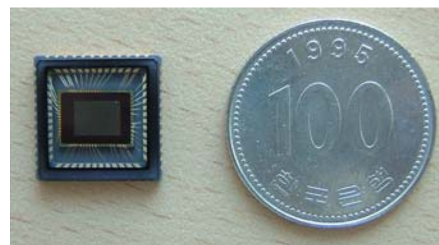


Fig. 8. Packaged chip photograph compared to Korean coin.

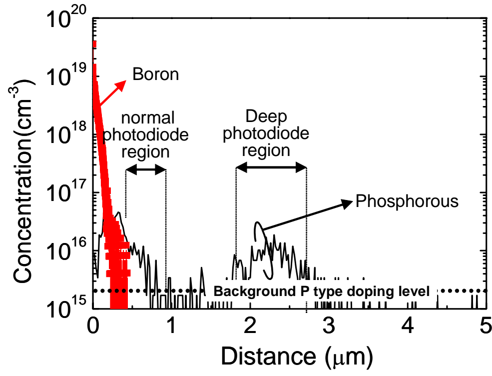


Fig. 9. Doping profile of Boron and Phosphorous in the photo diode region.

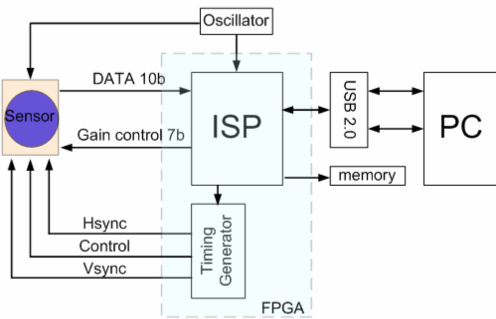
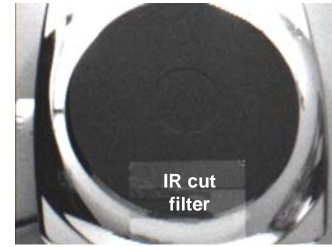


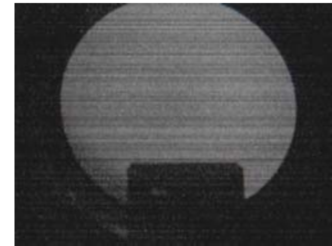
Fig. 10. Simplified schematic of the image test board.

Table. 1. Specification and characteristics of VIPS.

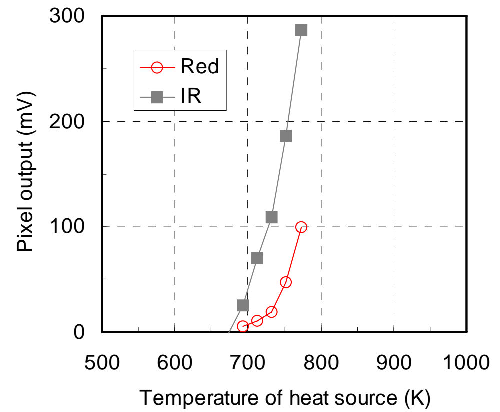
Process technology	0.25μm, 1P3M, CMOS
Optical format	1/3 inch
Pixel size	7.5μm × 7.5μm
Effective pixel array	640 × 480
saturation	1400mV
Responsivity	2.4V/lux·sec
Dark current	< 10mV/sec @ 20°C



(a) Image of hot plate at 300K



(b) Image of hot plate at 823K under zero lux



(c) Thermal responsivity

Fig. 11. Thermograph of hot plate and the thermal responsivity.

(a) normal RGB mode image

(b) IR mode image

(c) RGB + IR composite image

Fig. 12. Captured images with high temperature(773K) hot plate in RGB, IR, and composite mode without IR cut filter.

Gr Gb difference in 3M CMOS Image Sensor with 1.75µm pixel

Samsung Electronics Co., LTD., Nongseo-Dong, Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea 446-711
Bumsuk Kim, Yoonho Jang, Jongjin Lee, Kyoungsik Moon, Eun-Gyu Lee, Alexander Getman, JungChak Ahn, and YongHee Lee.

Keywords: CMOS image sensor, Gr Gb difference, Bayer pattern, Maze-like noise, 4-shared structure, 2-shared structure

Abstract

For CMOS image sensors with smaller pixel size, the pixel structure in which several pixels share floating diffusion or transistors tends to be adopted to enhance photodiode capacity and sensitivity. We have observed that in spite of aforementioned benefits, application of this structure may result in sensitivity difference between the shared pixels when light is obliquely incident. On captured images it appears as a difference between Gr and Gb channels. In this paper we compare structures of initial and improved 2.25um pixels. And the new sensor with 1.75um pixel size is compared. The improved 1.75um pixel was designed much more symmetrically than the 2.25um pixel due to advantage of 90nm Cu process. Gr Gb difference according to microlens shift and sensor factors (relative sensitivity at oblique incidence) were measured and compared for both sensors with 2.25um and 1.75um pixel sizes. It was proved that tolerance of Gr Gb difference to microlens shifts was greatly improved and that sensor factor of 1.75um pixel is superior to that of 2.25um.

I. Introduction

Typical color filter array which is used for CMOS image sensor (hereafter CIS) is Bayer pattern, which consists of Red, Blue, and two Greens (Fig. 1a). Therefore green pixels are able to show more information than red and blue pixels. But as pixel size gets smaller, problems such as low sensitivity and small photodiode capacity become more and more serious. Smaller photodiode capacity causes larger shot noise, and lower sensitivity increases integration time to gather same amount of electrons. All of these lead to degradation of signal to noise ratio. Therefore most recent pixels in CIS tend to adopt shared structure to achieve larger photodiode capacity and sensitivity [1]. If several transistors and active area are shared, geometry and structure of sharing pixels are inevitably asymmetric. All these things related with smaller pixel size can lead to signal difference between sharing pixels. If the signals of Gr and Gb pixels are different from each other, a kind of noise is induced. After an advanced color interpolation is applied, the Gr Gb difference can be seen to be a spatial noise which looks like maze.(Fig. 1b) Gr Gb difference is usually defined as (Gr-Gb)/<G> where <G> is average of Gr and Gb. The maze-like spatial noise is well seen when Gr Gb difference is larger than 3% from experience.(Fig. 2) It is desirable to remove the difference by optimized design of pixels without any help of digital compensation block.

II. Gr Gb difference of 2.25µm pixel

2.25µm pixel was developed using 0.13µm copper process. It adopted 4-shared structure which maximizes area of photodiode [2]. Four pixels share one floating diffusion and transistors such as reset and source follower. While the array of sharing pixels is 1x4, the structures of pixels in even and odd rows are different from each other just like 1x2 2-shared structure. But large Gr Gb difference was observed especially at oblique incidence of light. Finally metals were adjusted such that the Gr Gb difference at oblique incidence could be removed only by controlling microlens shift.

Fig. 3(a) shows the initial structure of 2.25µm pixel. Photodiodes are arranged asymmetrically due to the shared pixel structure. Photodiodes in even rows are moved upward from center of pixel, and those in odd rows downward. Electron may be generated outside of depletion region in odd rows, such that sensitivity could be lowered. They

might contribute to crosstalk between pixels. If sensitivities of even and odd rows are different from each other when light is incident obliquely, Gr Gb difference and color tint will occur which were already shown in Fig. 1. In order to solve this problem the pixel structure was re-designed so as to be able to cancel out the Gr Gb difference due to the asymmetry. Metal shields were adjusted like Fig. 3(b). In this structure sensitivity difference between even and odd rows can be successfully removed only by optimizing microlens shift. It was confirmed that modified metal shields play a role of reducing the sensitivity difference between even and odd rows. Fig. 4 and 5 show the experimental result of Gr Gb difference according to microlens shift.

III. Gr Gb difference of 1.75μm pixel

1.75μm pixel was developed and designed using advanced 90nm Copper process. Both high fill factor as much as 46% and good symmetry could be achieved even though the pixel adopted 2-shared structure. Therefore metal apertures are much more symmetric than those of 2.25μm pixel. Moreover pixel height was greatly reduced by using only two metal layers, which contributed to the improvement of tolerance to microlens shift and sensitivity at oblique incidence.

Gr Gb differences were measured according to microlens shift using 1/4inch 3M CIS with 1.75μm pixels. As a result, it is shown in Fig. 6 and Fig. 7 that the Gr Gb difference is much more insensitive to micolens shift compared with 2.25μm pixel.

The sensor factors of 1.75μm and 2.25μm pixels are compared in Fig. 8. Sensor factor is defined to be shading factor of pixel itself. Therefore it excludes shading of camera lens, and it is usually normalized at normal incidence. The sensor factors were measured using the camera lens of which the relative illumination and the angle of incidence according to image height are well known. The comparison in Fig. 8 shows that the sensor factor of 1.75μm pixel is superior to that of 2.25μm due to the much lower pixel height in spite of larger pixel size.

IV. Conclusion

2.25μm pixel was developed using 0.13μm copper process, and it adopted 1x4 4-shared structure. Gr Gb difference was observed in the initial pixel structure at oblique incidence. But metal shields were adjusted to remove Gr Gb difference only by optimizing microlens shift. Gr Gb difference can be removed without help of digital logic.

1.75μm pixel was designed using the advanced 90nm Cu process. Though 1x2 2-shared structure was adopted, the fill factor as much as 46% could be achieved while the photodiodes and metal shields of even and odd rows are much more symmetric than those of 2.25μm. Since the pixel height was lowered by reducing number of metal layers, the sensor factor of 1.75μm is superior to that of 2.25μm in spite of smaller pixel size. Gr Gb difference was proved to be much more insensitive to microlens shift compared with 2.25μm.

References

[1] M. Mori, et al., "A 1/4 inch 2M Pixel CMOS Image Sensor with 1.75 Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2004.

[2] Young Chan Kim, et al., "1/2-inch 7.2MPixel CMOS Image Sensor with 2.25μm Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation", 2006 IEEE International Solid-State Circuits Conference, pp. 1994-2003, Feb., 2006.

Figures

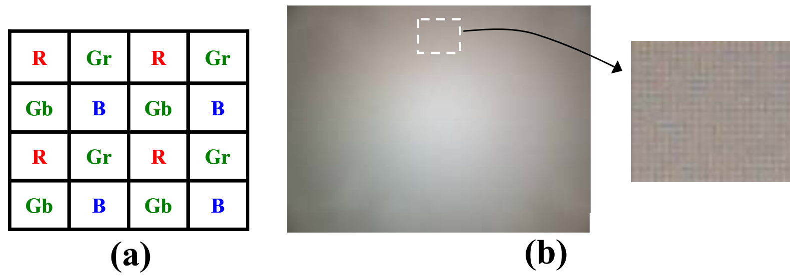


Figure1. (a) Bayer color filter pattern (b) Example of maze-like noise.

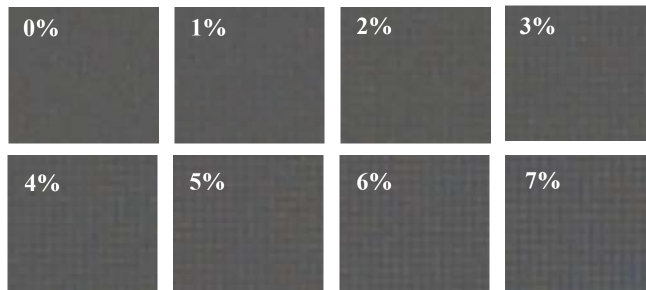


Figure2. Spatial noise according to Gr Gb difference.

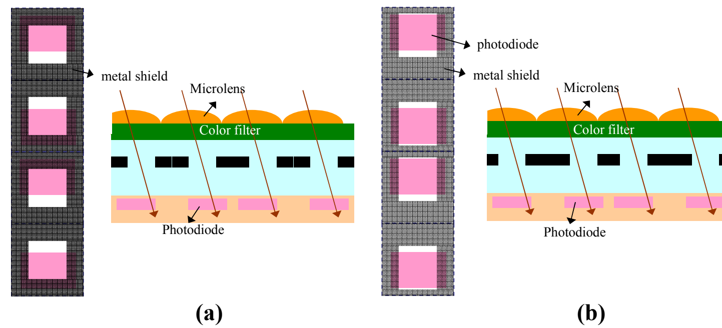


Figure3. (a) Initial structure of 2.25μm pixel (b) Modified structure to remove Gr Gb difference only by optimizing microlens shift.

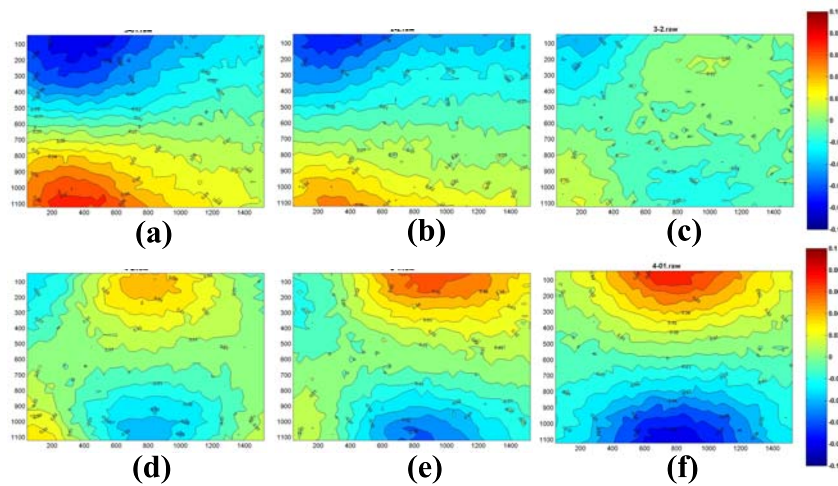


Figure4. Contour of Gr Gb difference of 2.25μm pixel according to microlens shift.

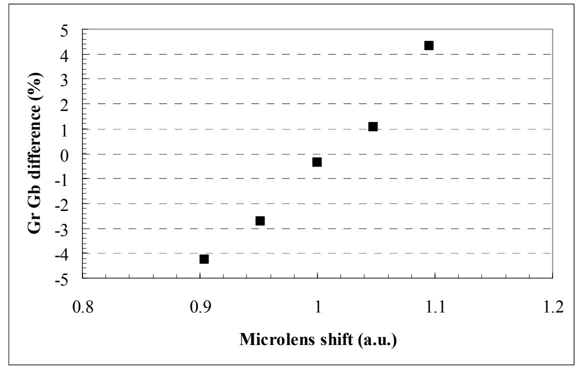


Figure5. Gr Gb difference of 2.25μm pixel according to microlens shift

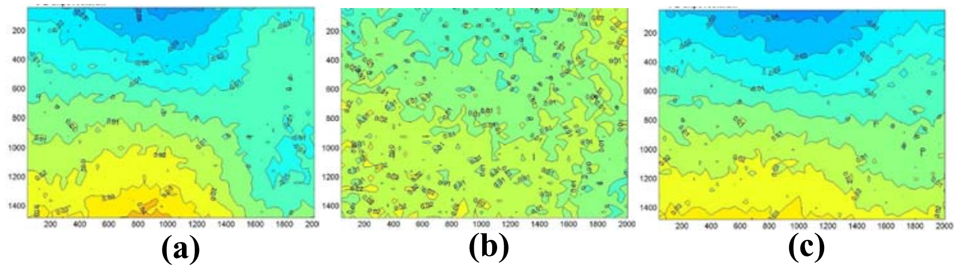


Figure6. Contour of Gr Gb difference of 1.75μm pixel.

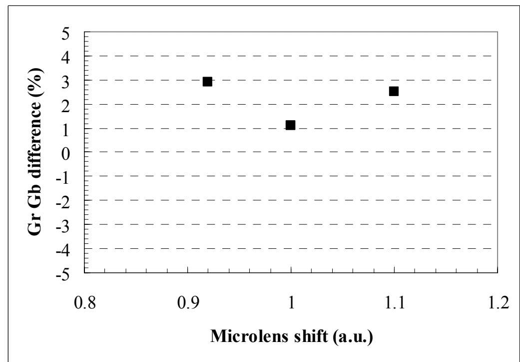


Figure7. Gr Gb difference of 1.75μm pixel according to microlens shift.

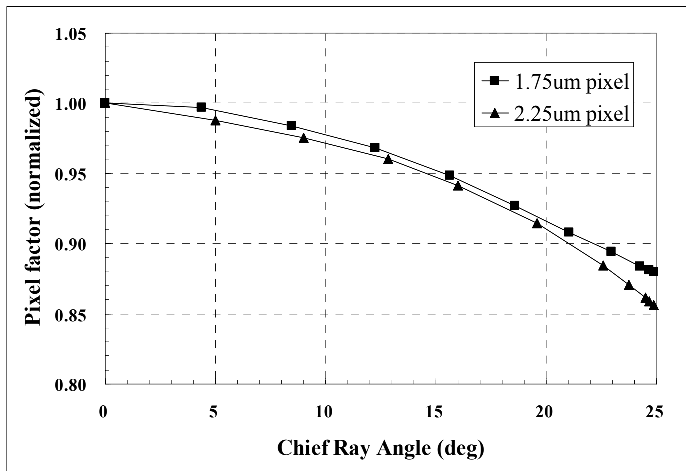


Figure8. Comparison of sensor factors between 2.25μm and 1.75μm pixels.

CMOS Color Image Sensor Overlaid with Organic Photoelectric Conversion Layers : Depression of Dark Current

Shunji Takada*, Masayuki Hayashi, Tetsuro Mitsui, Yoshiki Maehara, Mikio Ihama
FUJIFILM Corporation, Research & Development Management Headquarters,
577, Ushijima, Kaisei-machi, Ashigarakami-gun, Kanagawa, 258-8577, Japan

ABSTRACT

We have proposed the new CMOS color image sensor overlaid with organic photoelectric conversion layers in order to overcome the problems in sensitivity, moiré and color shading, which current CCD and CMOS image sensors have been facing with. Although the proposed image sensor and an organic solar cell depend on the photoelectric conversion by organic layers in common, the former distinctly differs from the latter in that the dark current should be markedly reduced to be as small as that in a silicon photodiode. Confirming the fact that the charge carriers of the dark current were predominantly injected from electrodes by applied field, we examined the effect of injected charge blocking layers upon the dark current in the proposed sensor and the quality of the pictures, which were taken by it and would be shown during this presentation.

INTRODUCTION

Both CCD and CMOS are the current image sensors predominantly used for digital imaging and continuously making progresses. They are principally the same in the method for color separation and the structure of photodiodes. While visible light is divided into the regions of three primary colors (i.e., blue, green, and red), each pixel is regularly arrayed on a plane and has a built-in color filter, which transmits and allows incident light in the region of one of the three primary colors to reach a photodiode for photoelectric conversion. This should be a principal reason for their deficiency in image-capturing ability, since incident light is uselessly absorbed in the regions of the other two primary colors by a filter in each pixel. In addition, they are facing with such problems as the color moiré caused by regularly arrayed color filters, the color-shading caused by inclined light incident to a color filter and a diode, which are apart from each other in a pixel, the decrease in the number of incident photons captured by a pixel and therefore the decrease in sensitivity with decreasing the size of a pixel.

In order to overcome these problems, we have proposed a multiply layered image sensor having a CMOS read-out circuit overlaid with three photoconductive layers, as illustrated in Fig. 1[1-2]. In this sensor, each of three photoconductive layers absorbs incident light in the region of one of the three primary colors, and transmits incident light in the regions of the other two primary colors, making it possible for each pixel to capture incident light in all the visible region for image formation. In addition, the proposed image sensor has several important advantages over current image sensors including large fraction in a pixel area available for capturing incident light owing to the

*shunji_takada@fujifilm.co.jp; phone 81-465-86-1161; fax 81-465-86-1014

structure with photoconductive layers on a read-out circuit, absence of color moiré owing to the structure without any color filter in each pixel, reduction of color-shading by causing the color separation and photoelectric conversion at the same place in each pixel. Although the proposed image sensor and an organic solar cell depend on the photoelectric conversion by organic photoconductive layers in common, the former distinctly differs from the latter in that the organic photoconductive layers in the former need sharp absorption spectra for color separation, rapid operation, and reduced dark current, which should be as small as that in a silicon photodiode. Usually, the dark current is enhanced by the increase in bias voltage, which is applied for the enhancement of the photoelectric conversion efficiency, and is therefore an important problem to be solved for the realization of the proposed image sensor.

In order to depress the dark current, we studied it in the proposed image sensor, in which bias voltage was applied to organic photoconductive layers. It was judged from the analysis of the current-voltage characteristics that the dark current predominantly arose from injected charges from electrodes to organic photoconductors. Then, we tried to depress the dark current by putting injected charge blocking layers between an electrode and a photoconductive layer, as illustrated in Fig.2. Furthermore, we produced a trial product of the proposed image sensor with a CMOS read-out circuit overlaid with a photoconductive layer, in which the dark current was depressed according to the result obtained in this study.

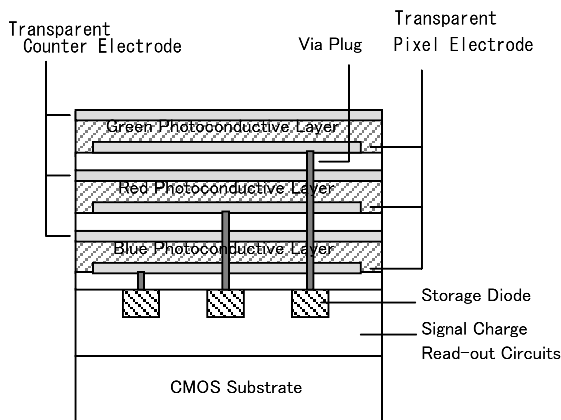


Fig. 1 Structure of image sensor with organic photoconductive layers.

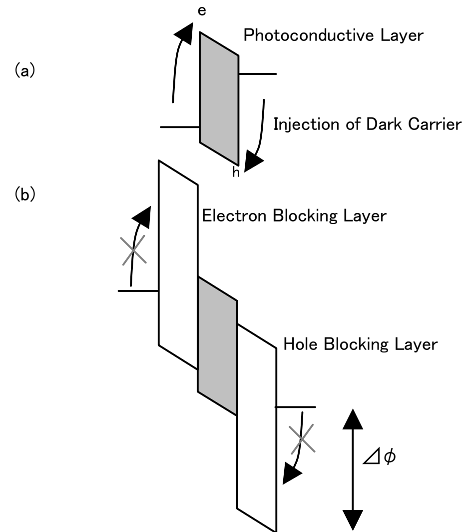


Fig. 2 Schematic energy diagram of photoconductive layers (a) without blocking layers, and (b) with blocking layers.

EXPERIMENTS

In order to study the dark current in the proposed sensor in the presence of applied voltage, a device was prepared by depositing one after another on an ITO electrode with a glass substrate an organic layer with variation of ionization potential (Ip) for hole-blocking, a photoconductive layer composed of quinacridone, and an Al electrode by means of high-vacuum thermal evaporation method. Then, the dark current was given by the current-voltage characteristics of the device in the presence of positive bias voltage to the ITO electrode.

In order to evaluate a picture taken by the proposed image sensor on the basis of the result of the above-stated experiment, a device was prepared by depositing a quinacridone sandwiched between injected charge blocking layers,

which were the best in performance by high-vacuum thermal evaporation method, and an ITO counter electrode by sputtering on an ITO pixel electrode installed on a CMOS read-out circuit. The devices thus prepared were sealed. All the above-stated processes were carried out without breaking vacuum. Since each pixel in this CMOS sensor has a quinacridone layer on a silicon diode, this sensor is sensitive to two color regions (Fig. 3). Namely, incident light is absorbed in green region by a quinacridone layer for photoelectric conversion, while incident light is transmitted in blue and red regions by a quinacridone layer for the absorption and photoelectric conversion by a silicon photodiode. Incident light is captured separately in blue and red regions by a photodiode through color filters transmitting light in blue and red regions, respectively. Then, a full color image was constructed by the images, which were separately captured in blue, green, and red regions according to the above-stated procedures.

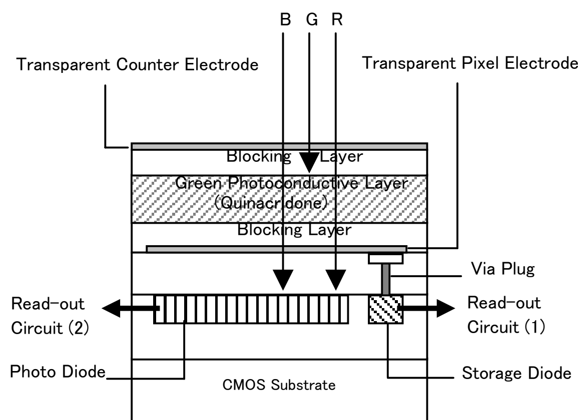


Fig. 3 Structure of trial product of CMOS image sensor with overlaid organic layer.

RESULTS and DISCUSSIONS

Fig. 4 shows the relationship between Ip of a hole-blocking material and the resultant dark current, indicating the tendency that the increase in the former results in the decrease in the latter. The hole-blocking layer with the largest Ip among those examined could decrease the dark current by as large as five orders of magnitudes. This result seems to indicate that a hole-blocking layer could depress the dark current by increasing the barrier height for the positive hole injection ($\Delta\phi$; the difference between the work function of an ITO electrode and the Ip value of an organic layer in contact with the ITO electrode) . It is however noted that the dependence of the dark current on $\Delta\phi$ is too small to explain the observed dark current according to the scheme shown in Fig. 2. In addition, the observed dark current differs considerably among the hole-blocking materials with similar $\Delta\phi$ values. It is therefore considered that the hole-blocking ability depends, not only on Ip, but also on intermediate levels in a hole-blocking layer.

Fig. 5 shows the picture taken by the proposed CMOS image sensor having a green-sensitive photoconductive layer composed of quinacridone in contact with the best blocking layers. The obtained picture was fairly good, indicating that the green image, which was captured by an organic photoconductive layer, was comparable to the blue and red images captured by a silicon photodiode in the ratio of the number of signal charge carriers to that of dark charge carriers.

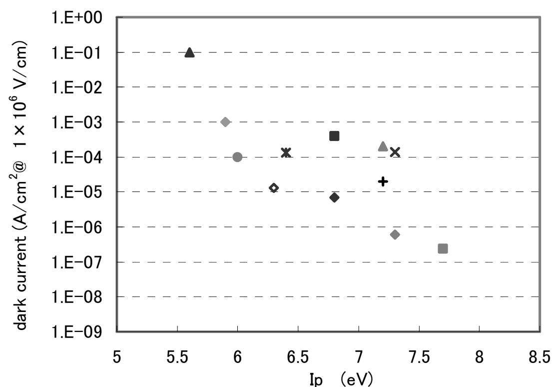


Fig. 4 Dependence of dark current on Ip under voltage biasing condition.

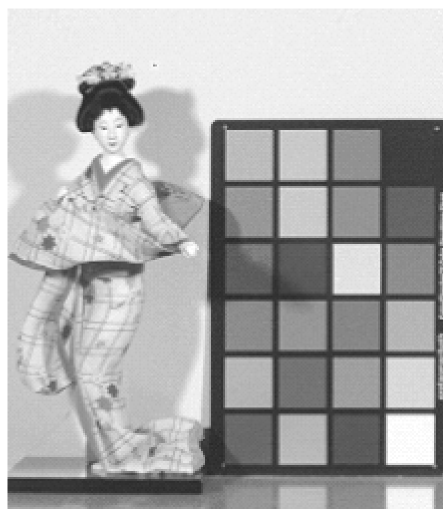


Fig. 5 Color picture taken by trial product.

CONCLUSION

The dark current in an organic photoconductive layer in the presence of applied electric field could be markedly depressed by introducing injected charge blocking layers between electrodes and the photoconductive layer. The introduction of the best blocking layers into the proposed CMOS image sensor overlaid with an organic photoconductive layer made it possible to take fairly good color pictures.

ACKNOWLEDGEMENTS

The present authors thank Prof. Shoji Kawahito of Shizuoka University and Prof. Takahiro Saito of Kanagawa University for their collaboration in designing the CMOS circuit and in simulating the optimized spectral sensitivity of proposed image sensor, respectively.

REFERENCES

1. Shunji Takada, Mikio Ihama, and Masafuni Inuiya, “CMOS Image Sensor with Organic Photoconductive Layer Having Narrow Absorption Band and Proposal of Stacked Type Solid-State Image Sensors”, IS&T/SPIE’s Electronic Imaging 2006 San Jose, CA.
2. Shunji Takada, Mikio Ihama, Masafuni Inuiya, Takashi Komatsu and Takahiro Saito, “CMOS Color Image Sensor with Overlaid Organic Photoconductive Layers Having Narrow Absorption Band”, IS&T/SPIE’s Electronic Imaging 2007 San Jose, CA.

A Buried Triple-Junction Self-Reset Pixel in a 0.35µm High Voltage CMOS Process

Thomas D. Ross, Robert K. Henderson, Bruce Rae, David Renshaw
Institute of Micro and Nano Systems, University of Edinburgh, Edinburgh EH9 3JL
Tel +44 131 650 5568, Fax: +44 131 650 6554, E-mail: Robert.Henderson@ed.ac.uk

ABSTRACT – Light to frequency converters are used to sense the photocurrents of a buried triple-junction pixel achieving high dynamic range and low dark current colour sensing without the use of colour filters. The pixel is realised in a high voltage 0.35µm CMOS enabling sample manipulation by electrowetting and spectral sensing for a FRET biosensor.

I. INTRODUCTION

Colour sensing without the need for surface optical filters has been achieved by using buried p-n junction structures in various CMOS processes [1-3]. In addition to reducing process costs, this increases overall photon collection efficiency and eliminates the colour aliasing introduced by conventional Bayer pattern sub-sampling [4-5]. BiCMOS processes provide several p-n junctions at different depths which can be employed to realise stacked triple-junction photodiodes [6]. In this paper, we present the use of a 0.35µm high voltage CMOS process for the realisation of such buried triple-junction (BTJ) photodiode structures (Fig. 1). High voltage handling and optical filterless colour sensing are required for electrowetting and spectral sensing for FRET-based biosensors [7-8]. The pixel itself employs light-to-frequency (L2F) techniques, and is presented in section II.

II. CIRCUIT OPERATION

BTJ sensors generally employ integrating mode photodiodes (Fig. 2) whereby the three junctions are reset to various potentials to keep the photodiodes reverse-biased. The diodes then integrate at different rates dependent on the spectral content of the light and their respective responsivities. Because the junctions are coupled, they will become forward biased if the signal in one spectral band is particularly high relative to the others, resulting in crosstalk between colour channels. Moreover, the stack of voltage levels uses up voltage headroom and requires careful management.

Self-resetting L2F converters are a popular means of realising very high dynamic range image sensors [9-11]. In the sensor proposed here, L2F converters are employed to sense the currents through each of the reverse-biased p-n junctions of the BTJ structure (Fig. 3). The virtual ground of the amplifiers allows the junction potentials to be held constant at arbitrary levels during operation. In this case, the charge amplifier bias voltage, V_{CM}, is chosen to be 1.6V; approximately half of the 3.3V supply. Thus, the blue and green junctions have zero potential across them, resulting in minimal dark current [12]. A 1V swing was chosen for the integrators, resulting in V_{CP}=2.6V (Fig. 4). The charge amplifier of the middle junction integrates in the opposite sense, and so the comparator has been inverted, and its voltage threshold set to V_{CN}=0.6V. The output frequencies of the top and bottom charge amplifiers are given by (1) and (3), while that at the output of the middle charge amplifier is given by (2), shown below:

$$f_b = \frac{I_{blue}}{2C_f(V_{CP} - V_{CM})} \qquad (1)$$

$$f_{bg} = \frac{I_{blue} + I_{green}}{2C_f(V_{CM} - V_{CN})} \qquad (2)$$

$$f_{gr} = \frac{I_{green} + I_{red}}{2C_f(V_{CP} - V_{CM})} \qquad (3)$$

Note that the L2F output frequencies represent the I_{blue}, $I_{blue}+I_{green}$, and $I_{green}+I_{red}$, respectively because of the summations of currents into the amplifier virtual earths. The frequencies are directly proportional to the photocurrents. 100fF poly-poly capacitors have been chosen as integrating

capacitors setting the sensitivity of the sensor. The high linearity of these capacitors assures a linear relationship between photocurrent and frequency.
The denominator terms in (1), (2) and (3) are designed to be identical by choosing matched integrating capacitance and $(V_{CP}-V_{CM})=(V_{CM}-V_{CN})$. This allows the contributions of the individual I_{blue}, I_{green} and I_{red} photocurrents to be dissociated by simple subtraction of the frequencies. A convenient hardware implementation is possible using up-down counters clocked by the output transitions of the blue/green or red/green L2F outputs.
An extremely high dynamic range is obtained (>150dB). Saturation does not occur regardless of the spectral content of the illumination leading to good colour detection over a very high dynamic range.
In Fig. 5, an L2F structure is proposed with improved full scale-range. A switched-capacitor feedback structure allows independent choice of the photodiode voltage level and the comparator threshold voltage. The full range of the power supply can thus be used (between V_{CN} and V_{CP}), maximising SNR and full-well capacity.

IV. MEASURED RESULTS

The chip micrograph is shown in Fig. 6. The die has had the polyimide passivation removed by oxygen plasma, providing around 3-5x increase in quantum efficiency in the 500nm range. Four different BTJ structures were implemented using the various junction depths available. Fig. 7 shows a typical set of outputs of the L2F converters. The spectral response curves of photocurrents corresponding to the n-diffusion, p-well, deep n-well BTJ structures are shown in Fig. 8. The sensor performance is summarized in Table. 1. Dark current of the blue and green diodes with 0V reverse bias is not measurable while the dark current of the red photodiode with 1.6V bias is $2nA/cm^2$. A dynamic range of >150dB with frequencies ranging from 1mHz to 5MHz is obtained.

V. CONCLUSION

Self-reset loop structures can be applied to buried triple junction photodiodes to provide high-dynamic range, filterless colour sensing. Low dark current with simple digital colour outputs are beneficial for biosensor applications.

REFERENCES

[1] Nozaki et al., "Color sensor," US patent 4,677,289, 1987.

[2] Gay et al., "Vertically integrated solid-state color imager," US patent 4,581,625, 1986.

[3] B. Chouikha et al., "Photodetector based on buried junctions and a corresponding method of manufacture," US patent 5,883,421, 1999.

[4] R.B. Merrill, "Color separation in an active pixel cell imaging array using a triple-well-structure," US patent 5,965,875, 1999.

[5] R. Lyon and P. Hubel, "Eyeing the camera: into the next century," 10th *Color Imaging Conference: Color Science and Engineering Systems, Technologies*, Applications, Scottsdale, Arizona, pp. 349-355, Nov. 2002.

[6] M. Ben Chouikha, G.N. Lu, M. Sedjil, and G. Sou1, "Colour detection using buried triple pn junction structure implemented in BiCMOS process," *Electronics Letters*, Vol. 34, No. 1, pp. 120-122, 1998.

[7] A R Mount et al., "The stability and characteristics of a DNA Holliday junction switch," *J. Biophys Chem.*, Vol. 124, pp.214-221, Dec. 2006.

[8] K. Current et al., "A high-voltage CMOS VLSI programmable fluidic processor chip," *Symposium on VLSI Circuits*, pp. 72-75, 2005.

[9] J. Rhee, Y. Joo, "Wide dynamic range CMOS image sensor with pixel level ADC," *Electronics Letters*, Vol. 39, No. 4, pp. 360-361, 2003.

[10]S. Kavusi, K. Ghosh and A. El Gamal, "Architectures for high dynamic range, high speed image sensor Readout Circuits," *IFIP VLSI-SoC*, Nice, Oct. 2006.

[11] G. de Graaf, R.F. Wolffenbuttel, "Optical CMOS sensor system for detection of light sources," *Sensors and Actuators A*, Vol. 110, pp. 77–81, 2004.

[12] L. Simpson et al., "An integrated CMOS microluminometer for low-level luminescence sensing in the bioluminescent bioreporter integrated circuit," *Sensors and Actuators B*, Vol. 72, pp. 134-140, 2001.

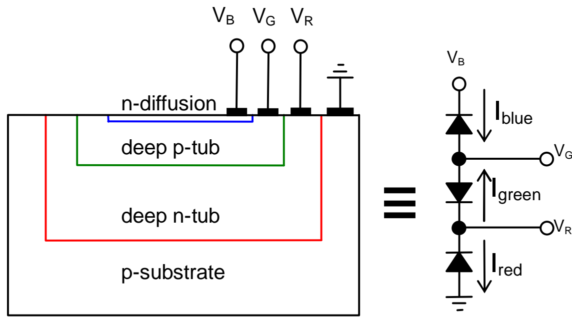


Fig. 1 Diagram of buried triple structure showing junctions and diodes

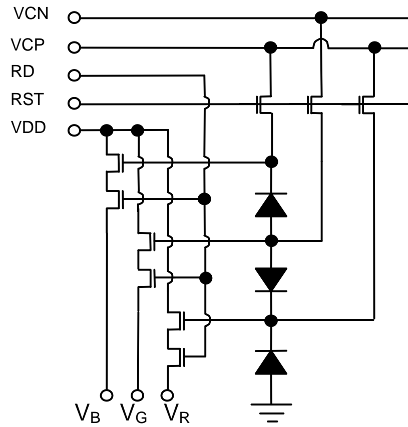


Fig. 2 BTJ source-follower readout

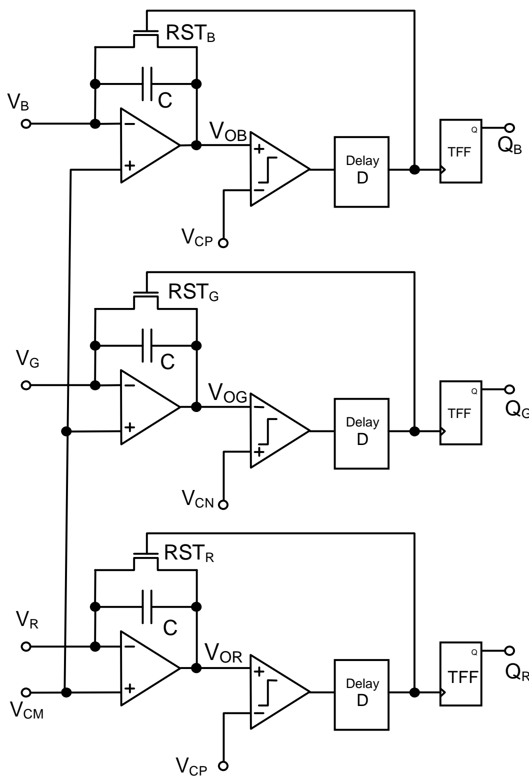


Fig. 3 BTJ readout using three L2F converters

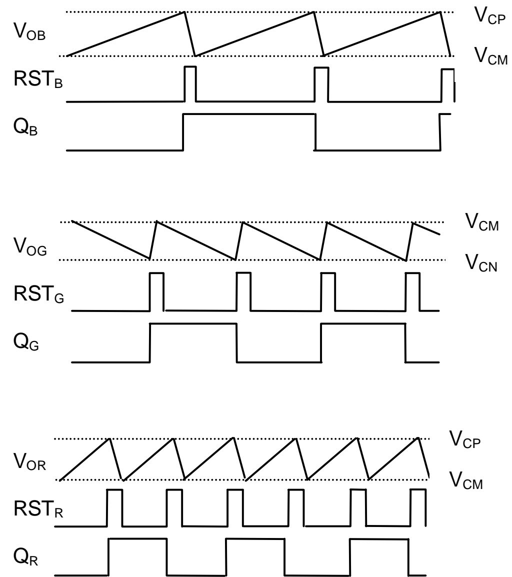


Fig. 4 Timing diagram showing the operation of the L2F readout

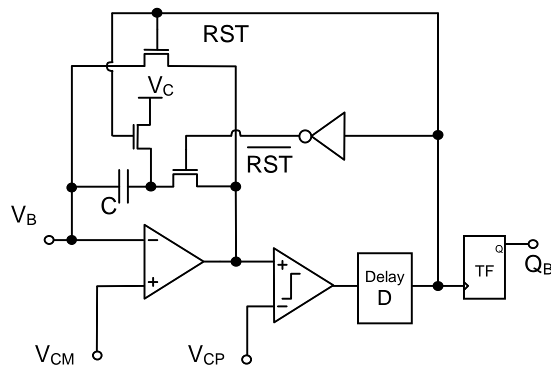


Fig. 5 L2F converter with optimised output swing

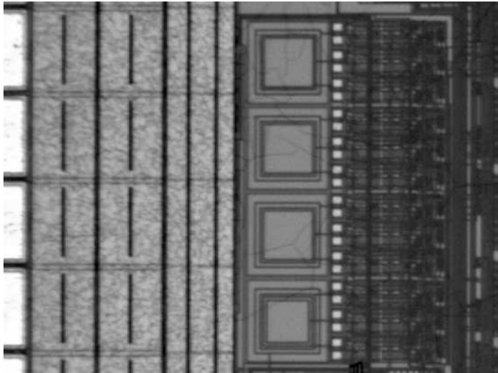


Fig. 6 Chip micrograph showing four 80µm x 80µm BTJ diode structures with L2F readouts

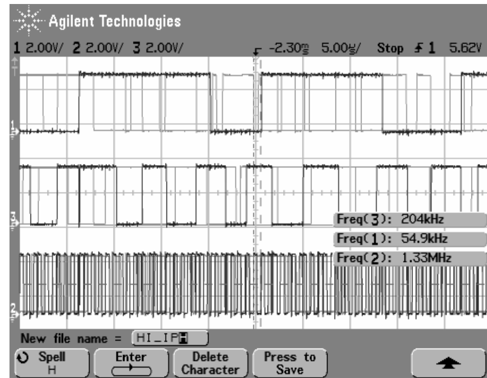


Fig. 7 Oscilloscope trace showing the three L2F outputs

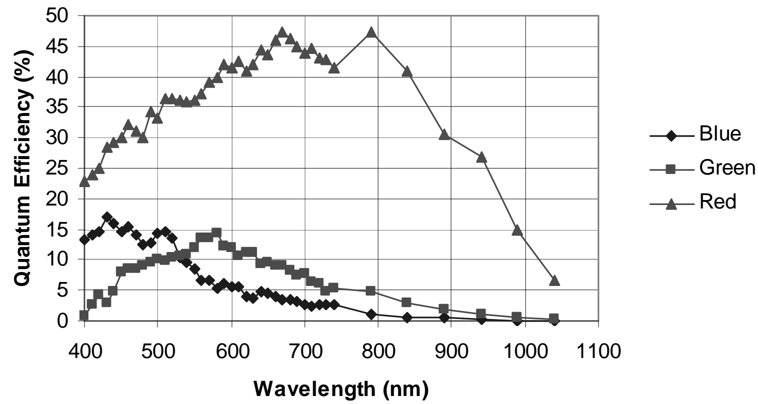


Fig. 8 Quantum efficiency versus wavelength for the three junctions

Parameter	Value	units
Process	0.35µm 50V 4LM 2P	CMOS
Dynamic Range	>150	dB
Dark current (red)	2	nA/cm^2
Dark current (blue, green)	Not observable	nA/cm^2
Capacitance	100 (poly-poly)	fF
Area	0.016	mm^2
Current consumption	500	µA
Supply voltage	3.3	V
Full well	625k	e^-
Maximum frequency	5	MHz

Table 1 BTJ Sensor Performance Summary

An SXGA CMOS image sensor with 8 Gbps LVDS serial link

T. Cools[(1)], P. Deruytere[(1)], J. De Bondt[(1)], R. Sankhe[(1)], T. Geurts[(1)], K. Takada[(2)], T. Yamamoto[(2)]

(1) Cypress Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
ftg@cypress.com, tel +32 15 446 395, fax +32 15 446 358
(2) NED, 2-5-12, Itachibori, Nishi-ku, Osaka 550-0012, Japan
k.takada@ned-sensor.com, tel + +81 6 6534 5300, fax + +81 6 6534 6080

This paper describes a highly integrated SXGA high speed, high sensitivity CMOS image sensor targeted at various industrial monitoring applications. Implemented in a 0.25 um CMOS process, the sensor runs at 500fps and features triggered and pipelined shutter modes. The sensor packs 24 parallel 10-bit A/D converters with an aggregate conversion rate of 740 MSPS. On-chip digital column FPN correction allows the sensor to output ready-to-use image data for all but the most demanding applications. In order to allow simple and reliable system integration, the 13 channel 8 Gbps LVDS serial link protocol supports per channel skew correction and serial link integrity monitoring. Peak responsivity of the 14x14um 6T pixel is 7350V/s/(W/m^2). Dynamic range is measured to be 57dB. In full frame video mode the sensor consumes 1.2W from a 2.5V power supply.

Introduction

LVDS is an emerging interface of choice on CMOS image sensors. Using LVDS camera developers can build compact camera heads by physically separating image capture and image processing. Recently, image sensors with on-chip LVDS serial links have been presented. In [1] a sensor is presented with a single LVDS channel interface. In [2] the authors describe a sensor with a 9-channel interface proving a 4Gbps link interface packed together with a low-resolution ADC. The sensor being presented combines more parallelism, higher ADC resolution and higher power efficiency than previously reported.

Image Sensor Design

The sensor (Figure 1) consists of an image core, 24 analog front-ends, a digital data processing block, an LVDS interface, timing control and registers. All bias currents and reference voltages are generated on-chip, a POR and a temperature monitor circuit are foreseen.

The pixel array contains 1280x1024 6T pixels (Figure 2) to display the recorded image (Figure 3) as well as a number of dummy rows and columns. Black columns are available for read-out and can be used to support off-chip black-level calibration accounting for most important shifts in black level due to PVT variations. An average black value can be derived from the black columns which can be used to set the ADC black reference through the register interface.

The pixel array data is sampled and stored in the columns and sequentially read out in 54 kernels for each line. Each kernel consists of 24 pixels and the analog data is multiplexed over 24 analog busses. In order to support intelligent subsampling in both B/W and RGB products, the columns are connected to the busses in a triangular shape rather than a more typical sawtooth (Figure 4). A beneficial side-effect is that any mismatches between the 24 busses and subsequent 24 analog processing channels due to IR-drop or other spatial differences –although already minimized by careful design and layout – get smoothed out into less visually disturbing patterns.

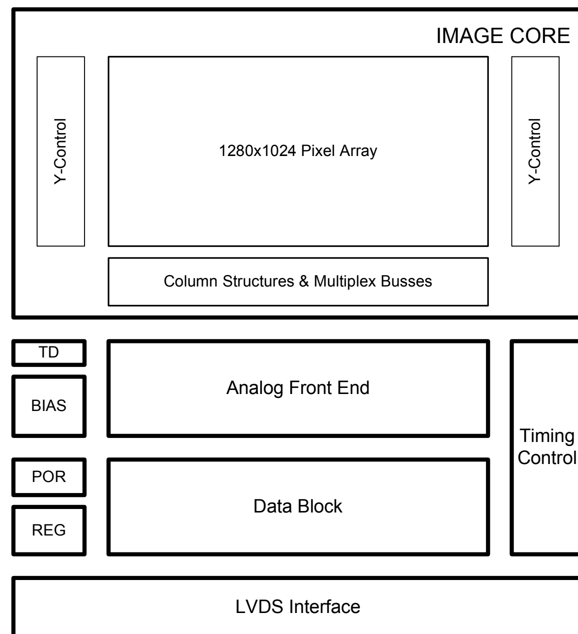


Figure 1: Block Diagram

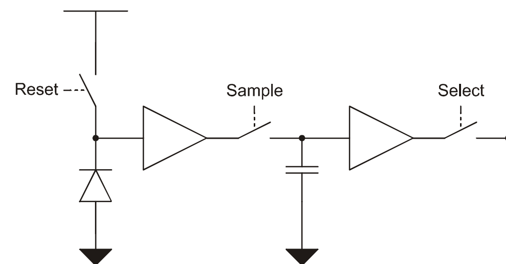


Figure 2: Pixel Architecture

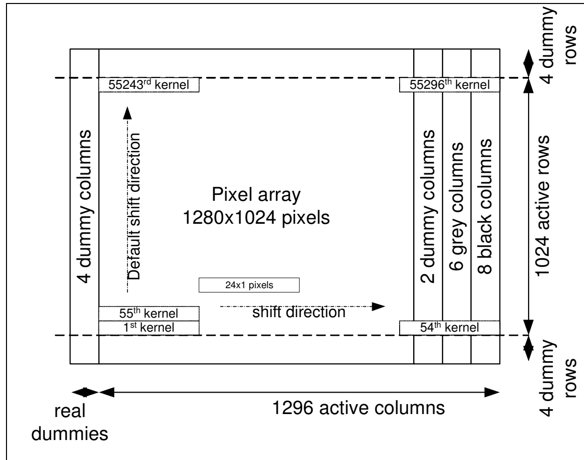


Figure 3: Frame Format

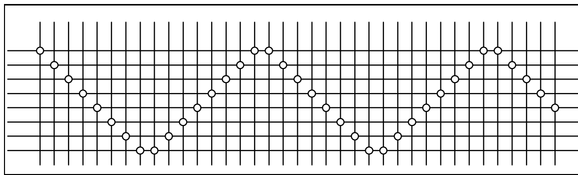


Figure 4: Multiplex bus connections

The analog front-end consists of a programmable gain amplifier and a low-power 10-bit pipelined ADC. Using commutated feedback switching [3], capacitor sizes are minimized and a power efficiency of 0.5pJ/bit is achieved. Implementing 24 ADCs in parallel introduces some interesting challenges in the layout. The ADCs are implemented as 24 slices of ADCs sharing common supply lines and reference voltages. 10 different pads connect to the ADC power supply and in order to further minimize IR-drop, up to 400um wide power busses are used with > 30nF of on-chip decoupling. The resulting dynamic IR-drop on the ADC power supply is limited to <5mV in the center of the die. Another challenge is presented by the reference voltages shared by the different ADCs. Any difference in reference voltage across the die results in a gradient in the image within each kernel. The ADC system has a low-bandwidth reference buffer and a large decoupling cap to average out spikes of current pulled by the 24 parallel blocks. If the average net current pulled from the cap is different for different codes, a sustained input at one level could disturb the AFE reference voltage before the amplifier kicks in to correct the voltage level. The reference voltage buffer was designed to ensure the difference in differential reference voltage due to a sustained black or white input level was < 0.5mV.

Column FPN calibration is implemented by applying a fixed voltage to all columns during frame blanking time. One line is then read out and the data is stored in an on-chip memory. For all subsequent lines, the stored value is subtracted from the pixel data. This way all FPN related to column circuit, PGA and ADC offsets is corrected.

Data from the 24 ADCs is multiplexed to 12 parallel data channels. The data block supports the communication protocol, and is capable of correcting column FPN. A 13th data channel is dedicated to sending frame and row synchronization as opposed to 8B/10B like encoding, where synchronization data is embedded in the data stream. This strategy is straightforward to implement, scales easily with word-size and has a particularly low overhead considering the parallelism. When the sensor is not transmitting image data, a training pattern is transmitted that allows the receiver to lock on to the data phase. During image transmission, CRC codes are inserted in the data stream during row blanking to allow monitoring link integrity. Also in the logic design, care has to be taken to avoid the parallelism and large distances to be travelled causing any problems. The number of critical signals travelling across the die at high speed must be minimized. Although it is feasible to transmit data across the 2 cm over which the channels are spread within a 65 MHz clock cycle, too many critical signals would blow-up the complexity of top-level timing closure. Therefore, most control signals from the sequencer have been daisy-chained from one data channel to the next and re-synchronized at each channel.

The LVDS interface accepts a 310 MHz input clock from which clocks and load signals are generated for the 13 transmit channels and for one replica channel used to transmit a DDR clock to the receiver, synchronized with the data stream, hence simplifying clock recovery and mitigating the risk of low frequency jitter affecting serial link integrity. The 620 Mbps LVDS transmitters are compliant with the TIA644 standard. The implemented interface allows the sensor to be controlled and read-out by a standard FPGA without the need for any separate buffers or deserializer ICs.

The on-chip logic has been implemented to support many different operating modes such as triggered and pipelined shutter, master and slave operation, multiple slope for wide dynamic range applications, subsampling in X&Y, random windowing in X&Y, multiple windowing (up to 4 independently programmable windows), by programming the register interface.

A high degree of testability is ensured by scan chains for the 300k gates of logic, allowing to meet a 99.5% coverage for the logic, a dual mixed signal boundary scan bus and several BIST features.

Experimental Results

Full characterization has been finalized and the product is ready to go into full production. The key sensor specifications are listed in Table 1;

Table 1: key specifications and measurements.

Parameter	Value	Remark
Pixel size	14 x 14 μm^2	
Pixel array	1280 x 1024	
Pixel type	NWell – 6T	
Interface	Serial LVDS	TIA644 compliant
Frame Rate	500fps	
Data Rate	8Gbps	
Main power supply	2.5 V	
Power Consumption	1.2 W	
Full well	30 ke^-	
kTC noise	28 e-	
Read noise	28 e^-	
Responsivity	7350V/s/(W/m^2)	
DR	57.6dB	Intra-scene
ADC resolution	10-bit	
LVDS jitter	50 ps_{RMS}	TIA644 compatible
Chip size	22.5x22.5mm^2	
Package	168 pins ceramic µPGA	

A receive-end eye diagram for one of the LVDS output channels is shown in Figure 5. Random jitter is less than 50 ps. The design efforts to minimize duty cycle distortion typically resulting from DDR operation are shown to be successful.

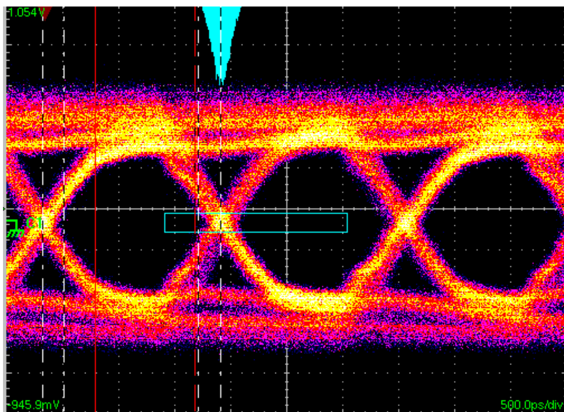


Figure 5: Receive-end eye diagram

Table 2 lists the sensor main spatial noise components. Without column FPN correction enabled, column FPN is as high as 13mV_{RMS}. Enabling column FPN correction yields a 1.8mV_{RMS} remaining column FPN. The temporal noise increases because the read-noise is added twice as expected from the applied methodology which shows the additional logic operations and memory-access do not significantly disturb the noise performance of the sensor.

Table 2: Spatial Noise

FPN	14 mV_{RMS}	
Column FPN	13 mV_{RMS}	1.8 mV_{RMS} with column FPN correction enabled
PRNU	< 1%	% of full scale
Dark Signal	170mV/s	@ 30C
DSNU	14 mV/s	@30C

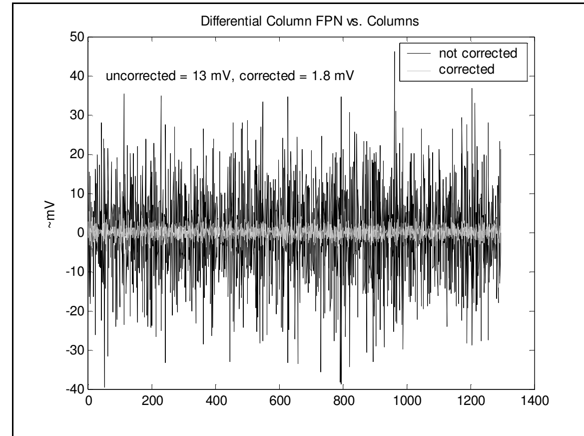


Figure 6: Column FPN with and w/o on-chip correction

An offline corrected image of a test chart is shown in Figure 7.

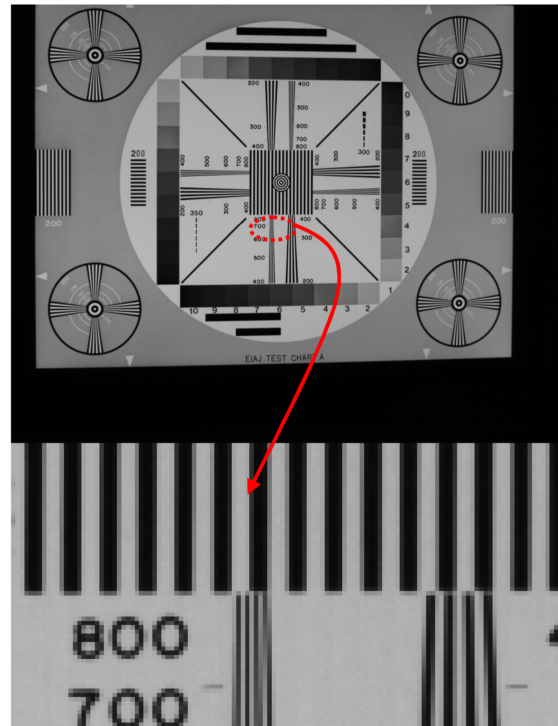


Figure 7: image from the sensor with off line FPN correction.

Conclusion

In this paper we presented a low-noise, high sensitivity SXGA image sensor for up to 500fps industrial imaging. The sensors integrates A/D conversion, on-chip timing for a wide range of operating modes and features an LVDS interface for easy system integration. By removing the visually highly disturbing column patterned noise, this sensor allows building a camera without having to perform any off-line correction or the need for any memory making this sensor highly suitable for lower-cost applications. Moreover, since the on-chip column FPN correction is more reliable than an off-line correction as it is intrinsically compensated for supply and temperature variations, this sensor also allows to build reliable high-end camera's without having to worry about column FPN appearing in environments with highly varying ambient temperatures.

References

[1]N. Bock, et al., "A Wide-VGA CMOS Images Senosr with Global Shutter and Extended Dynamic Range" *Proc. of IEEE Workshop on CCDs and AIS, Karuizawa,* pp. 222-225, 2005

[2]Alex Krymski, Kenji Tajima, "CMOS Image Sensor with Integrated 4Gb/s Camera Link Transmitter", *in ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2005*

[3] P.Yu and H. Lee, "A 2.5-V, 12-b, 5-MSample/s, pipelinedCMOSADC," *IEEE J. Solid-State Circuits, vol. 31, pp. 1854–1861, Dec. 1996*

A 600×600 Pixel, 500 fps CMOS Image Sensor with a 4.4μm Pinned Photodiode 5-Transistor Global Shutter Pixel

I. Takayanagi, Y. Mo*, H. Ando, K. Kawamura, N. Yoshimura, K. Kimura,
T. Otaka, S. Matsuo, T. Suzuki, F. Brady**, and J. Nakamura
Micron Japan, Ltd. 4-2-8 Shibaura, Minato-ku, Tokyo 108-0023, Japan
* Micron Technology, Inc. 251 South Lake Avenue, Suite 600, Pasadena, CA 91101-1101, USA
** Micron Technology, Inc. 8000 S. Federal Way, Boise, ID 83707-0006, USA
Contact: Isao Takayanagi: tel: +81-3-5439-3300, fax: +81-3-5439-3311, email: istakayanagi@micron.com

Abstract

To realize a low cost image sensor, while maintaining a 500 fps-class high frame rate, we have developed a prototype image sensor where a 600×600 imaging array with a 4.4μm global shutter pixel and multiple pipeline analog-to-digital converters (ADCs) are implemented. In this paper, its image sensor architecture, pixel configuration and operation are described and characterization results are reported.

I. Introduction

Machine vision and high frame rate applications usually require the global shutter operation to "freeze" the image. In global shutter pixels, an in-pixel signal memory, an additional global reset gate and a global transfer gate should be equipped, which results in a larger pixel size than that of general purpose CMOS imagers. In previously reported high speed CMOS image sensors with the global shutter functionality, relatively large pixels, ranging from 7μm to 16 μm, have been used [1-3]. However, the large pixel size results in a large die size and thus high image sensor cost. Therefore, pixel size reduction has been strongly requested for low cost applications and/or small module applications.

In this paper we present a 600×600 pixel prototype imager with a 4.4μm pitch 5-transistor global shutter pixel. The imager can operates at a high frame rate of 500fps.

II. Sensor Design

a. Chip specifications and structure

Figure 1 shows a block diagram of the image sensor. The pixel signals from a 600×600 imaging array are read out through top and bottom circuit blocks and transferred to analog signal chain / analog-to-digital converter (ASC/ADC) blocks. The column block consists of column gain amplifiers, sample-and-hold capacitors and a column decoder with column select switches.

The ASC/ADC block consists of second gain amplifiers and 8bit low power pipeline ADCs. A DAC/Buffer block contains bias generators and reference voltage generators that are controlled by two-wire serial I/F, thus yielding a fully digital interface. All internal pulses are generated by an internal timing generator (TG) so that external control/trigger inputs are minimized.

The chip handles pixel readout and signal processing at 200Mpixel/s with a 50MHz master clock and operates at 500fps with 600×600 full pixel resolution.

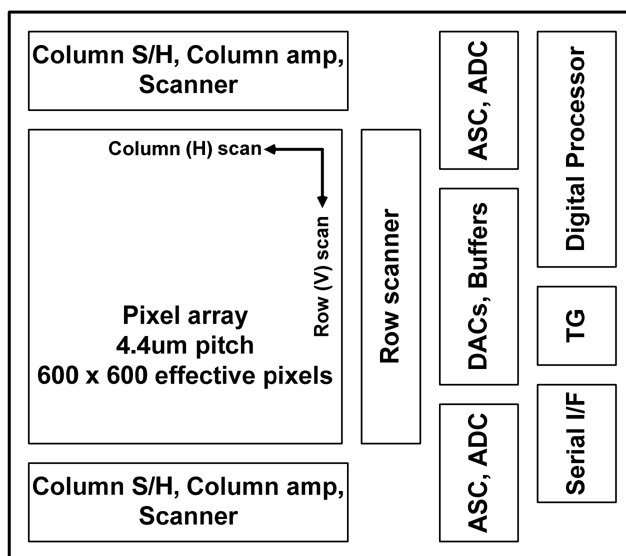


Figure 1. Block diagram of the chip.

b. Pixel configuration

The pixel consists of a pinned photodiode (PD), pixel memory (storage node M) and five transistors for pixel reset and readout as shown in Figure 2. The AB gate controls reset of the photodiode. This reset is global, i.e., all the pixels are reset simultaneously. The TX gate controls the charge transfer from PD to M. The complete charge transfer is required for both AB and TX operations to eliminate image lag and pixel-wise FPN.

In a global shutter mode, signal charge is transferred to node M, then the charge is read out in a similar manner to that of the conventional 3T pixel operation. Since a signal charge integration part and a readout part are separated by TX, the pixel allows simultaneous operations of charge integration and signal readout.

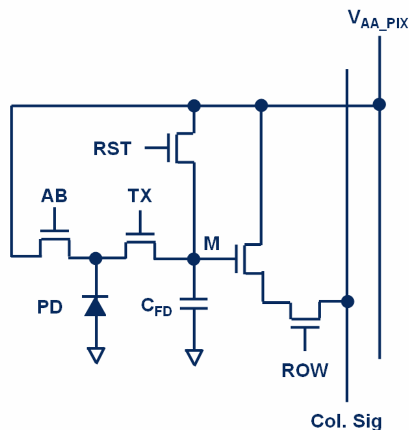


Figure 2. 5T global shutter pixel configuration

c. Signal chain

A schematic diagram of the signal chain is shown in Figure 3. The imager has two gain stages; one is in the column block and another in the video ASC block, as a primary gain stage and a secondary supplemental gain stage, respectively.

Pixel signal is amplified up to 8x by the column amplifier simultaneously to the pixel readout then stored on SH capacitors. Through a column select switch addressed by the column address decoder, stored signal in the SH capacitor is serially transferred to the ASC block followed by a low power 8bit ADC. Four ADC's, each operates at 50Msps, are integrated. Thus a total data rate reaches 200Msps.

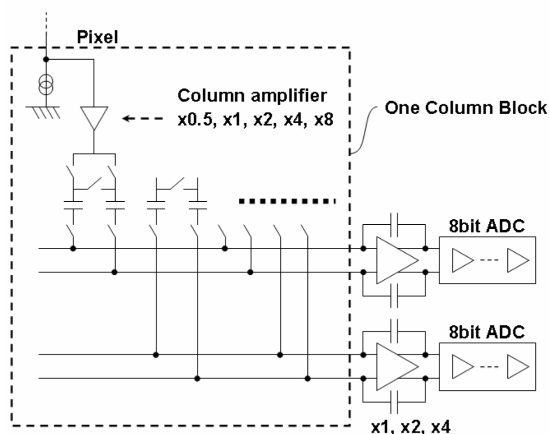


Figure 3. Signal chain of one column block

d. Global control and internal operation

A timing diagram for a frame operation is shown in Fig. 4. The sensor receives three external control pulses, 'START_EXPOSURE', 'END_EXPOSURE', and 'READ_START', each triggering the start of the exposure, the end of the exposure and the signal readout sequence. When 'START_EXPOSURE' is asserted, all photodiodes are reset by the global AB pulse that sweeps the charge out of the photodiode. Next, 'END_EXPOSURE' determines time for global TX that forces the charge to transfer from a photodiode to a memory node M. Readout of the charge in the memory node M starts when 'READ_START' pulse is asserted.

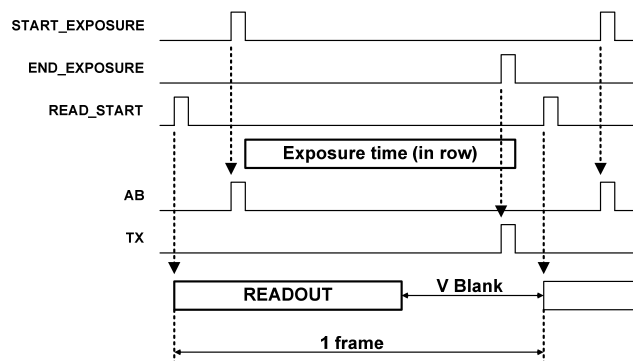


Figure 4. Operation timing

I2C interface is used for detail imager control. Also, two register banks are implemented, thus enabling instantaneous switching between two registered operation modes. This functionality helps enhance usability of high-speed imaging. For example, one register is set for a high-frame rate operation with reduced number of readout rows, and the other is set for reading out full resolution images. In this case, when an object is detected while the imager is operating in the high-frame rate mode, the system requests the imager to capture an full resolution image, thereby the imager immediately changes its operation mode for the full resolution snapshot readout. When the snapshot mode is chosen, the signal memory M should be reset to clean up noise charge or lag charge on the node during the charge integration period before the global TX is asserted.

III. Fabrication and Characterization

a. Fabrication

The 600×600 pixel image sensor was fabricated in 0.13μm 2P4M CMOS image sensor process. The prototype is a monochrome sensor with an on-chip

microlens array.

Figure 5 shows the top layout of the imager. An imager core including a pixel array and the rest of the analog blocks, together with integrated logic circuits, are implemented for prototyping. Video output is read out through 8bit × 4 parallel output ports, each handling a 50MHz data rate. Thus, a total output data rate of 200Mpix/sec is achieved. Imager core size is approximately 4.0mm × 4.0mm.

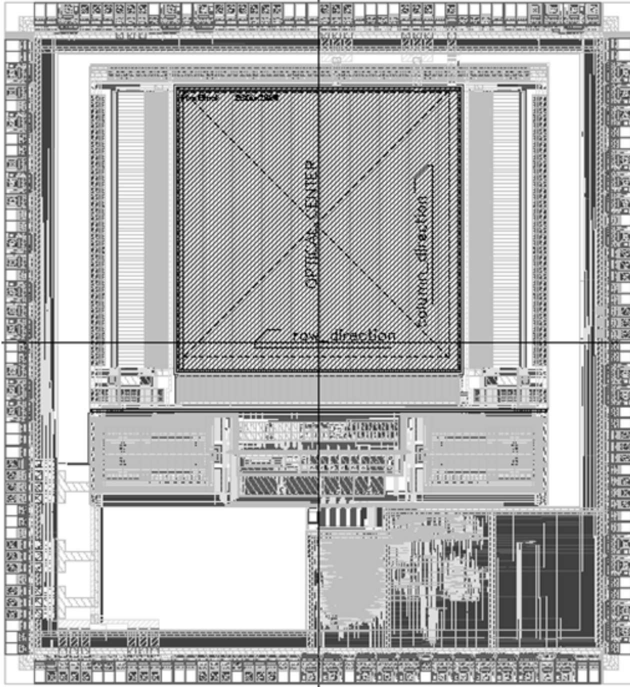


Figure 5 Prototype chip layout

b. Operation sequence for characterization

Besides the external trigger mode, the imager operation can be programmed with combinations of two registered modes. To perform characterization, we use a following operation sequence as shown in Figure 6; One cycle includes 8 fast readout frames and 8 full resolution readout frames. 32 effective rows are read out at 5000fps in the fast readout period then full resolution readouts at 500fps follow.

A full resolution image is evaluated from the first full resolution image. Also, image lag can be characterized with consecutive 8 frames in the full resolution readout period. Characterization was done under the 500fps full resolution condition.

c. Characterization results

Fig. 7 shows a spectral response. With an on-chip microlens, peak quantum efficiency reaches 63% at 500nm. Also the result shows good sensitivity against a wide wavelength range from near ultraviolet to near infrared. Quantum efficiency exceeds 20% within a range from 380nm to 830nm.

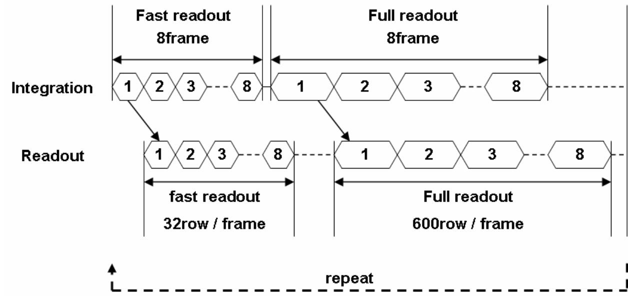


Figure 6. Operation cycle for characterization

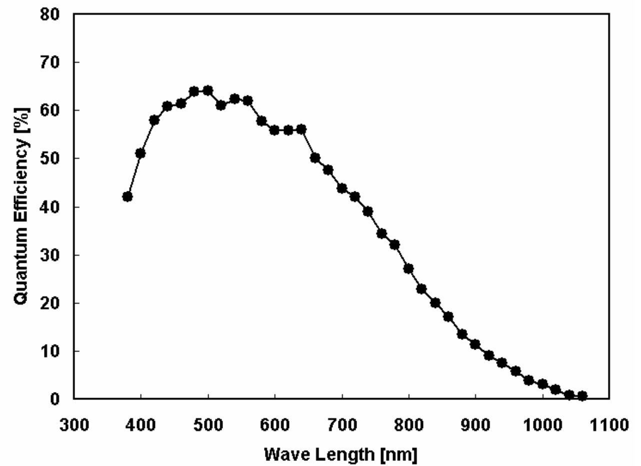


Figure 7. Spectral response

Image lag was negligibly small, which demonstrates the signal charge transfer from the pinned photodiode to both the memory node and the AB drain is almost complete.

Noise performance versus analog gain is plotted in Figure 8 with pixel-wise noise, temporal noise and structural noise. The data was obtained from one output port of 4, therefore offset variation between output ports are ignored. Total noise is very close to pixel random temporal noise and the result suggests main noise source is the pixel temporal noise that is caused by a reset operation of a floating node M in Figure 2. Capacitance of the floating node is estimated to be 3.4fF and it causes noise of 27 electrons-rms per reset operation. FPN including structural noise is smaller than 1/5 the pixel temporal noise when gain is larger than 2 and it is mostly invisible.

On the other hand, offset variation between signal chains was measured to be approximately 1.2LSBs at 4x gain, which corresponds to 17 electrons-rms. Although this noise level is smaller than 1/2 the total

noise at 4x gain, we can reduce the noise by offset adjustment in the backend process.
An image obtained from a snapshot and summary of imager specifications are shown in Figure 9 and Table 1, respectively.

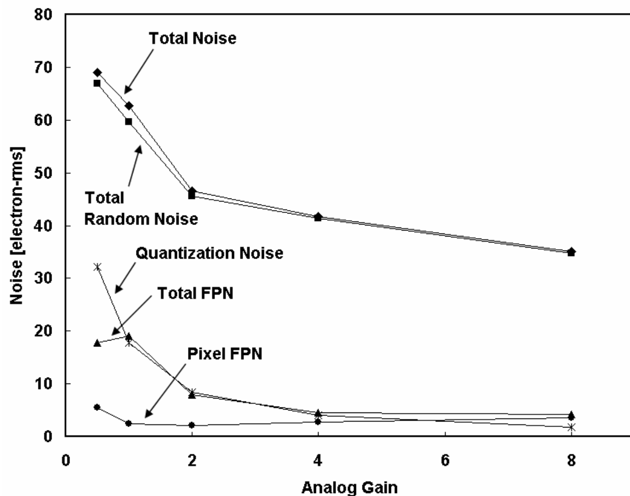


Figure 8. Noise measurement result

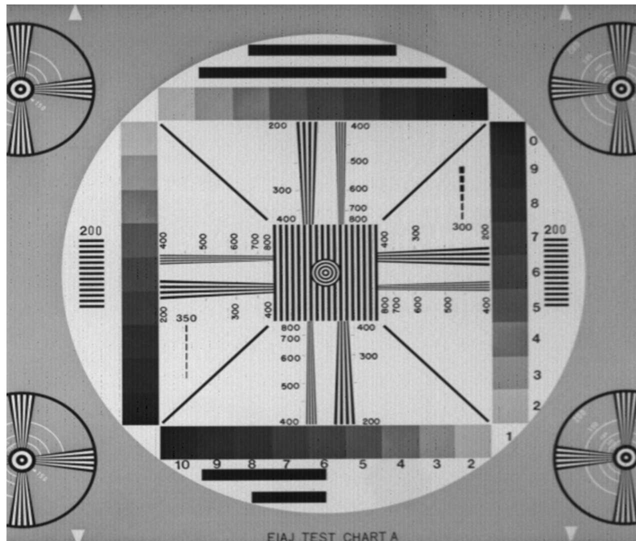


Figure 9. An output image from the first frame in a full resolution readout period in Figure 6 operating at 500fps. No correction of channel offset variations.

Table I. Specifications and Performance

Resolution	600 x 600
Pixel size	4.4 µm
Optical format	1/5 inch
Shutter scheme	Global shutter
Master clock	50 MHz
ADC resolution	8 bit
Full resolution frame rate	500 fps
Power consumption	248 mW
Peak quantum efficiency	63% at 500nm
Total noise	42 electrons at 4x gain
Linear full well capacity	12k electrons

IV. Conclusion

We have developed a prototype 600×600 pixel, 500 fps CMOS image sensor with a 4.4µm 5T pinned PD global shutter pixel for low-cost, high-frame rate imaging applications. It features a quick operation mode switching (ex. from a 5000fps windowing mode to a 500fps full resolution mode, and vice versa), while no degradation in image quality of the first frame after the switching is observed. High quantum efficiency of 63% at 500nm is obtained. The kTC noise associated with the in-pixel memory reset is a dominant noise source. Both FPN and image lag are reasonably suppressed.

Acknowledgment
The authors acknowledge R. Panicacci, J. Solhusvik, T. Gilton, G. Agranov, R. Mauritzson, N Bock and P. Gallagher for their guidance and valuable discussions. The authors would also like to thank H. Wang for developing a characterization system.

References

1]http://www.micron.com/products/partdetail?part=MT9M413C36STM
2] A. I. Krymski and N. Tu, “A 9-V/lux-s 5000-frames/s 512 ×512 CMOS sensor,” IEEE Trans. ED., vol. 50, no. 1, pp. 136-143, January 2003.
3] N. Bock, et al., “A CMOS image sensor with global shutter and extended dynamic range, “ in Final Program and Proceedings of ICIS ’06 Int’l Congress of Imaging Science, pp. 571-574, 2006.

2MPix 2.6μm Pixel Size Image Sensor in AIC Technology

T. Lulé, F. Mütze, M. Sommer
J. Prima(1), F. Roy(1), B. Glück(1), D. Thomas(1), R. Nicol(2)

STMicroelectronics, Imaging Division, 12 rue Jules Horowitz,
38019 Grenoble, France, tarek.lule@st.com, +33 4 76 58 59 35
(1) STMicroelectronics, 850 rue J. Monnet, 38926 Crolles Cedex, France
(2) STMicroelectronics, 33 Pinkhill, Edinburgh EH12 7BF, UK

Abstract

The general interest in AIC image sensors lie in the 3D integration that vertically separates light collection and signal processing, naturally giving rise to high QE. Low optical cross-coupling is replaced by an electrical cross coupling that can be mastered with standard CMOS design techniques. A 2MPixel image sensor with 2.6um pixel size is presented with very large full well and good low light sensitivity despite the presence of kTC noise. Permanent change of material characteristics under extreme light conditions has been reduced by optimization of material properties and design paradigms.

Introduction

Various CMOS image sensors overlaid with thin amorphous semiconductor layers, also sometimes referred to as AIC (Above-IC) or TFA (Thin-Film on ASIC) image sensors, have been presented in the past. In some publications the additional layers are used to create avalanche photodiodes that amplify the photo-generated current which can lead to high pixel to pixel gain variations [1]. Instead, the present publication realizes a good sensitivity in low light conditions due to the large quantum efficiency of the amorphous silicon photodiode as was predicted previously [2].

Figure 1 shows the principle cross section of an AIC image sensor. Only the readout electronics is realized by standard bulk CMOS technology. The amorphous silicon layer system is deposited on top of the CMOS wafer. It is sandwiched between two electrodes where the front electrode is realized from a transparent conductive oxide (TCO) while the rear electrode can be realized from any suitable material [3].

Cross-Coupling

In CMOS image sensors, the number of metal layers is strongly limited as the light that passes through the color filter must be focused on the corresponding photo diode. Any reflection, scattering contributes not only to the loss in signal in the targeted pixel, but furthermore when impinging on a neighbor pixel contributes to color cross talk. This cross talk reduces the separation of the colors and needs to be corrected by a color matrix with larger off-diagonal components which reduces the usable signal and adds noise thus reducing the signal to noise ratio twofold [4].

In AIC image sensors, after passing a color filter the light only has to penetrate the TCO electrode and is absorbed directly in the underlying AIC a-Si layers. Effectively the optical path length is greatly reduced. This directly allows for lens designs with much larger chief ray angle as can be found especially in miniature camera modules for portable devices such as mobile phones. Applications with high circuit density or more complex pixel architectures also benefit from the additional routing layers, as for example the 120dB LARS image sensor employing an auto-exposure mode per pixel [5]. Instead, an effect on signal quality is given by capacitive coupling (depicted by symbolic equipotential lines) between adjacent metal lines around the conductors for the photo current, which can be much easier controlled. The optical cross coupling effect when transporting the light through the metal stack in CMOS sensors is thus replaced by an electrical cross coupling effect, both being electromagnetic but at very different frequencies.

Sensor Design

A 2MPixel (1620 x 1228) image sensor with 2.6um pixel size has been realized based on a 180nm technology node with 5 layers of metal. The pixel is based on a commonly used CTIA architecture shown in Figure 2 [6]. While the photodiode is realized in the a-Si:H layers, only three transistors need to find place in the pixel as shown in pixel layout of Figure 3. The largest transistors M1 forms the driver of an inverter. It's large size leads to a reduction in 1/f noise and probability for RTS noise. M1 is connected to a common column line through a read transistor M2. The

input and the output of the CTIA are shorted by the third transistors M3 to reset the pixel to a voltage level depending on M1. The integration capacitor is realized by parasitic metal-metal capacitance throughout the metal stack thus benefiting from the large number of metal layers.

The chip floor plan is shown in Figure 4 with the pixel matrix marked in red. Mainly analogue support circuits have been implemented here as the most critical elements. An I2C interface serves to configure various analogue settings and test modes. Otherwise, the digital control logic is largely implemented in an external FPGA to allow for flexible changes in timing or operating modes. A CDS readout mode with uncorrelated kTC noise is used to reduce FPN while a kTC-noise-correlated mode, called double-read, employs the use of a buffer memory to store an image of the per-pixel kTC noise level.

Results

Figure 3 shows a sample picture taken from the image sensor with an excellent picture quality and no visual artifacts such as pin holes or white pixels. The measured dark current has a mean value that is much higher than for pinned photodiode technology. However, the distribution proves to be more narrow which provides a comparable level of white pixels at low light illuminations.

Feature	Performance
Pixel Size	2.6 µm
Sensitivity @6000K	1.8 V/lxsec
Conversion Gain	88.2 uV/e^-
Max. SNR (incl. FPN)	40 dB (29 dB)
Read Noise (Single Read)	11 e^- (59 e^-)
Dynamic Range (Single Read)	47 dB
Dynamic Range (Double Read)	62 dB
Dark Current Mean/Sigma	49 aA / 26 aA
Min. Illumin. @T=67ms,DblRd	22 mlx
Full usable Well	13.8 k e^-
FPN	680uV
Pixel PRNU at Sat. (T=67ms)	1.8%

Table 1 Performance Characteristics of AIC Image Sensor

The detailed performance characteristics in Table 1 show the typical features of a CTIA pixel design. The small effective integration capacitance leads to a high sensitivity in V/lxsec.

The concomitant large kTC noise needs to be corrected by means such as double read operation, in order to provide good low minimum illumination value of 22mlux. As can be shown, the kTC noise can become progressively de-correlated between start and end of frame for long frame lengths, given and depending on the a-Si coupling resistance between adjacent pixels. A tapered reset analogue to previous proposals [7] theoretically giving a reduction of kTC noise level by nearly 2.5, was shown to be difficult to apply due to inherent variations of Vth of the reset transistor M3.

When focusing strong light sources (Halogen bulb, Sun) the lens creates a very high intensity light spot on the sensor surface of up to 100Mlux. The extreme light condition can lead to change in the properties of the amorphous material called "aging" as was discussed in previous publications [8].

The two effects that produce at first are a reduction in sensitivity and an increase in dark current. The stability under these conditions was greatly improved based on circuit and technology efforts [9]. As a novel approach to the effect, a safe operating area in the intensity/time space has been defined as the operation condition under which no visual artifacts due to this effect is noticeable. Figure 6 shows the safe operating area chart that was obtained from the sensor using state of the art AIC technology. The points follow an $I^2 \times T = const$ trend line rather than $I \times T = c$.

Outlook

Figure 7 shows a sample 1.39um pixel in AIC technology using a 3T source follower architecture per pixel based on a 130nm technology node with little process modifications. Using parasitic extraction programs and ELDO simulator the performance of the pixel is extrapolated. While the full well and maximum SNR are still large with >11ke and 40dB, the dynamic range is clearly limited by the kTC noise of the diode and wiring capacitance to 50dB. The demand of the kTC-correcting double read of a frame store becomes more and more common in today applications. Alternative techniques that compensate for at least part of the kTC noise have been published previously and would allow to regain a dynamic range of 60dB.

Acknowledgements

The authors would like to thank all actual and former colleagues of ST France and UK, as well as from CEA/LETI and UNAXIS who have contributed to the results.

References

[1] Y. Takiguchi et al, IEEE Trans. on Electron Devices, Vol. 44, No. 10, p. 1783, 1997

[2] T. Lulé et al, IEEE Trans. Electron Devices, vol. 47, p.2110, Nov. 2000

[3] M. Böhm et al., Materials Research Society Symposium Proceedings, Vol. 507, p. 327, 1998

[4] R. Nicol et al., 2005 IEEE Workshop on CCD and Advanced Image Sensors, p. 84

[5] T. Lulé et al., 1999 IEEE Workshop on CCD and Advanced Image Sensors, p. 215

[6] Fowler et al, Sensors and Camera Systems for Scientific, Industrial and Digital Photography. Applications II, Proc. SPIE Vol. 4306, p. 68, 2001

[7] B. Pain et al, 1999 IEEE Workshop on CCD and Advanced Image Sensors, p. 140

[8] R. Miyagawa, IEEE Trans. on Electron Devices, Vol. 39, No. 2, p. 325, 1992

[9] N. Moussy et al, IEDM Technical Digest, p. 182, 2006

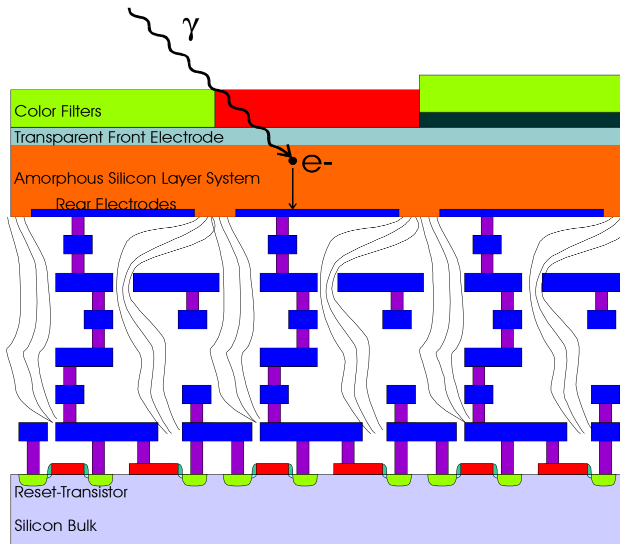


Figure 1 Principle Cross Section of AIC Image Sensor Technology

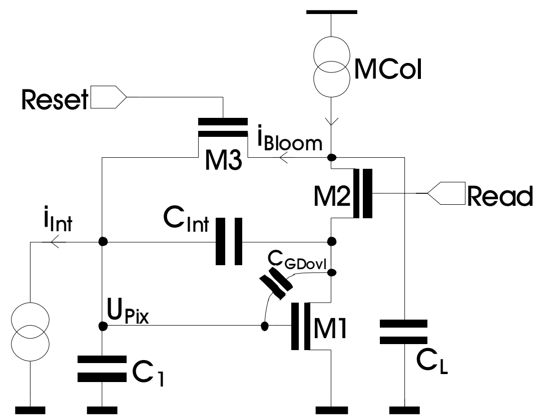


Figure 2 Schematic of CTIA Pixel Architecture of the AIC Image Sensor

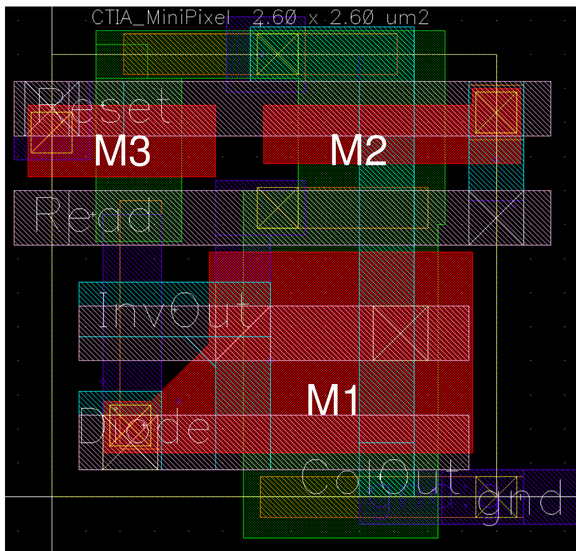


Figure 3 Layout of CTIA CMOS Pixel Circuit

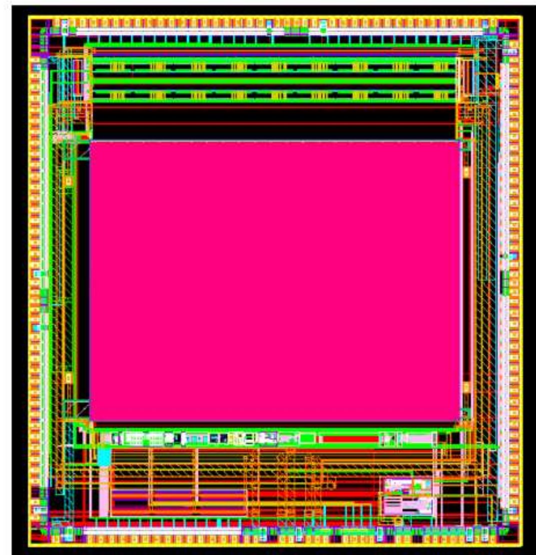


Figure 4 Chip Layout of 2MPix Image Sensor in AIC Technology

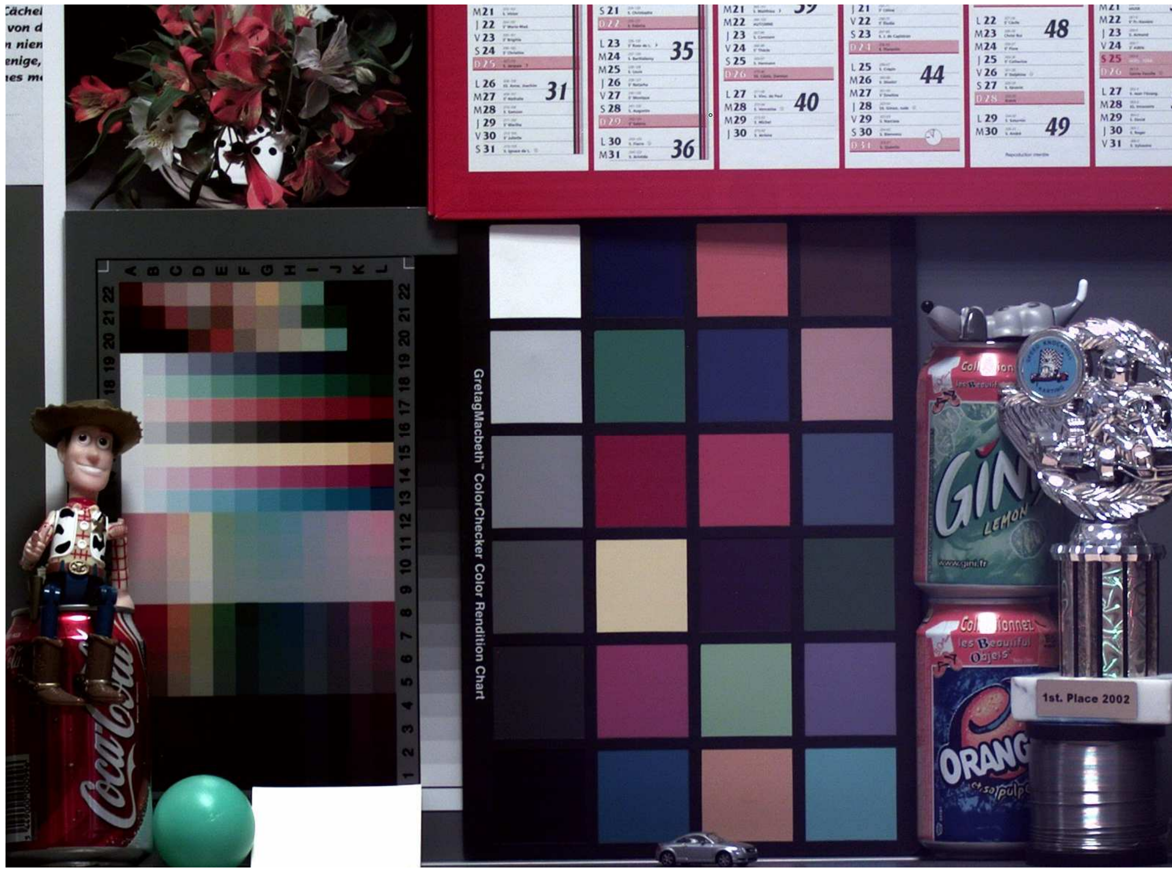


Figure 5 Color Picture Taken with the Sensor

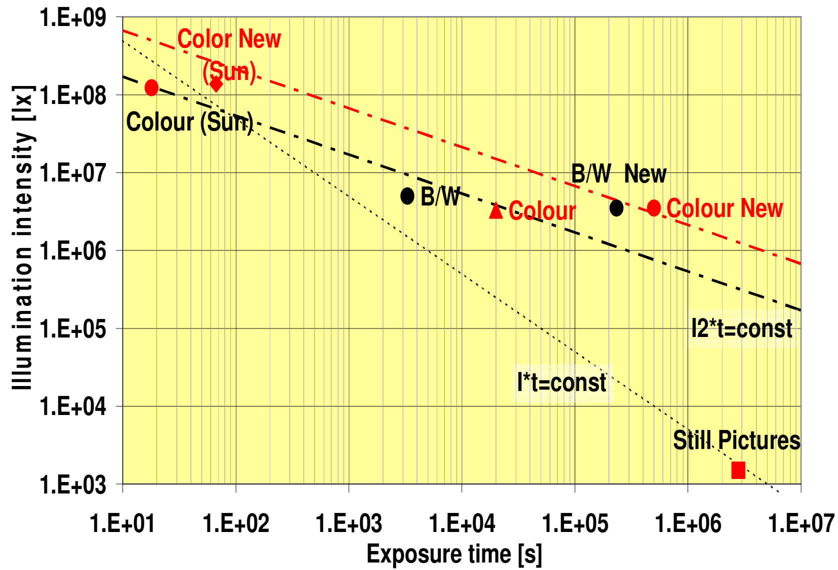


Figure 6 Safe Operating Area Chart for AIC Image Sensor for initial and Improved (New) Sensors with (Color) and without (BW) Color Filters

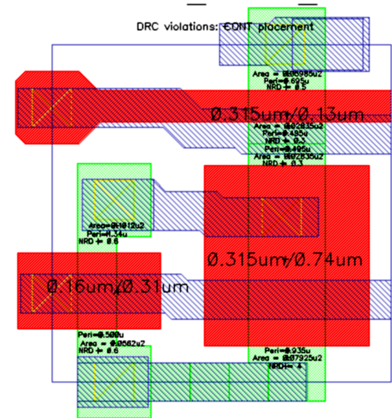


Figure 7 Sample 1.39um Pixel in "130nm based Technology"

52 Mega-pixel APS-H-size CMOS Image Sensor for Super High Resolution Image Capturing

Masaaki Iwane, Takashi Matsuda, Takashi Sugai, Koichi Tazoe, Takashi Okagawa, Toshiaki Ono,
Takanori Watanabe, Katsuhisa Ogawa, Hidekazu Takahashi, Shunsuke Inoue
Canon Inc, 2596 Yoshioka Ayase-shi Kanagawa-ken, 252-1124, Japan
Phone: +81-467-70-5209 Fax: +81-467-70-5462 Email: iwane.masaaki@canon.co.jp

Abstract

We have developed a new CMOS image sensor having pixels of more than 52M in APS-H size. The CMOS image sensor has the most number of pixels known to date without stitching. The sensitivity of the monochromatic image sensor is 39000e$^-$/lx・s. The sensitivity of the color image sensor (green pixel) is 16600e$^-$/lx・s. Pixel size is 3.2um x 3.2um. Random noise is 5.5e$^-$ with a saturation level of 24000e$^-$. The CMOS image sensor has 5 x 5 random block readout mode and 4(2×2) adjacent pixels averaging mode. The reproduced image shows splendid high resolution.

1. Introduction

The number of pixels in image sensors used for digital cameras and camcorders is growing year by year. In addition, demand for high resolution image capture in machine vision and security cameras is becoming stronger. We have already reported small pixel CMOS image sensor for full high-definition camcorders [1] and large format image sensor chip for digital SLRs [2]. The both technologies have been merged to realize a 52 Mega-pixel CMOS image sensor in APS-H film size. The CMOS image sensor has the most number of pixels known to date without stitching [3].

2. Pixel Architecture

Figure 1 shows schematic cross section of pixel. Shallow trench isolation (STI) is employed for the pixel isolation. The buried photodiode is surrounded by the potential barrier of p type regions. These structures contribute to low cross talk, high sensitivity and high saturation. The pixel pitch is 3.2µm×3.2µm with high conversion gain using 2-shared pixel architecture. M1, M3, M4 and FD represent transfer gate, reset MOS transistor, source-follower amplifier and floating diffusion, respectively.

We have experimentally fabricated both monochromatic image sensor and color image sensor. The monochromatic image sensor has micro lenses and colorless interlayer that has same thickness as the color filter of the color image sensor.

3. Circuit Structure

Figure 2 shows readout equivalent circuit with pixel unit. Two buried photodiodes (PD1, PD2) and two transfer gates (M1, M2) share one FD, reset MOS transistor (M3) and source-follower amplifier (M4) in the pixel unit [1].

The signal on the output line is amplified by a column amplifier to suppress random noise [4]. The column amplifier consists of a CMOS operational amplifier, an input capacitor (C_0), a feedback capacitor (C_{FB}) and a switch MOS transistor. The amplifier gain is set by the ratio of C_0 to C_{FB}. Gain settings of ×1.5, ×3, ×6, ×12 and ×24 are employed.

The noise cancellers, consisting of line memories (C_{TN} and C_{TS}), remove the vertical offset stripes caused by the column amplifiers. Each line memory stores the reset level of the column amplifier (N) and photo signal level (N + S), individually. Output amplifier subtracts voltages stored on C_{TN} from the voltage on C_{TS} and output the amplified signals.

Figure 3 shows a block diagram of the CMOS image sensor. The image signals are read-out in 8ch with 20MHz clock input. Vertical shift register and horizontal shift register (represented by V1,…,V5 and H1,…,H5) are divided into 5 blocks in order to achieve arbitrary block group readout. Decoders control these divided shift registers.

4. Specification and characteristics

Specifications and characteristics are summarized in Figure 4. The sensitivity of the monochromatic image sensor is $39000e^-/lx\cdot s$. The sensitivity of the color image sensor (green pixel) is $16600e^-/lx\cdot s$. Random noise is $5.5e^-$ with a saturation level of $24000e^-$. Dark current is $56.4e^-/s$(@60℃) per pixel.

Figure 5 shows input referred noise versus actual column amplifier gain of the image sensor. Up to ×3 gain setting (actual gain is 2.93), the signal can be read out without losing pixel saturation.

Figure 6 shows spectral characteristic of the color image sensor. High sensitivity and low cross talk have been realized.

Figure 7 shows reproduced image of 52M-Pixel taken by the image sensor with full readout mode. With 52M-pixels, splendid high resolution is achieved. Figure 8 is another reproduced image with full readout mode.

Figure 9 shows reproduced image with 5 x 5 random block readout mode. With this mode, any partial 25(=5 x 5) blocks can be read. The readout of arbitrary combined blocks is possible. In addition, the monochromatic image sensor has 4(2×2) adjacent pixels averaging mode. In this mode, the signals in vertical adjacent pixel are averaged in FD of 2-shared pixel, thus can be readout faster than a 52M full readout mode.

Figure 10 shows a chip micrograph. of the CMOS image sensor.

5. Conclusion

Super high resolution image capturing is archived with the APS-H size 52M-pixel CMOS image sensor. The CMOS image sensor has small random noise and high saturation. The reproduced image shows splendid high resolution. The CMOS image sensor has random block cropping mode. The monochromatic CMOS image sensor has 4(2×2) adjacent pixels averaging mode.

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The authors wish to thank the members of the Semiconductor Device Development Center and Semiconductor Device Plant of CANON INC. for their valued contributions to this study and experimental manufacture.

References:

[1] H. Takahashi, et al., "A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders" *ISSCC Dig. Tech. Papers,* pp. 510-511, Feb., 2007.

[2] S. Inoue, et al., "A 3.25M-pixel APS-C Size CMOS image sensor," *IEEE Workshop on CCDs and Advanced Image Sensors*, pp.16-19, 2001.

[3] Suat U. Ay, et. al., "A 76 x 77mm^2, 16.85 Million Pixel CMOS APS Image Sensor," *2006 Symposium on VLSI Circuits Digest of Technical Papers*.

[4] S. Kawahito, et al., "A Column-Based Pixel-Gain-Adaptive CMOS Image Sensor for Low-Light-Level Imaging," *ISSCC Dig. Tech. Papers*, pp. 224-225 Feb., 2003.

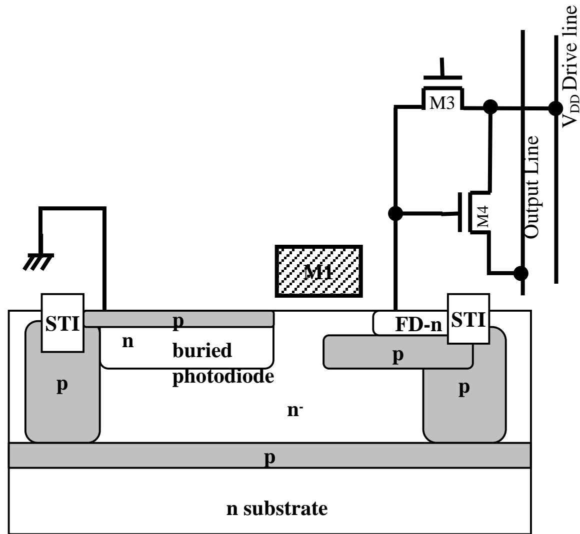


Figure 1 Schematic cross section of pixel.

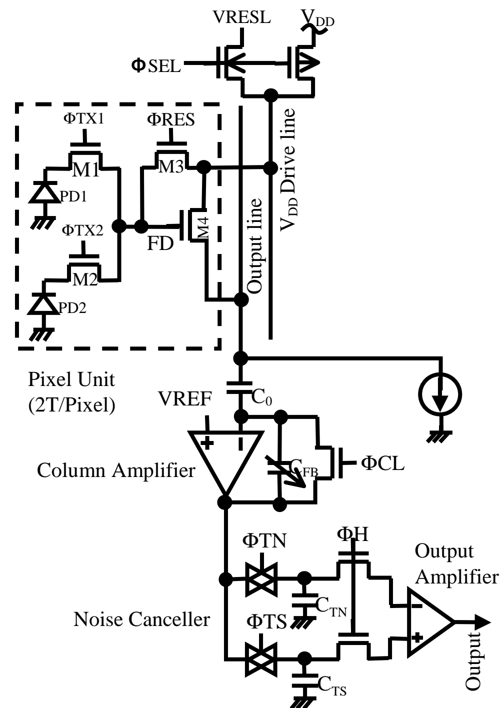


Figure 2 Readout equivalent circuit with pixel unit.

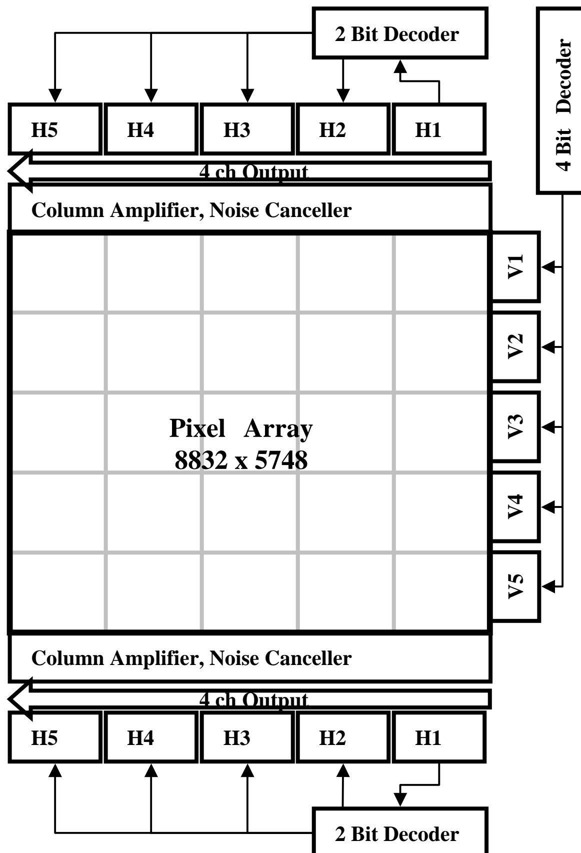


Figure 3 Block diagram.

Technology	0.18µm 1P 3M CMOS
Chip size	31.6mm(H)x23.1mm(V)
Pixel size	3.2µm(H)x3.2µm(V)
Number of total pixels	8984(H)x5792(V)
Number of effective pixels	8832(H)x5748(V)
Pixel rate	160MHz (20MHz×8ch)
Column gain stage	×1.5, ×3 , ×6 , ×12 , ×24
Readout Mode	•52M full readout •5 x 5 random block readout •Adjacent 4 pixels addition readout(the monochrome image sensor only) • Rolling shutter
Conversion gain	50.2 µV/ e^-
Sensitivity of the monochrome image sensor	39000 e^-/lx s (2856k light source with IR cut filter)
Sensitivity of the color image sensor(Green pixel)	16600 e^-/lx s (2856k light source with IR cut filter)
Saturation full well	24000e^-
Dark current(per pixel)	56.4e^-/s (@60℃)
RMS random noise	5.5e^- (@column gain stage= 3)
Power supply	5 V
Power consumption	430mW

Figure 4 Specification and characteristics.

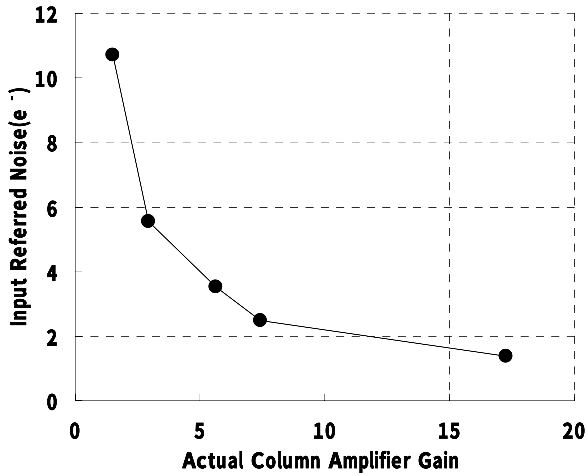


Figure 5 Input Referred noise vs. Actual column gain.

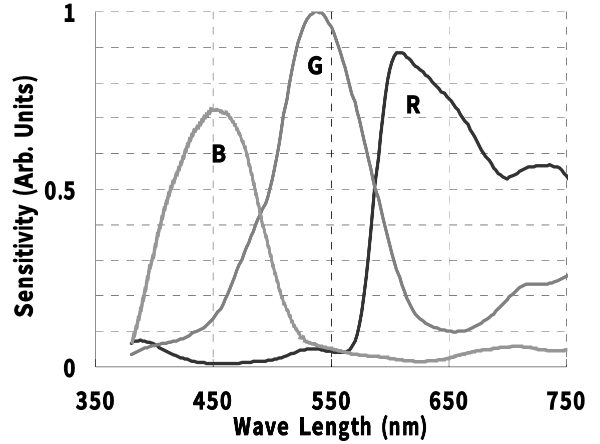


Figure 6 Spectral characteristic of the color image sensor.

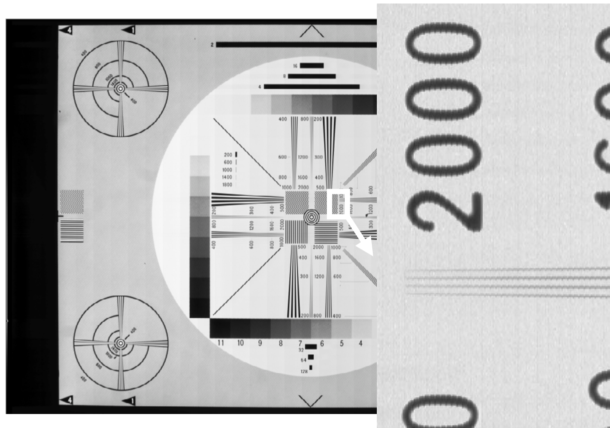


Figure 7 Reproduced image of the resolution chart captured by the monochromatic image sensor.

Figure 8 Another reproduced image captured by the monochromatic image sensor.

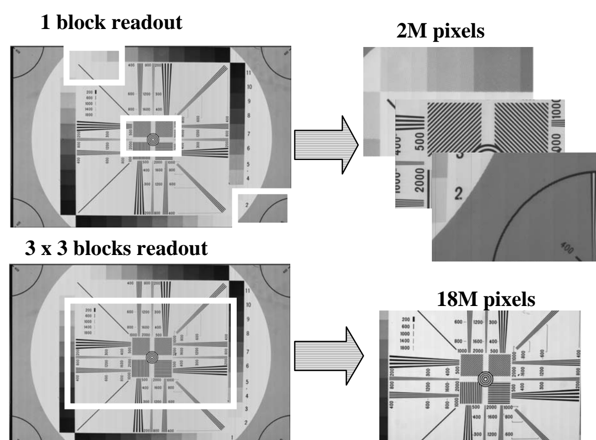


Figure 9 5 x 5 random block readout .

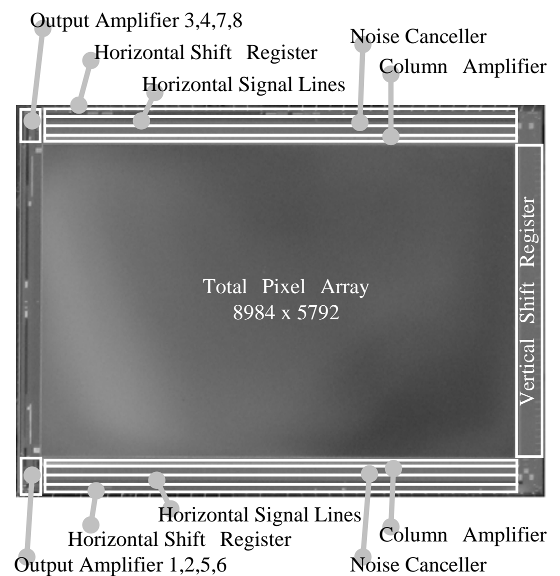


Figure 10 Chip micrograph.

A CMOS image sensor for Earth observation with high efficiency snapshot shutter

Gérald Lepage[(1)], Alex Materne[(2)], Christophe Renard [(3)]

(1) Cypress – FillFactory, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium, fle@cypress.com.
(2) CNES, 18, avenue Édouard Belin, 31401 Toulouse Cedex 9, France, Alex.Materne@cnes.fr.
(3) Thales Alenia Space, 100, bd du Midi, BP 99, 06156 Cannes la Bocca Cedex, France, Christophe.Renard@thalesaleniaspace.com

Abstract

This article describes a 4 / 16 Mpixel CMOS image sensor with 106 dB efficiency snapshot electronic shutter and 62 dB dynamic range within +/- 3 % linearity. It is monolithic, front side illuminated and processed on plain 0.35 µm process with stitching. This sensor could be an interesting alternative to power consuming TDI CCD sensors in LEO orbit configuration.

1. Introduction

With increasing performances, CMOS detectors are gradually becoming attractive for CCD replacement in space applications. First used where the added functionality of CMOS devices is most obvious (e.g. star trackers) [1], they are now competing with observation detectors [2][3]. This paper presents the specification definition, the design and the characterization of a sensor compatible with a LEO orbit mission.

2. Application

Spaceborne Earth observation missions implemented by CNES (French space agency) for metric resolution imaging, from Spot satellites to Pleiades, are mostly based upon scanning satellites with camera operating in a puhsbroom mode from a polar heliosynchronous LEO orbit.
Detectors at the focal plane are linear CCD arrays and the 2D image is sequentially built by a line by line integration of photogenerated charges, with a sampling period along the velocity axis matched to the flight duration over the requested ground pitch.
A significant improvement in signal to noise ratio was reached with linear CCD arrays operated in Time Delay Integration (TDI) mode. TDI allows dissociation of the integration time from sampling period along the velocity axis. In a TDI detector the linear array is repeated over N stages. Photogenerated charges are transferred from stage to stage at a speed matching satellite motion, allowing an integration time N times the sampling period. When combined with back thinning technology, which offers high quantum efficiencies, linear CCD TDI arrays are interesting for high resolution earth observation applications [4].
It remains however necessary to investigate and develop alternative solutions to CCD TDI back thinned detectors as they suffer from several drawbacks:

- Clock levels required to operate the CCD need specific driving devices, and lead to high power dissipation,
- The offer in back thinned CCD TDI products is decreasing: it is now limited to only one company in Europe.

The emergence of CMOS image sensors (CIS) and their very fast development for high volume applications bind the actors of the space borne sensing applications to take a look at the performance achievable with CMOS technologies.
For Earth observation applications in the metric resolution range from LEO scanning orbits, one solution is to re-create in CMOS technology the principle of TDI operation, in order to keep the benefit of large integration times decoupled from sampling period. Such a device has been developed by Cypress, under Thales Alenia Space contract [5], proving that the concept is adaptable to CMOS technologies. It shows however some limitations:

- The complexity of the architecture and the readout noise both increase with the number of TDI stages,
- As no charge transfer is performed in CMOS devices, synchronisation between charge transfer and satellite velocity is no more applicable, and MTF degradation has to be taken into account, along the velocity axis. This drawback may be circumvented by oversampling but it adds more complexity to the architecture.

An alternative solution is to use CMOS 2D-arrays. 2D single shot image construction offers several advantages:

- Geometric corrections due to the satellite pointing axis drift, or instability during scanning, are no more required,

- The temporal axis dedicated to the image line by line construction in the case of a linear array is free and available to be used for multispectral imaging or image summation.

A 2D CCD array is operated on the French satellite PARASOL, launched in December 2004, on a LEO polar orbit, to observe the Earth atmosphere with a 5 km ground pitch. In this case the temporal axis is used to explore the spectral domain: 15 narrow band filters and polarizers are placed in succession in front of the 2D CCD array [6].

For metric resolutions, as the time allowed for integration decreases, it becomes necessary to include a mechanism for compensation of the satellite motion during image shot, and a shutter mechanism to prevent illumination during image readout. The conjunction of these two mechanisms is a significant drawback when compared to the TDI solution.

Thanks to the CMOS technology, the shutter function may be performed electronically and thus contributes to the simplification of the overall concept.

Taking into account the capabilities of the CMOS technology CNES decided to revisit the trade-off between 2D arrays and linear arrays, via the development of a snapshot 2D CMOS array for metric resolution Earth observation applications.

The main specifications were established to meet the requirements of a typical 1-meter resolution instrument, on a LEO microsatellite (see Table 1).

Requirements	Min	Typical	Max
Spatial resolution (m)		1	
Swath width (km)	8	12	20
Altitude (km)	500		700
Spectral band (nm)		[480 – 830]	
Spectral radiance useful range (W/m^2.sr.µm)		[10 – 320]	
Optics diameter(m)	0.3		0.4
Pointing stab. (µrad/s)			100
SNR @ 90 W/m^2.sr.µm	90		
MTF at Nyquist frequency	0.1		

Table 1: typical satellite requirements.

To effectively compete with linear array solutions, the design of the CMOS 2D-array detector had to be oriented toward the driving specifications below [7]:

- High quantum efficiency: the snapshot electronic shutter must be included in the pixel at minimum reduction of the fill factor. High QE is requested to keep integration time in the range allowed by pointing stability constraints.
- High shutter efficiency: to maintain the parasitic signal due to a high illumination during readout less than 2 % of the minimum useful signal at low illumination the shutter efficiency must be higher than 86dB.
- High readout frequency: minimise readout time.
- Large array size: the minimum size was specified at 2 k x 2 k, with the objective to reach 4 k x 4 k in order to reach a 12 km swath width with easy arrangement in the focal plane.
- MTF: as CMOS devices operate with reduced voltages, care must be taken in the selection of doping profiles to ensure a correct depletion depth. This is a key requirement to achieve a MTF as good as in CCD over the specified spectral band.
- Charge capacity: the charge capacity has to be designed to cover the full dynamic range and meet the signal to noise specification. The minimum specification was set at 75 ke^-.

3. Image sensor design

The sensor (Figure 1) has an array of 2004 x 2058 pixels divided into top and bottom sub blocks, enabling simultaneous read out of two rows. Pixel control, row control and biasing blocks are on the left side of the sensor leaving the right side free of bonding pads for abutting. Goal is to build a larger array (4008 x 4018) with the same mask set. As the pixel pitch is 14 µm, both devices are larger than the reticle size, therefore stitching technique is required. The sensor is monolithic and front side illuminated.

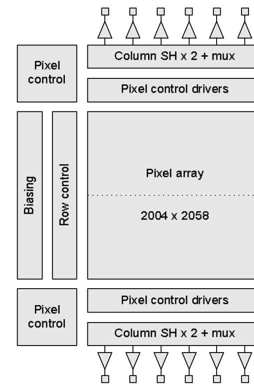


Figure 1: block diagram.

On chip control circuitry is straightforward. Pixel commands, synchronous for all pixels (electronic shutter), are directly controlled off chip. Rows and columns are selected via shift registers. Column sample and hold commands are also accessible directly off chip. Biasing is tuneable via off chips resistors.

The pixel (Figure 2) has 6 transistors and a capacitor. This architecture allows “snapshot” acquisition. If the integration time is longer than the frame read out time, off chip correlated double sampling is possible using

non destructive read out. Two frames are read out: one right after reset and one after the integration time. If the integration time is shorter than the frame read out time, then only "Raw" read out is possible, i.e. single frame read out after the integration time without kTC noise correction. In this case, the pixel array is operated as follows: it is first reset, and after the integration time the signal on the photodiode is sampled on the capacitor. Top and bottom frames are then read out simultaneously in a rolling shutter sequence through respectively top and bottom sample and hold arrays. Integrate while read out is only possible with raw read out.

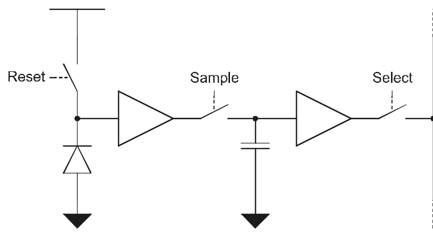


Figure 2: pixel architecture.

Main specifications driving the pixel were full well charge, fill factor, MTF and parasitic light sensitivity (PLS) of the electronic shutter. The PLS is defined as the ratio of the sensitivity when the shutter is closed (read out) and opened (integration time). The initial goal specification, 1/20000, is very low and multiple techniques have been used to meet it.

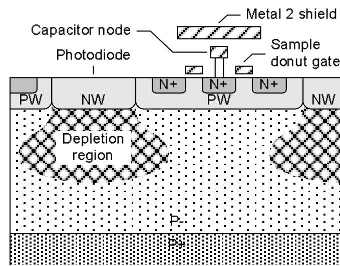


Figure 3: pixel simplified cross section.

One source of PLS is the sample switch. The reversed bias junction of the transistor tied to the capacitor is acting as a second photodiode and corrupts the signal stored on the capacitor in the period between the end of the integration time and when the row is read out. An obvious solution consists in shielding it from light to avoid direct charge generation (Figure 3). This is however not preventing collection of charge generated in the Pwell or the epi layer in the vicinity of the junction, even if the Pwell is repelling free electrons from the epi layer.

In [8], a deep NWell is efficiently used to shield the junction. However, this process step is not available in all technologies and typical large spacing design rules associated are not compatible with relatively small pixel. In addition, it is competing with the photodiode, especially for charges generated deep in the substrate (long wavelengths), resulting in a QE x FF degradation. Instead, the sample transistor has been drawn with a donut shape [9], de facto surrounding the parasitic light sensitive region with a ring of N+ active acting as a shield. This structure is more compact, with an N+ layer smaller and closer to the junction than in [8]. The rest of the pixel is classical. The photodiode is a NWell [10].

During frame read out, rows are sequentially sampled by column sample and hold stages. After the signal is stabilized, the row is multiplexed to 12 analogue outputs. In order to reduce the row blanking time, i.e. the dead time between two rows multiplexing burst required to sample a row onto the sample and hold stages, two rows of sample and hold stages on each side are used alternatively. Together with fast analogue outputs, this is reducing the frame read out time, which at the same time reduces the impact of PLS on the signal.

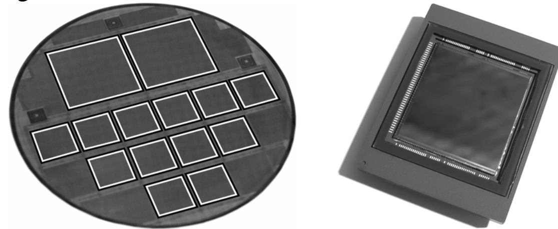


Figure 4: first wafer and device in PGA package.

The device has been processed in the 0.35 µm XFAB technology. In order to reduce costs, both low (4 Mpix) and high resolution (16 Mpix) devices have been processed on the same wafer (2 big and 12 small devices, see Figure 4Figure 4). Currently only the low resolution device has been assembled. Thanks to yield driven design techniques and an intrinsically reliable technology, preliminary estimation of the yield is excellent: on 19 devices assembled from 2 wafers, all are functional and 7 have hardly a dozen off specification pixels. Yield of the big resolution device is then expected to be fairly high.

4. Experimental results

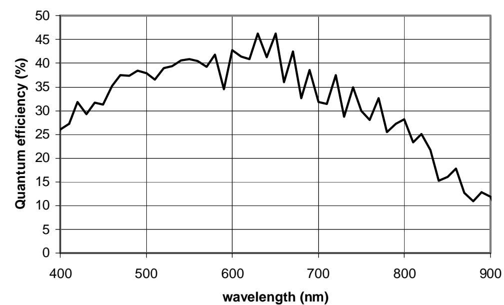


Figure 5: measured QE x FF.

Fine characterization has been completed and results are summarized in Table 2. All specifications have been met or exceeded. Measured external quantum efficiency is given in Figure 5. Peak QE is about 45 % and the roll off starts at about 650 nm, which is consistent with a 7 µm epi. Parasitic Light Sensitivity is at least 10 times better than the specification. A picture taken with the sensor is given in Figure 6.

Parameter	Value	Remark
Pixel size (μm^2)	14 x 14	
Pixel array	2004 x 2058 (4008 x 4018)	
Pixel type	NWell – 6T	
Analogue outputs	12 (24)	
Mean output data rate (Mpps)	300 (600)	Using only one SH array.
Main power supply	3.3 V	
Full well (ke^-)	130	Flat saturation
Full well (ke^-)	80	Within +/- 3 % linearity
Read noise (e^-)	60	Raw mode
Dark current	0.1 nA/cm^2	
QE x FF	35 %	Average on [470 – 830] nm
PLS	< 1/200000	> 106 dB
MTF at Nyquist frequency	> 0.6	X and Y, on [470 – 830] nm
Chip size (mm^2)	29.1 x 31.6 (57.2 x 59.0)	

Table 2: key specifications and measurements. High resolution sensor values are given in between brackets.

Figure 6: image with off line FPN correction.

5. Conclusions

A CMOS image sensor for Earth observation with high efficiency electronic shutter is presented. All specifications have been validated experimentally on a 2 k x 2 k array; 4 k x 4 k arrays will soon be assembled and evaluated.

6. Acknowledgement

The authors would like to thank the team, and in particular James Cunningham, Ian Daniels and Roy Starr at XFAB for helping us out with the processing and manufacturing of this sensor.

References

[1] J. Bogaerts, W. Ogiers, T. Cools, W. Diels, “Next Generation CMOS Active Pixel Sensors for Attitude and Orbit Control Systems”, 6th International ESA Conference on Guidance, Navigation and Control Systems, Loutraki (Greece), October 17-20 2005.

[2] J. Bogaerts, G. Lepage, D. Dantès, “High-end CMOS Active Pixel Sensors for Space-borne Imaging Instruments”, Disruption in Space, Marseille, July 4-6, 2005.

[3] J. Bogaerts, B. Dierickx, P. De Moor, D. Sabuncuoglu Tezcan, K. De Munck, C. Van Hoof, “High-end CMOS Active Pixel Sensor for Hyperspectral Imaging”, Proc. 2005 IEEE Workshop on CCDs/AISs, Japan, 2005.

[4] A. Materne, A. Bardoux, H. Geoffray, T. Tournier, P. Kubik, D. Morris, I. Wallace, C. Renard “Backthinned TDI CCD image sensor design and performance for the Pleiades high resolution earth observation satellites”, Proc. ‘6th Internat. Conf. on Space Optics’, ESTEC, Noordwijk, The Netherlands, 27-30 June 2006 (ESA SP-621).

[5] G. Lepage et al., “CMOS long linear array for space application”, Proc. of SPIE-IS&T Electronic Imaging, SPIE Vol 6068, January 2006.

[6] P. Lier, M. Bach , “Parasol a micro satellite in the A-train for Earth atmospheric observations” IAC-05-B5.4.03. 56th Int. Astronautical Congress of the Int. Astronautical Federation, the Int. Academy of Astronautics, and the International Institute of Space Law, Fukuoka, Japan, Oct. 17-21, 2005

[7] A. Materne, C. Buil “Development of a CMOS snapshot active pixel sensor for spaceborne earth observation applications”, Proc. of 1st Symposium on Potentially disruptive technologies, Marseille, France, 4-6 july 2005.

[8] G. Yang and T. Dosluoglu, “Ultra High Light Shutter Rejection Ratio Snapshot Pixel Image Sensor ASIC for Pattern Recognition”, Proc. IEEE Workshop on CCD and Advances Image Sensors, Nagano, Japan, June 9-11, 2005.

[9] Patent pending.

[10] US patent 6,225,670 and 6,545,303.

Variability limits the advantage of a photo diode's zero bias operation

Bart Dierickx[1], [2]

Abstract
In the dark a photodiode is a passive structure. At zero bias it thus exhibits zero leakage (dark) current. This feature is known since ever; in hybrid photovoltaic infrared detectors one exploits it to minimize dark current. In monolithic CMOS or CCD sensors this "trick" is often not applicable as the design freedom to bring the bias voltage at zero volts does not exist.

Note that it is not the dark current itself that we want to reduce, but its related noise and spatial non-uniformity. The goal is thus not to reduce the dark current to zero, on average, but to minimize the spread of the effect of dark current. In this paper we will point out that there *is* a lower limit on the improvement due to variability of the dark current and of the pixel's circuit parts.
The essence of this paper: is it worthwhile doing effort to operate photodiodes at or near zero-bias? At first sight, reducing the photodiode's bias voltage to zero is the wonder solution for dark current.

The message is: *Yes*, dark current can be greatly reduced; DSNU and DCSN may decrease too. And *No*, the gain is by far not what you hoped for. In some not-so-extreme operation conditions, it does even more harm than good.

We derive formulas for the basic behavior, which allow estimating the best temperature/integration time/bias voltage working point. These formulas are just tools to understand dependencies. Real prediction requires variability aware analog transient and noise transient simulations.

1 Pixel operation near zero bias

1.1 Leakage current / voltage relation

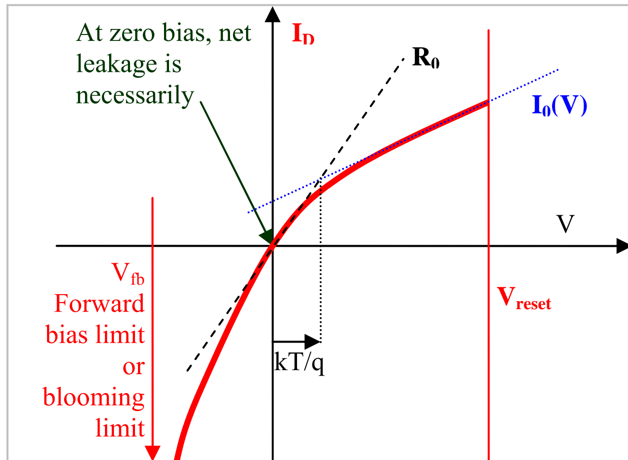


Figure 1 Dark current / voltage relation of a photodiode (arbitrary curve).

The dark current obeys

$$I_D(V) = I_0(V) \cdot \left(1 - \exp(\frac{q.V}{k.T})\right) \quad (1)$$

which yield an expression for R_0 as

$$\frac{1}{R_0} = \frac{\partial I_0(V)}{\partial V} + \frac{q \cdot I_0(0)}{kT} \quad (2)$$

$$I = I_{ph} + I_D(V) \approx I_{ph} + \frac{V}{R_0} \quad (3)$$

1.2 Photo response near zero-bias

$$Q_D = (V_{reset} - V) * C = \int I_D(V) \partial t \quad (4)$$

The integral of (1) and (2) expression fit in (4) and yield:

[1] With IMEC, Leuven, Belgium. Email: bart.dierickx@imec.be
[2] With Caeleste CVBA, Edegem, Belgium. Email: bart@caeleste.be

$$(V_{reset} - V) * C = \int (I_{ph} + I_0(V) \cdot \left(1 - \exp(\frac{q.V}{k.T})\right) dt \approx \int (I_{ph} + \frac{V}{R}) dt \quad (5)$$

This is a differential equation describing V(t). The solution is (simplifying with a constant R or $I_0(V)$):

$$V(t) = (V_{reset} - V_\infty) * \exp(-\frac{t}{RC}) + V_\infty \quad \text{or} \quad V(t) = (V_{reset} + R * I_{ph}) * \exp(-\frac{t}{RC}) - R * I_{ph} \quad (6)$$

For infinite R, this simplifies to the classic photoresponse expression for the integration of photocurrent:

Take the solution $V(t_{\text{int}}) = (V_{reset} + R * I_{ph}) * \exp(-\frac{t_{\text{int}}}{RC}) - R * I_{ph}$ found here above and let's agree that we shall avoid the regime where the behavior becomes non-linear as function of time, or $t_{int} \ll R.C$. Then:

$$V(t_{\text{int}}) = (V_{reset} + R * I_{ph}) * (1 - \frac{t_{\text{int}}}{RC} + \left(\frac{t_{\text{int}}}{RC}\right)^2) - R * I_{ph} \quad (7)$$

How to interpret (7)? We learn that the photoresponse remains truly linear (caveat: this linearity falls with the assumption that R and C are linear). Integration starts at V_{reset}, but V_{reset} will seemingly shift towards zero as t_{int} becomes significant compared to RC.
The photoresponse itself will decrease as t_{int} becomes significant compared to RC:

Photoresponse in terms of V/A: $\frac{dV(t_{\text{int}})}{dI_{ph}} = \frac{t_{\text{int}}}{C} * \exp(-\frac{t_{\text{int}}}{RC})$ or simplified: $\frac{dV(t_{\text{int}})}{dI_{ph}} = \frac{t_{\text{int}}}{C} * (1 - \frac{t_{\text{int}}}{RC})$ (8)

2 Spatial non uniformity math

Spatial variability of V_{reset}, R and C will translate into spatial offset and gain non-uniformity. In this paragraph the symbol σ() denotes the *spatial, pixel-to-pixel,* non-uniformity of the expression between brackets.

Caveat: the results are based on the linearized relation of Figure 5. This approximation is only valid when operating very close to zero bias.

2.1 Variability of V_{reset}

Take (6) and make it dark. Pixel to pixel variability of V_{reset} will enter the raw pixel voltage V. On-chip CDS or DS can subtract the reset voltage, but will not cancel all non-uniformity due to V_{reset}.

$$V(t_{\text{int}}) - V(t = 0) = V_{reset} \cdot \left(\exp(-\frac{t_{\text{int}}}{RC}) - 1\right) \quad (9)$$

I.e. spatial Variability of V_{reset} enters the pixel signal as an offset non-uniformity (ONU).

$$ONU_{VR} = \sigma(V_{reset}) . \left(1 - \exp(\frac{t_{\text{int}}}{RC})\right) \quad (10)$$

2.2 Variability of the photo diode leakage resistance R

Take (7). After CDS or DS and keeping only first order terms in R it becomes:

$$V(t_{\text{int}}) - V(0) = -\frac{1}{R} . \frac{V_{reset} . t_{\text{int}}}{C} + \frac{1}{R} . \frac{I_{ph} . t_{\text{int}}}{C} . \left(\frac{t_{\text{int}}}{C}\right) \quad (11)$$

Differencing to R yields the sensitivity to variability of the signal voltage to variation of R. The first term results in an offset non-uniformity (ONU) that is proportional to t_{int} and thus behaves mathematically as the classic DSNU. The second term is a spatial gain non-uniformity (GNU) that is proportional to I_{ph}, hence it behaves mathematically equal to classic PRNU, *yet* the error is not a pixel constant as with classic PRNU, but a factor that grows linearly with (t_{int}). These offset and gain non-uniformities are mathematically:

$$ONU_R = \frac{\sigma(R)}{R} . \frac{V_{reset} . t_{\text{int}}}{R.C} \quad \text{and} \quad GNU_R = \frac{\sigma(R)}{R} . \frac{t_{\text{int}}}{R.C} \quad (12)$$

The spatial non-uniformity of the leakage current or leakage resistance translates to a form of PRNU. As a rule of thumb this formula teaches that, in order to keep this contribution below the already existing 1..2% PRNU, we need $PRNU_{@LARGE_BIAS} > \frac{\sigma(R)}{R}.\frac{t_{\text{int}}}{R.C}$. As σ(R)/R is close to unity, this means that one should operate the image sensor in practice in the regime t_{int} smaller than a few % of R.C. This means that image quality may severely degrade at long integration times, exactly the opposite of what one tried to improve with lowering the bias, unless software PRNU correction can be applied.

2.3 Variability of the photo diode capacitance C

Starting from (11) one can now difference to C, yielding:

$$GNU_C = \frac{\sigma(C)}{C} \quad \text{i.e. the classic PRNU, and} \quad ONU_C = \frac{\sigma(C)}{C}.\frac{V_{reset}.t_{\text{int}}}{C.R} \tag{13}$$

3 Dark current shot noise near zero bias

Usually the temporal noise associated to dark current is simplified to be dark current shot noise. DCSN charge is the square root of the number of electrons dark current. Dark current $I_D(V)$ near zero bias, from [3]:

$$I_D(V) = I_0(V)\cdot\left(1-\exp(\frac{q.V}{k.T})\right) \tag{14}$$

Which consist of the “reverse bias” $I_0(V)$ dark current, itself voltage dependent, and an opposite diffusion current that becomes important near zero bias (V<kT/q). Both terms independently exhibit shot noise. Thus, although the net I_D is zero at zero bias, one has two independent sources of shot noise with spectral density:

$$S_I(f) = 2.q.I_0(V) + 2.q.I_0(V)\cdot\exp(\frac{q.V}{k.T}) \tag{15}$$

Assuming that t_{int} is always far below the bandwidth of the shot noise then

$$Q_{DCSN} = \sqrt{\frac{I_0(V).t_{\text{int}}}{q}\cdot\left[1+\exp(\frac{q.V}{k.T})\right]} \tag{16}$$

Observations on this formula:

1. The formula predicts that DCSN steeply increases at slight forward bias. This applies equally if this forward bias is due to photocurrent. In that case the photon shot noise power can double as if the photodiode were a photoresistor.
2. In an idealized photodiode $I_0(V)$ is a constant; then DCSN at zero bias is $\sqrt{2}$ times the large bias value. Real diodes might not obey this simplification
3. $I_0(V=0)$ is in fact an unmeasurable value. In the remainder of this text we assume that $I_0(0)$ is known.
4. The formula is in no way exact, as during integration, the diode voltage will travel from V_{reset} towards 0.
5. At large bias (V>>kT/q) the expression becomes equal to the classic expression for DCSN.

4 Summary

Is it worthwhile doing effort to operate photodiodes at or near zero-bias? The real goal of reducing dark current is reducing DSNU and DCSN. If dark current becomes zero on the average, but has large spatial non-uniformities or temporal noise as side effects, then we have gained nothing.

Table 1. In the following table we compare the photodiode related contributors for DSNU, PRNU and DCSN. Note that the low bias operation involves more but likely smaller contributors.

Contributor	High bias operation	Low /zero bias operation

[3] A. van der Ziel, "Noise in Solid State Devices and Circuits", John Wiley & Sons, New York, New York, p. 93-95, 1986

DSNU-like [mV_{RMS}]		$ONU_{VR} = \sigma(V_{reset}).\frac{t_{\text{int}}}{RC}$
	$ONU = \sigma(I_D).\frac{t_{\text{int}}}{C}$	$ONU_R = \frac{\sigma(R)}{R}.\frac{V_{reset}.t_{\text{int}}}{R.C}$
		$ONU_C = \frac{\sigma(C)}{C}.\frac{V_{reset}.t_{\text{int}}}{C.R}$
PRNU-like [$\%_{RMS}$] Only the fraction due to the photodiode	$GNU = \frac{\sigma(C)}{C}$	$GNU_C = \frac{\sigma(C)}{C}$
		$GNU_R = \frac{\sigma(R)}{R}.\frac{t_{\text{int}}}{R.C}$ (*)
Dark current shot noise DCSN [e^-_{RMS}]	$Q_{DCSN} = \sqrt{I_D.t_{\text{int}}/q}$	$Q_{DCSN} = \sqrt{\frac{I_0(V).t_{\text{int}}}{q}\cdot\left[1+\exp(\frac{q.V}{k.T})\right]}$

4.1 Example

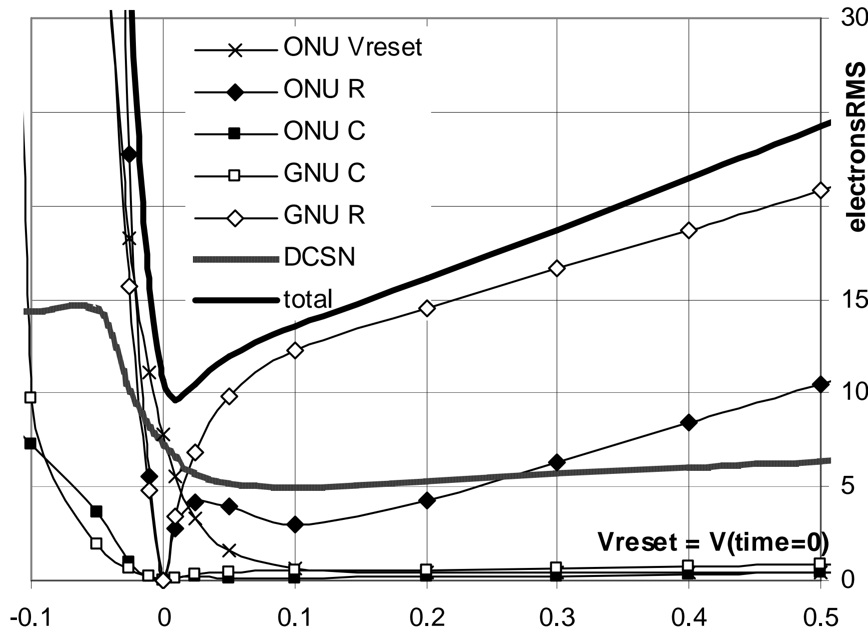


*Figure 2 ONUs, GNUs and DCSN in electrons$_{RMS}$ based on the formulas in table 1, for following parameters and operating conditions: dark, , t_{int}=10sec,σR/R=50%$_{RMS}$, $I_0(V)$=[2e$^-$/s]*1+V/500mV, σC/C=2%$_{RMS}$, σV_{reset}=10mV$_{RMS}$, C=1fF=160 uV/e$^-$,*

The optimal operating point is a slight reverse bias; if all spatial non-uniformity can be calibrated the optimal operating point depends solely on DCSN, V=1V in this example.

5 Conclusions & recommendations

1. Zero bias or near zero bias operation yields a significant reduction of the dark current but just a limited reduction of dark current induced noise and non-uniformity.
2. Its associated spatial non-uniformity effects behave like DNSU and time/temperature dependent PRNU.
3. A serious limitation is that the non-uniformity of the leakage resistance translates to an excess PRNU that becomes dominant when the integration time becomes longer than a few % of the auto-saturation time. However this limitation should not stop one to pursue operation at lower bias.
4. Another important issue is the low full well charge; this may be solved by special technology enhancements or by living with the high photon shot noise. One must anticipate having to work with very low full well charges, in the order of a few 1000 electrons or less
5. When we assume that all effects than can be calibrated are calibrated, in the end we will remain stuck with only the dark current shot noise contribution. In order to avoid a steep increase of shot noise due to forward diffusion, one must stay clear of zero bias operation by a few kT/q.

Super Small, Sub 2µm Pixels for Novel CMOS Image Sensors

G.Agranov, R.Mauritzson; S.Barna, J.Jiang, A.Dokoutchaev, X.Fan; X.Li

Micron Technology, Inc., 8000 S. Federal Way, Boise, Idaho 83707-0006
Tel: 208-368-4268, Fax: 208-368-4660, gagranov@micron.com

Abstract

Pixel shrink is a driving force for novel CMOS image sensor development used in mobile and DSC applications. This paper describes the latest results in super small, sub 2µm pixel development at Micron Technology, Inc. Presented are results of optical and electrical characterization of super small pixels and their respective pixel arrays. The paper considers general light signal characteristics, spectral characteristics, quantum efficiency and crosstalk of super small pixels, and their effect on the final quality and signal-to-noise ratio of the color image post color processing.

1.75µm Pixel Development

Micron demonstrated the first image from a 1.75µm pixel array in June 2005 [1]. In the two years since the first pixel arrays were demonstrated, significant progress has been made in 1.75µm pixel and process development. Several generations of 1.75µm pixels were created over this period of time, and a full line of image sensors with different array sizes (from 1.3Mp through 8Mp) are in production now. This paper will compare optical and electrical characteristics of 1.75µm pixels used in the first and current generations of pixel arrays and image sensors.

To date, Micron's development of the 1.75µm pixel has been focused on using our common element pixel architecture (CEPA) with 1.75- and 1.5-equivalent transistors, per pixel. Early 1.75µm pixel generations utilized asymmetrical pixel structures, enabling a high conversion gain of the floating diffusion (up to 115uV/e for the 4-way CEPA), large photodiode fill factor, and a large pixel capacity (up to 9200 electrons for the linear full well). Current pixel designs focus more on symmetrical pixel architectures where metal openings and photodiodes are equally spaced for pixels within different color planes. Symmetrical architectures simplify pixel shading and color distortion compensation at the system level; however, keeping the same level of pixel performance in regards to fill factor and pixel capacity becomes a significant challenge. This is partially resolved by using an advanced 95nm manufacturing processes for the pixel array. Figure 1 presents photodiode fill factors and pixel capacities for different revisions of Micron's 1.75µm pixel. The square, triangle, and circle data points represent versions of the pixel with an asymmetrical, quasi-symmetrical, and practically fully symmetrical design. Solid data points represent pixel capacity, and hollow data points - fill factor. Arrows at the bottom of the plot indicate manufacturing process nodes used for the respective pixel designs. As can be seen from the plot, the latest pixels with a symmetrical design achieve similar fill factor and pixel capacity to their asymmetrical predecessors - 43% fill factor and 9200 electrons for the linear full well.

Quantum efficiency and crosstalk are two of the most important pixel characteristics that significantly affect sensitivity, general image quality, and signal-to-noise ratio after color processing. Optimization of the pixel was accomplished in several aspects: optimization of the optical path of the pixel, optimization of the pixel design/architecture, and optimization of the Si substrate. Optimization of the pixel optical path includes an advanced aluminum process with a reduced stack height of dielectric layers, a gapless microlens process, optimized metal routing, and embedded anti-reflective coatings. The total stack height between microlens and Si surface for the optimized process was reduced to less than 3.2µm, which provides a large-pixel acceptance angle of light as well as the ability to work with low-profile lenses with chief ray angles up to 27 degrees. By utilizing an advanced aluminum metal process, Micron eliminated the need to remove any light inhibiting diffusion barrier layers associated with copper processing. Figure 2 presents the results of a wave propagation simulation for the 1.75µm pixel with an optimized optical path for green light (550nm). As can be seen from the picture, light is well confined by pixel optics into the photodiode area. The pixel exhibits a large acceptance angle of light - signal degradation is less than 20 percent for angles of incident light up to 25 degrees.

Optimization of the Si substrate was conducted by using both traditional p-substrate and n-substrate approaches. N-substrates significantly reduce electrical crosstalk by collecting and sinking carriers that are created with deep absorbed photons. Use of n-substrates also reduces dark current from the substrate. However, reduced thickness of p- EPI above the n-substrate can degrade QE for green and red pixels, resulting in degradation of overall sensitivity. Thus, optimization of the thickness of the p- EPI layer needs to be done to assure optimal trade off between quantum efficiency and crosstalk from the SNR after color processing stand point. Resulting experimental spectral response data for the p-substrate and n-substrate versions of a 1.75µm pixel currently in production are presented in Figure 3a and Figure 3b, respectively. These figures present both spectral response and crosstalk data calculated according to [2]. The p-substrate version of the pixel QE maximum is equal to 42%, 45%, and 38% for blue, green, and red pixels respectively. The n-substrate version of the pixel has QE maximum equal to 42%, 37%, and 29% for blue, green, and red pixels respectively. As will be shown later, in spite of the slight degradation of QE for the n-substrate version of the pixel, overall sensitivity of the sensor after color processing becomes higher due to a significant reduction of electrical crosstalk. Also, the n-substrate version of the pixel exhibits higher SNRmax when compared with the p-substrate pixel at the same full well capacity due to lower crosstalk. For comparison purposes, the earliest generations of 1.75µm pixels on the p-substrate exhibited QE maximum of 28%, 36%, and 23% for blue, green, and red pixels respectively. The progress in pixel development resulted in about a 50% improvement in QE and a 40% improvement in crosstalk. Note that n-substrates may not provide an advantage for all pixel sizes, and the benefit of n-substrates becomes more advantageous in

regards to pixel optimization/performance as pixel become smaller and electrical crosstalk increases.

Table 1 summarizes the performances of 1.75µm pixels currently in production and compares them with earlier generations of the pixel. Figure 4 presents estimations of luminance SNR after color processing as a function of light intensity on the scene for the following conditions: integration time, 67ms; lens F-number, 2.8; lens transmittance, 0.9; reflectance of the scene, 18%; IR-cut filter, 650nm; and color saturation, 100%. As can be seen from the plot, current pixels in production provide (2x – 3x) improvement of SNR when compared to the earliest pixel generations. For these same pixels, a n-substrate version of the pixel provides ~10% improvement in sensitivity over the p-substrate version using the conditions specified above, as well as higher SNRmax at the same full well capacity. The improvement of SNR from n-substrates is more pronounced for higher color saturation.

1.4µm and 1.2µm Pixel Development

To address the market needs of the mobile and DSC imaging, Micron continues to advance pixel technology in support of new CMOS image sensor product lines, including 1.4µm and 1.2µm pixel sizes. Reduction of pixel size to these small values requires advanced manufacturing processes and creative pixel designs, and has been a significant challenge for all aspects of pixel development. Similar to the 1.75µm pixel, development of smaller pixels continues to focus on improvements in the pixel optical path, increasing QE and pixel capacity, and reducing crosstalk. Pixel designs are based on CEPA with 1.5 equivalent transistors per pixel. Micron successfully built a pixel array with its first generation of 1.4um pixel, and demonstrated a color image of reasonable quality and pixel performance. Figure 5 presents an example of a color image from a 1.4µm pixel array. The pixel achieves 6000 electrons linear full well capacity, quantum efficiency close to 30%, and readout noise less than 2e.

Pixel design for the 1.2µm pixel is also based on CEPA with 1.5 equivalent transistors per pixel. Early indications show the ability to achieve 4000 electrons for the linear full well capacity, quantum efficiency of 30%, and readout noise of less than 2 electrons.

Image Quality and Pixel Performance Trade Off – Pixel Arrays with Super Small Pixels

In spite of the big challenges in shrinking pixel sizes below 2µm and 1.5µm, camera miniaturization continuously drives development of image sensors in this direction. The natural questions that are typically raised in regards to this are: What is the trade off between the pixel performance and image quality of a sensor with super small pixels? What level of image quality can be expected from pixel arrays with such super small pixels? These questions have stimulated many interesting ideas, and are actively being discussed in relation to generating good quality images using pixels with limited performances [3]. This paragraph presents the concept of equal optical format for equal image quality and considers the reasoning for pixel scaling from the image quality stand point.

In general, pixel arrays with the same optical format, but a different density of pixels (and pixel size), should provide the same sensitivity, if SNR of the pixel is scaled proportionally to the pixel area. Moreover, a pixel array with smaller pixels will have an advantage of higher spatial resolution when the light intensity on the scene is high enough. If pixel SNR is scaled proportionally to the pixel area, integration of photons over the pixel area is substituted with spatial integration in the pixel array, resulting in similar or better sensitivity. To keep SNR scaled to the pixel area when shrinking pixel size, the correspondent trade-off between pixel performances needs to be established. For example, for photon shot limited sensitivity, an increase of crosstalk has to be compensated by an increase in quantum efficiency. The same logic can be applied to the scaling of readout noise and pixel capacity. Also, the reduction of pixel capacity when the pixel shrinks can be overcome with the high dynamic range approach. Based on this simplified consideration, the following conclusions can be made:

- ✓ as the pixel shrinks, image sensors with equal optical format provide the same sensitivity as long as pixel SNR is scaled proportionally to pixel area;
- ✓ pixel arrays with a smaller pixel size and higher density of pixels can potentially provide better image quality due to better spatial resolution;
- ✓ when targeting the same image quality, a pixel can shrink until pixel SNR is proportional to the pixel area;
- ✓ provided all of the scaling is observed, pixel size reduction makes sense as long as increased spatial resolution can be achieved.

To illustrate above considerations, we have estimated normalized SNR for pixels with varying sizes developed at Micron over the past several years. Figure 6 presents the normalized per-pixel area scene light intensity, providing luminance SNR equal to 10 for Micron's pixels with different sizes. (Conditions correspond to those used earlier for Figure 4.) As can be seen from the plot, the 1.75µm pixel has a normalized SNR equal to or very close to those pixels larger in size, and respectively will provide similar sensitivity as those larger pixels in the same optical format. Figure 7 presents an example of an image taken under bright light conditions (1000 lux) and under low light conditions (1 lux, 200ms integration time) using Micron's image sensors with identical optical formats: A ¼-inchVGA image sensor with 5.6µm pixel (on the left), a ¼-inch 2Mp image sensor with 2.2µm pixel (at the center), and a ¼-inch 3Mp image sensor with 1.75µm pixel (on the right). As can be seen from the zoomed fragments, sensors with smaller pixels, as expected, provide better spatial resolution at bright light. At the same time, in spite of a large difference in the pixel area, image quality and low light sensitivity of the sensors with these smaller pixels is comparable with a 5.6µm pixel-based imager.

Conclusion

In summary, Micron sensors have achieved "scaled" performance, preserving sensitivity and SNR performance when compared to similar optical format sensors, but with the added benefit of higher spatial resolution as the pixels shrink. We have achieved this by using process and architecture-optimized, symmetrical, n-substrate pixels. Maintaining this "scaled" performance as we drive towards super small pixels, perhaps even 1 micron pixels, poses a challenge for the CMOS imaging industry.

Acknowledgements

The authors would like to thank many people in Micron Technology for their support and contribution to this investigation.

References

[1] G.Agranov et al, IEEE, CCD - AIS WS, 2005, pp. 206-209
[2] G.Agranov et al, Trans. ED, ED-50, 2003, pp.4-11
[3] E.R.Fossum, IEEE, CCD - AIS WS, 2005, pp. 214-217

Table 1

1.75um pixel	Current pixel		1st gen
	p-sub	n-sub	
Responsivity (FD), V/(lux*s)	0.70	0.57	0.45
QE max, %			
blue	42	42	28
green	45	37	36
red	38	29	23
Color crosstalk, %	24.8	17.0	33.0
Pixel capacity(linear), e	9200	9200	7000

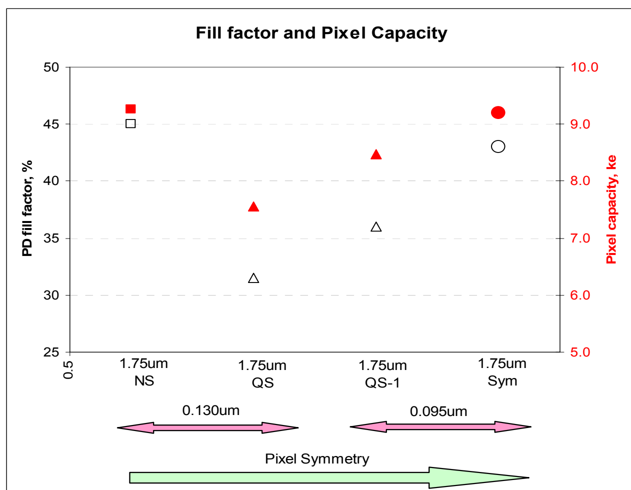


Figure 1. Fill factor and pixel capacity (linear full well) for different versions of 1.75µm pixel. Square, triangle, and circle data points represent asymmetrical, quasi-symmetrical, and symmetrical pixel. Solid and hollow data points correspond to pixel capacity and fill factor respectively.

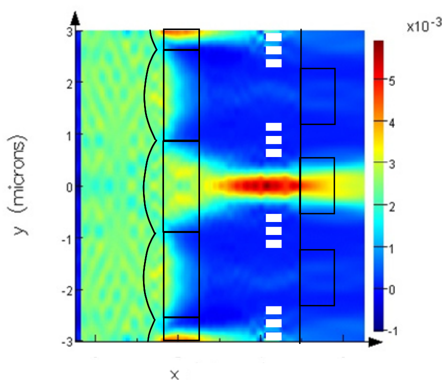


Figure 2. Wave optics simulations. Light intensity distribution of the 550nm light with normal incidence on cross-section of blue-green 1.75µm pixel.

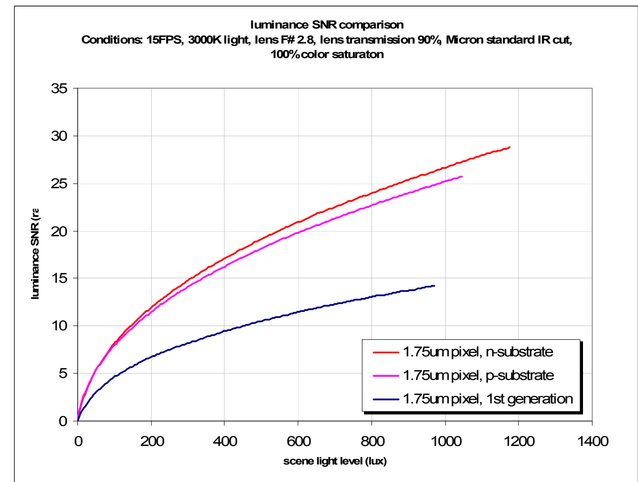


Figure 4. Luminance SNR after color processing for current 1.75µm pixels on p-substrate and n-substrate in comparison with 1st generation of 1.75µm pixel (series order corresponds to the legend).

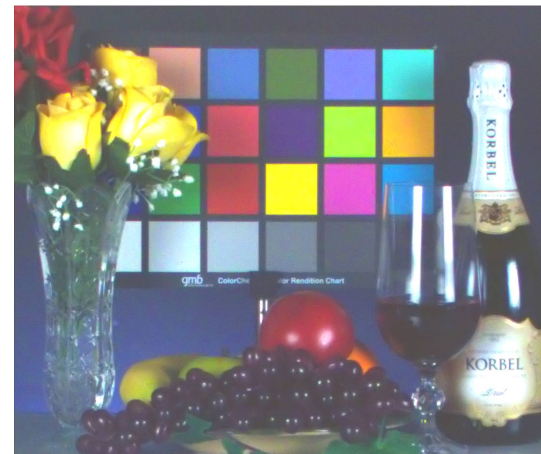


Figure 5. Example of image from 1Megapixel array with 1.4µm pixel

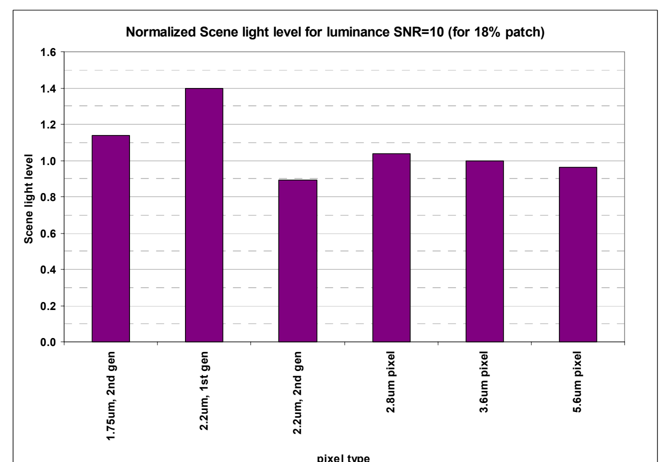
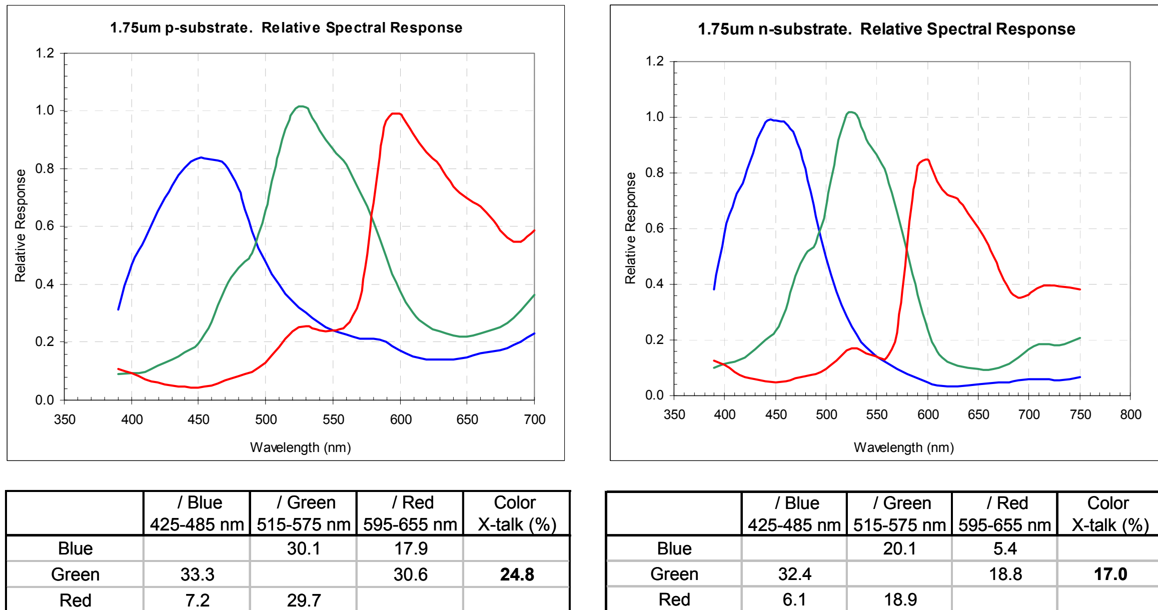


Figure 6. Normalized per-pixel area light intensity level for luminance SNR = 10 after color processing.



	/ Blue 425-485 nm	/ Green 515-575 nm	/ Red 595-655 nm	Color X-talk (%)
Blue		30.1	17.9	
Green	33.3		30.6	**24.8**
Red	7.2	29.7		

	/ Blue 425-485 nm	/ Green 515-575 nm	/ Red 595-655 nm	Color X-talk (%)
Blue		20.1	5.4	
Green	32.4		18.8	**17.0**
Red	6.1	18.9		

Figure 3. Relative response and crosstalk data for 1.75µm pixel on p-substrate (left) and n-substrate (right).

Figure 7. Images from sensors with the same optical format (1/4-inch) but different pixel size at bright light and low light conditions.

Stratified Photodiode a New Concept for Small Size-High Performance CMOS Image Sensor Pixels

Younsub Lim, Kyunglak Lee, Heejeong Hong, Jaeyeong Kim, Seunghoon Sa, Juil Lee, Daebyung Kim, and Jerry Hynecek
MagnaChip Semiconductor Ltd.1 Hyangjeong-dong, Heungdeok-gu, Cheongju-si, Chungcheongbuk-do, 361-725 Korea; Email : younsub.lim@magnachip.com

ABSTRACT

With continuing trend of pixel size reduction in CMOS Image Sensors from 2.8um through 2.2um down to 1.4um and beyond it becomes increasingly difficult to maintain an adequate pixel charge storage capacity and achieve the required DR and SNR. This paper addresses this problem and describes in detail a solution where charge is collected and stored in two layers located above each other in the silicon bulk in a stratified fashion. An excellent performance is achieved with about 50% well capacity improvement without any penalty of dark current increase. This has been achieved using the pinned PD architecture for both stratified layers and with a careful control of electrical fields. The very low depleted (pinned) voltage, which is typically less than 1.0 V for this structure, allows using high FD voltage swing and this in turn results in an easier and more area efficient design of low noise ADC circuits. The stratified PD is easy to fabricate with high yield, can be incorporated with any 4T pixel readout scheme, and does not require any special clocking or biasing.

INTRODUCTION

CMOS Image Sensors (CIS) have been used in a wide range of applications such as the digital still cameras and cellular mobile phones having clear advantages over the CCDs in terms of low power consumption, on-chip functionality, low cost, and so on [1]. However, as the pixel size shrinks, CIS are facing some limitations in both the low Signal to Noise Ratio (SNR) and Dynamic Range (DR), which leads to a degradation of image quality and reduction of usable full range of illuminations in the real world applications. Both the DR and the maximum SNR can be improved simultaneously by increasing the well capacity of the pixel. The well capacity is represented by the following formula: $Q_{PD} = (V_{pinning} - V_{blooming})C_{PD}$, where $V_{pinning}$ is the pinning voltage and $V_{blooming}$ is the blooming voltage of the pixel. C_{PD} is the capacitance of the PD. The reduction of $V_{blooming}$ is limited by the minimum voltage required for stopping the photo-generated electrons from overflowing into the silicon substrate during high illuminations. Therefore, to increase the well capacity of the pixel, $V_{pinning}$ or C_{PD} should be increased. However, it is very difficult to increase the charge storage capacitance as the pixel size shrinks, although some progress has been made by introducing the shared pixel concept to maximize the geometrical fill factor [2, 3]. Another problem typically encountered with the pixel size reduction is the image lag due to the increased n-type doping of PD. The higher doping is necessary to compensate for the reduction of full well capacity caused by the smaller PD area. In general, $V_{pinning}$ is proportionally increased with the increase of the full well capacity. This requires reduction of the maximum voltage swing on the Floating Diffusion (FD) in order to achieve a complete charge transfer of charge stored in the PD. Therefore, to improve or preserve the image lag performance and to obtain higher FD voltage swing resulting from higher full well capacity, $V_{pinning}$ should not be increased.

STRATIFIED PD CONCEPT DESCRIPTION

In this paper, a new PD structure is introduced as a solution to the above mentioned limitations resulting from the smaller pixel size. The new PD structure, called the stratified PD, has two n-type implant regions located above each other in the silicon bulk in a stratified fashion where charge is collected and stored. The drawing in Fig.1 shows the concept of the stratified PD structure. The surface of the PD is covered with a high p+ doped implant layer similarly as in the conventional pinned photodiode. This is necessary for minimizing the dark current generation from the interface states present at the Si-SiO2 interface. The conventional underlying n-type region is divided in this PD into two n-type regions (DN1, DN2) by a highly doped p+ layer (Insertion-p), which is implanted using an additional mask. The new mask is aligned to the edge of the transfer gate at a distance (X) and overlaps the STI region at the PD edge. The distance X is optimized to minimize the electric filed at the interface of the PD with the transfer gate and to provide the electrical connection between the DN1 and DN2 regions. The DN1, the Insertion-p, and a portion of the DN2 are implanted using the same Insertion-p mask. The rest of the DN2 is implanted using the conventional n-type PD mask. The two stratified n-type regions, which are electrically connected through the additional n-type implant, also help to extend the PD depletion depth without any degradation of image lag. In the stratified PD, the Insertion-p layer plays a very important role to increase the full well capacity and to increase the

depletion region depth. The structure can be modeled by two parallel connections of storage sites in a silicon substrate [4]. The Insertion-p layer essentially acts as an electrode between the two n-type PD regions and thus it has to have adequate electrical connections to the channel stop (NCST) p+ doped region and to the surface p+ doped region. The layer also cannot be depleted of holes when the transfer gate is turned on. For these reasons it is fabricated using a relatively high dose p-type implant, which covers both the PD and STI regions. The DN2 region contributes the major portion of the PD capacitance. The DN1 region adds PD capacitance and is formed using high implantation energy of 300keV~500keV with a medium dose. The simulated doping profile in the direction of the Si depth at the center of the stratified PD is shown in Fig.2. The electrostatic potential profiles after 1.0usec from the time when Tx gate is turned on (V_{op} = 2.8V) for the conventional and stratified PDs are shown in Fig.3. This is calculated using the 2D transient simulation. The Insertion-p layer occupies a very small region and does not deplete of holes at V_{op} = 2.8V as indicated by the narrow potential line in Fig.3. The profile also does not indicate any potential barriers for the electron transfer from the PD to FD. This is due to a careful optimization of all implants. Implementation of the PD with extended depletion region is important for minimizing of electrical crosstalk induced by the minority carrier diffusion and for maximizing of Quantum Efficiency (QE). The depth of the maximum potential of conventional PDs has an inverse relation to the maximum Qsat for the minimum image lag performance. So, in general, the high full well capacity and high depletion depth are mutually contradicting requirements. The stratified PD structure makes it possible to overcome this trade-off. The simulation results show the depletion depth of the stratified PD to be 0.3-0.4 um deeper than that of the conventional PD with about 50% improvement in full well capacity. The pixel sensitivity and crosstalk tend to degrade as the pixel size shrinks. The optical diffraction and the minority carrier diffusion are the major contributors to this trend. In order to improve the electrical crosstalk a thinner epi is usually very effective for this purpose. However, the sensitivity in this case is also reduced since both the crosstalk signal and the intended signal are lost. The deeper electrical isolation of pixels can be a solution to this problem, but this suffers from the reduction of PD depletion area in the pixel in horizontal direction and the corresponding loss of saturation well capacity. The increased depletion region of the stratified PD contributes to the improvement of both the electrical crosstalk and the sensitivity at the same time. The electrical crosstalk and the pixel response were simulated using a group of pixels where the center one was illuminated and the adjacent ones were blocked by a metal layer. As shown in the graphs in Fig.4 the total response of the stratified PD is about the same as that of the conventional PD, but the response of the illuminated pixel has a significant improvement in longer wavelengths. This is mainly due to the reduction of electrical crosstalk.

EXPERIMENTAL RESULTS

The pixel level performance of the stratified PD pixels was evaluated by characterizing the MagnaChip 2.0 Mega-pixel CMOS image sensor that has 2.2um x 2.2um pixel size and two-way shared pixel architecture. The sensor is being fabricated using the 0.13um technology node. Fig.5 shows the graphs of the measured photon transfer curve for each PD structure. The full well capacity of the stratified PD is approximately 50% higher than that of the conventional PD. Linear Qsat of the conventional PD is about 9800e- and that of the stratified PD is about 14600e- without any help from the pixel bias boosting circuits. Conversion gain is approximately 75uV/e-. The pinning curve of the stratified PD is shown in Fig.6. The curve is obtained from the test structures where the transfer gate bias is swept. $V_{pinning}$ of the stratified PD is about 0.9 V, which is significantly lower than 1.35 V of the conventional PD. The high Qsat and low $V_{pinning}$ of stratified PD improve the FD voltage swing and thus increase the maximum SNR without any degradation of image lag. Fig.7 shows the graph of the photo-electric conversion characteristics of the stratified PD for low light illumination levels. In comparison with the conventional PD the stratified PD shows no difference in the charge transfer efficiency or image lag despite of having much higher full well capacity. Good photo-electric conversion linearity and no image lag suggest that a complete charge transfer is achieved. In Fig.8 the graphs of the dark signal distribution for the integration time of 100msec and 450msec are compared for the conventional and stratified PDs. The temperature of the test is 60°C. The hot pixel count of the stratified PD is lower than that of the conventional PD although the maximum levels are the same. The reduction in hot pixel count results in the improvement of the average dark current. The measured dark current is 103e-/sec@60°C for the stratified PD and 125e-/sec@60°C for the conventional PD. This improvement is mainly due to the reduction of high electric fields at the boundary of the PD and the transfer gate and the presence of the high dose Insertion-p layer, which strengthens the isolation between the n-type PD and STI. Fig.9 shows the graph of measured spectral response of the conventional and stratified PDs. As it is expected from simulations, the wider depletion region of the stratified PD results in a lower crosstalk with enhanced quantum efficiency particularly in the longer wavelength region. The measured overall crosstalk of the stratified PD is approximately 4% lower than that of the conventional PD. The improvement of QE for each B/G/R is approximately +1% / +2% / +3% respectively. The key optical and electrical characteristics of the conventional and stratified PDs are summarized in Table I.

CONCLUSIONS

In this paper, we have introduced a new PD structure called the stratified PD as a solution to overcome the limitations of small size pixels. High full well capacity, improved SNR, very low $V_{pinning}$, and low crosstalk performance were achieved simultaneously without any degradation of dark current and image lag performance.

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REFERENCES

[1] E. R. Fossum, *SPIE*. Vol. 1900, pp. 2-14, July 1993.
[2] M. Mori, et al., *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2004
[3] H. Takahashi et al., *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb., 2004. [4] J. Lee, et al., US Patent NO. 6,489,643

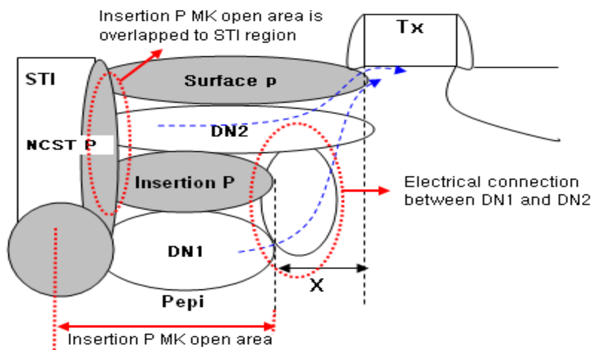


Fig.1. Schematic diagram of the stratified PD structure

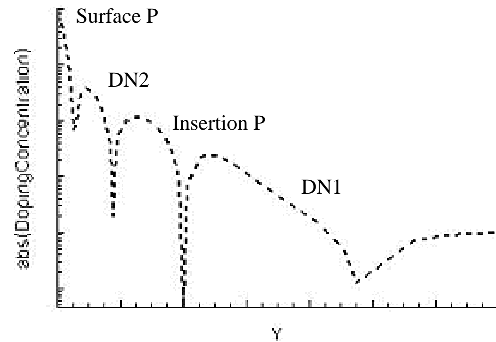


Fig.2. Doping profile at the center of the stratified PD

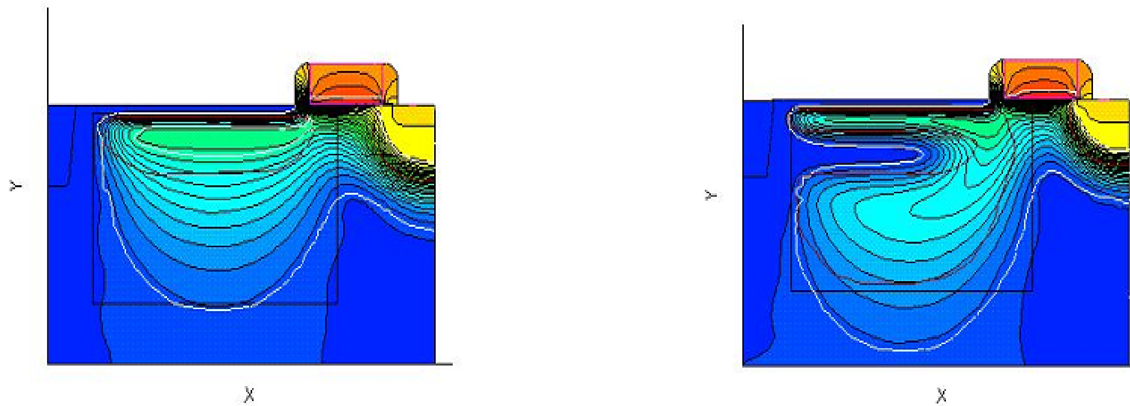


Fig.3. Electrostatic potential profiles after 1.0usec from the Tx turned on for a Conventional PD and Stratified PD

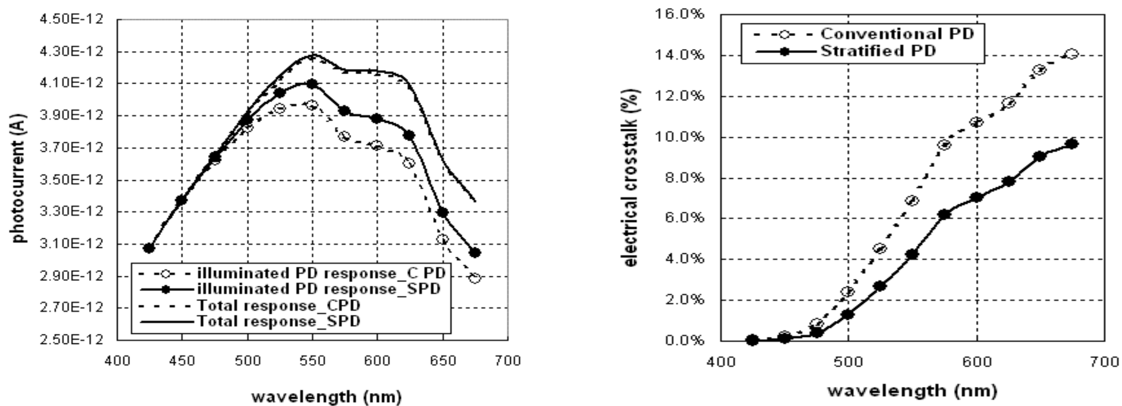
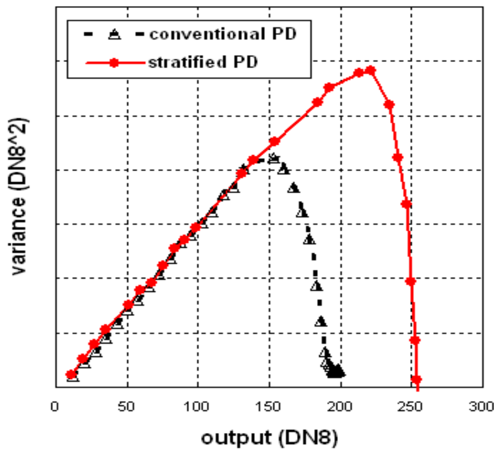


Fig.4. Simulated pixel response and electrical crosstalk (Conventional PD_CPD vs. Stratified PD_SPD)



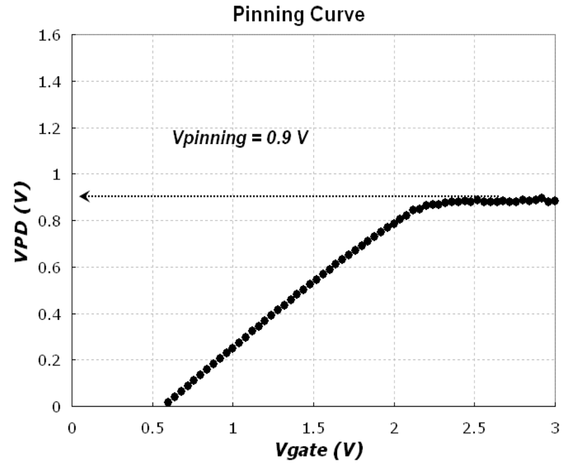
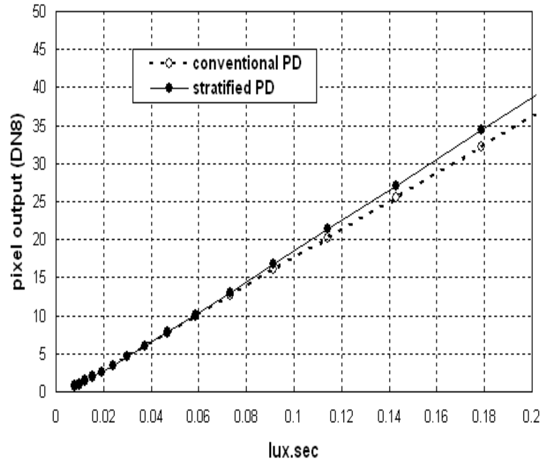


Fig.5. Measured photon transfer curves for the conventional PD and for the stratified PD.

Fig.6. Pinning curve for the stratified PD.



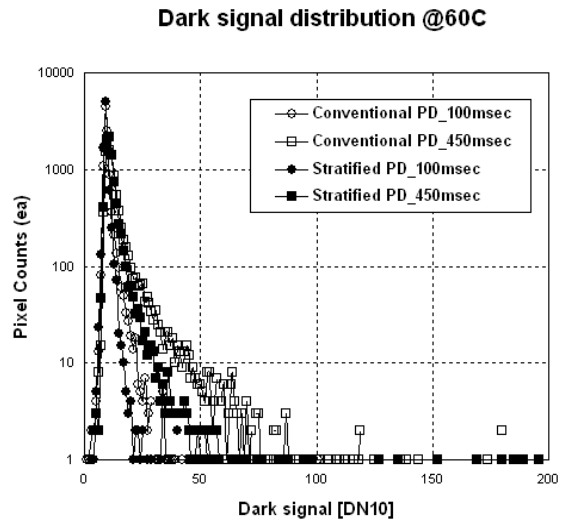


Fig.7. Photo-electric conversion under low illumination.

Fig.8. Dark signal distribution @ Temp = 60°C.

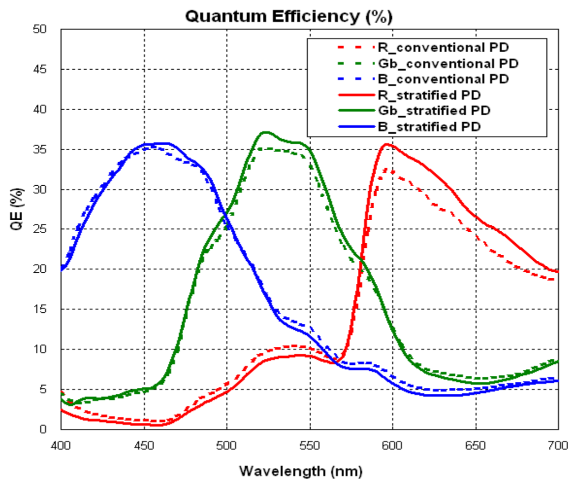


Table I: MagnaChip 2.2um 2 Mega pixel sensor key optical and electrical characteristics.

	Conventional PD	Stratified PD
G Responsivity (FD)	7650 e-/lux.sec	7850 e-/lux.sec
Quantum efficiency (G)	35%	37%
Pixel capacity (linear range)	9800 e-	14600 e-
Peak SNR	39.9 dB	41.6 dB
noise floor @max gain	6e-	6e-
Pixel dynamic range	64.3 dB	67.7 dB
Dark current (@60°C)	125 e-/sec	103 e-/sec
Pinning voltage (V)	1.35 V	0.9 V
Conversion Gain	75 uV/e- (Cfd = 2.15 fF)	

Fig.9. Measured spectral response of conventional and stratified PD.

Improved Design of 1T Charge-Modulation Pixel Structure for Small-Size and Low-Dark-Current Achievements

Arnaud Tournier[1,2], François Roy[1], Guo-Neng Lu[2], Benoît Deschamps[1]

[1] *STMicroelectronics, 850, rue Jean Monnet – F-38926 Crolles Cedex – France*
Tel: +33 4 76 92 51 43 Fax : +33 4 76 92 68 14 E-mail: arnaud.tournier@st.com
[2] *Université de Lyon; Institut des Nanotechnologies de Lyon INL-UMR5270, CNRS, Université Lyon 1, Villeurbanne, F-69622, France.*

Abstract

A ring-gate design of 1T (single-transistor) charge-modulation pixel structure is proposed. It obviates the need to employ STI (shallow trench isolation) for avoiding crosstalk. This enables achievements of smaller pixel size and/or higher fill factor. It also reduces dark current by limiting peripheral leakage current contribution and minimizing band-to-band tunneling effect. A test chip integrating an array of 1.4µm-pitch, 50%-fill-factor pixels is designed in a 0.13µm CMOS technology. The measured pixel characteristics are compared with those from a 2.2µm-pitch, 46%-fill-factor previous design (also in a 0.13µm CMOS process). The comparison shows that the 1.4µm-pitch ring-gate pixel has an improved conversion gain (CG) and a degraded full well capacity (FWC). It also shows substantial reductions on dark current, temporal noise and FPN. The resulting signal-to-noise ratio outweighs degradation of FWC, which also improves dynamic range.

1. Introduction

There have been rapid developments on CMOS image sensors to meet requirements of the fast growing market. Important R&D efforts have been focused on pixel-pitch reduction for higher image resolution and/or higher density of integration. In this miniaturization race [1]-[3], one effective approach consists in employing fewer transistors for active pixel sensors (APS) by sharing pixel components. This has led to suggestions of 2.5T, 1.75T and 1.5T architectural configurations as well as recent 1.4µm-pitch achievements [4].

Also in the attempt of minimizing the number of pixel components, the 1T charge-modulation pixel structure has been proposed and investigated [5]-[8]. It appears promising for pixel size reduction, because the pixel contains only a single transistor to combine the pixel operations: photodetection, charge integration, signal readout and reset.

2. 1T Charge-Modulation Pixel Structure

The 1T charge-modulation pixel contains only one NMOS transistor. The transistor structure differs from the conventional one mainly in that it is on a floating P-well with controlled doping profile. A potential well beneath the transistor channel can be formed to store a charge packet (holes) coming from photo-generation of electron-hole pairs. The I-V characteristics of the transistor are thus modulated by the stored charge, which is related to the light intensity received on the sensing surface of the pixel. The basic structure of the 1T charge-modulation pixel is shown in Fig. 1.

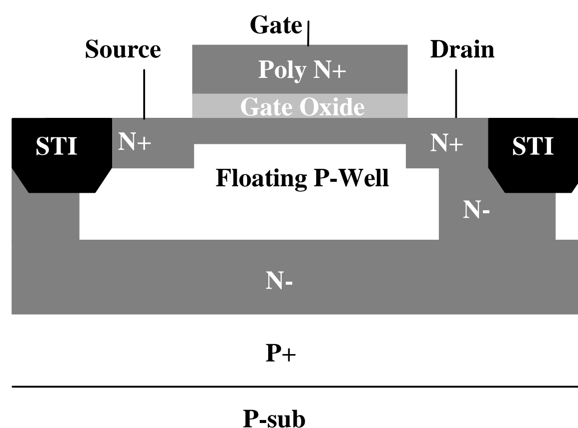


Fig. 1. Cross-section view of the 1T charge-modulation pixel structure

This 1T charge-modulation pixel operates with 3 phases: integration, readout and reset, which can be described as follows.

In the integration phase, a low voltage level is applied to the gate of the transistor to turn it OFF. In such a bias condition the body of the transistor exhibits a potential well in the well region for storing holes (see Fig. 2a). When the pixel is under illumination, light penetrates through the gate and is absorbed in the transistor body. Photo-generated electron-hole pairs are separated due to built-in electrical field in the body. The electrons are swept away mainly to the drain, while the holes are collected and accumulated in the potential well. The stored positive charge increases the potential of the transistor body, leading to a decrease of the transistor threshold voltage V_{th} [7].

In the readout phase, the transistor is switched ON by applying a gate voltage higher than the maximum V_{th} in dark conditions. It operates as a source follower with fixed gate and drain voltages. The decrease of V_{th} reflecting the amount of the stored charge is sensed as an increase of the source voltage. The source voltage is then readout by double sampling to suppress V_{th} dispersion and thus to reduce fixed pattern noise (FPN).

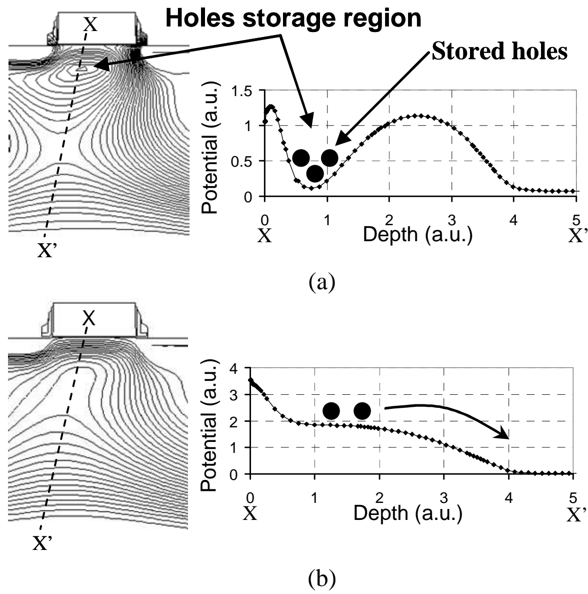


Fig. 2. Simulation with ISE TCAD. a) Potential profile in integration phase forming a well for storing holes; b) Potential profile for reset period with evacuation of stored holes

For the reset of the pixel, a still higher voltage is applied to the transistor gate. At the same time, the source voltage is clamped to the drain voltage to minimize channel current. Under this high gate voltage, the potential profile of the transistor body becomes monotonic decreasing (see Fig. 2b). The potential well disappears and the stored holes are pushed away to the substrate. Fig. 3 shows the timing waveforms of the pixel and sampling signals.

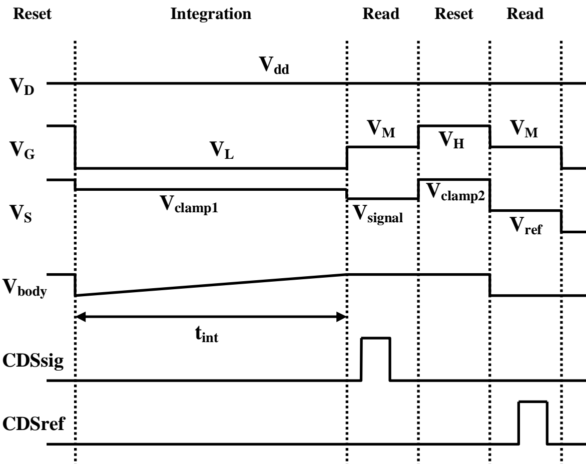


Fig. 3. Timing diagrams

This 1T pixel structure has a conversion gain defined as the pixel output voltage read for each photo-generated and stored hole (in $\mu V/h^+$). It is a key parameter related to performances such as responsitivity and signal-to-noise ratio. By modeling the device operation, it can be expressed as:

$$CG = \frac{qA_v C_{dep}}{C_{ox} C_{B'}} \quad (1)$$

where A_v is the gain of the source-follower slightly lower than unity, C_{dep} is the depletion capacitance under gate between the floating transistor body node B' and the Si/SiO_2 interface, C_{ox} the gate oxide capacitance, and $C_{B'}$ the total body capacitance between node B' and ground. Roughly, with simplifying assumption for $A_v \approx 1$ and $C_{ox} \approx C_{B'}$, the conversion gain can be estimated by:

$$CG \approx q / C_{ox}. \quad (2)$$

Another important parameter of the pixel is its charge-handling capability, also defined as full well capacity (FWC). It corresponds to the maximum amount of charge Q_{sat} that can be stored in the potential well without spread, minus reset residual charge Q_{rst} (that may cause image lag).

Both above parameters are involved in the setting of the dynamic range. Since they are surface-dependent, it can be expected that reducing pixel size will enhance CG on the one hand, and degrade FWC on the other.

3. Physical Design

We have recently designed the 1T charge-modulation pixel structure in a 0.13µm CMOS process [8]. The layout of the transistor was a conventional form with a gate area of 1µm x 1µm. To avoid crosstalk, both source and drain areas of the transistor were surrounded with STI (shallow trench isolation), as is shown in Fig. 1. The pixel size was a 2.2µmx2.2µm, with a 46% fill factor.

By analyzing this 2.2µm-pitch pixel design, we have noticed that the use of STI in the pixel also presents drawbacks. Firstly, it increases the pixel size and reduces the fill factor. Secondly, it increases peripheral leakage current at the silicon surface and its contribution to the pixel dark current.

On the other hand, a conventional rectangular-gate transistor is not suitable to minimize tunneling effects (band-to-band tunneling or/and trap-assisted tunneling, impact ionization) in high-doping pn junction areas. By characterizing the 2.2µm-pitch pixel, we have observed a sharp increase of dark current for the drain voltage of the transistor beyond a certain threshold value, which is due to the band-to-band tunneling effect (shown in Fig. 4). It occurs in the gate-to-drain overlapped surface area where high-doping-profile and high-electric-field conditions are met. Such conditions are first met near sharp corners of the drain area. Predictably, this tunneling effect may be more pronounced when reducing the pixel size.

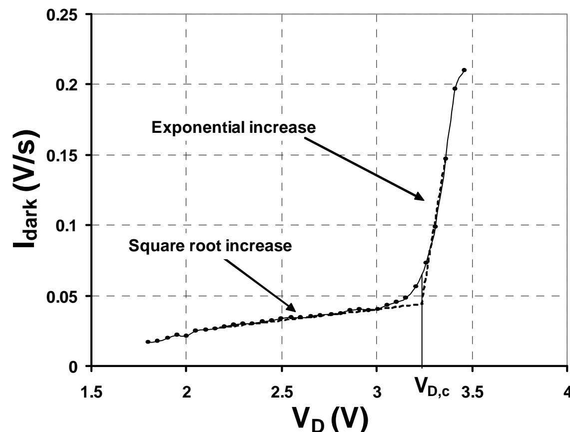


Fig. 4. Measured dark current of a 2.2µmx2.2µm rectangular-gate pixel versus drain voltage VD

To minimize this effect, we suggest a ring-gate design with source at the center and peripheral drain (see Fig. 5).

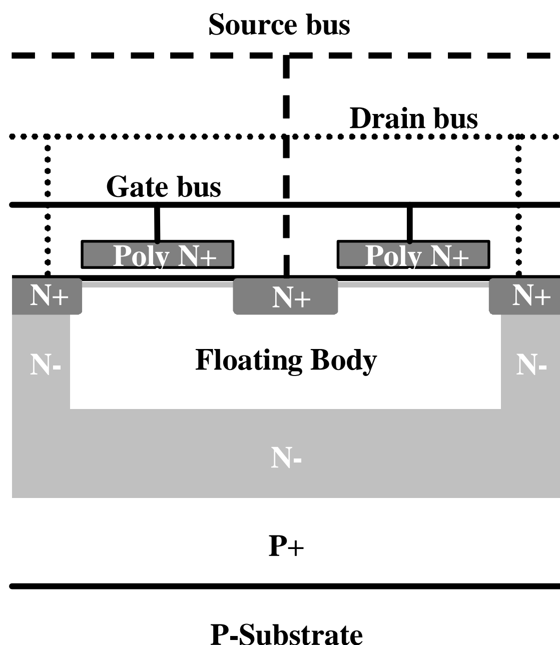


Fig. 5. Cross-section view of the ring-gate 1T Charge-modulation pixel

This implementation also eliminates the need for STI and its resulting dark-current contribution, because the surrounding drain of the transistor in the peripheral pixel area prevents charge diffusion. This STI suppression allows pixel-size reduction and/or fill-factor improvement.

Fig. 6 shows a 1.4µm-pitch, ring-gate pixel array designed in a 0.13µm front-end based CMOS process & 90nm copper-based process. The pixel has a 50% fill factor.

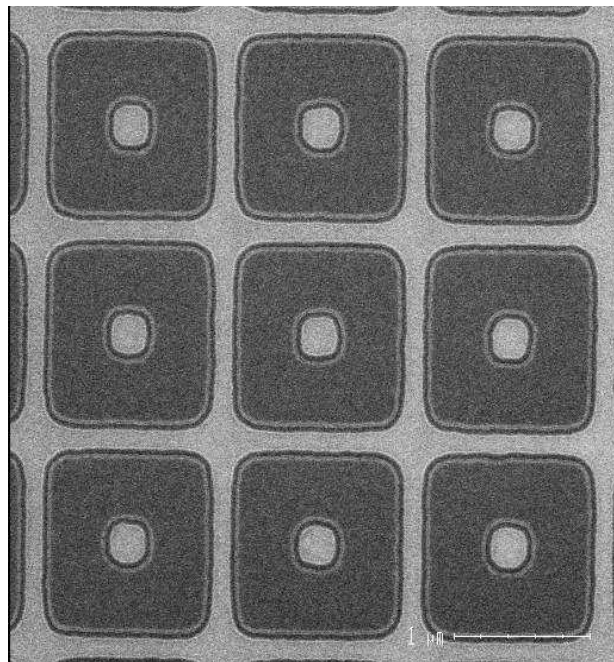


Fig. 6. Microphotography of a pixel array before metallization process (by Scanning Electronic microscope)

4. Pixel Characteristics

Fig. 7. shows a test chip integrating an array of 1.4µm-pitch pixel. It has been fabricated using a 0.13µm Front-End CMOS process that has the following characteristics: P-substrate, STI isolation (for peripheral region only), twin well, double gate oxide, and single poly. Unsilicided contacts have been used in the pixel arrays for higher integration density. The pixel fabrication process requires only 3 extra masks for specific implants and is fully compatible with the CMOS digital process.

Fig. 7. Microphotograph of a fabricated Test Chip

The measured characteristics of the 1.4µm-pitch ring-gate pixel are compared with those of the previously-designed 2.2µm-pitch pixel (summarized in Table 1).

The comparison of results in Table 1 shows improvements in most aspects (apart from FWC and sensitivity) for the 1.4µm-pitch ring-gate design. As expected, CG is enhanced while FWC is degraded. Meanwhile, the dark current is lowered from 80aA/pixel ($500h^+/s$) to 6.4aA/pixel ($39.7h^+/s$), which means a more than 12-fold reduction. Noise aspect including temporal noise and FPN is also substantially improved. One can also notice that a larger dynamic range is reached, meaning that the improvement on signal-to-noise ratio outweighs the degradation of FWC. However, many other improvements have still to be made (by design and process optimization) on this kind of architecture so as to reach performances (such as full well capacity, sensitivity, …) of current pixels employed in the image sensor application fields.

An example of image taken with this test chip is shown in Fig. 8.

Table 1. Comparison of measured characteristics between the 2.2µm rectangular-gate pixel and the 1.4µm ring-gate-design pixel

Parameter	2.2µm-pitch rectangular-gate	1.4µm-pitch ring-gate	Testing conditions
Process	0.13µm 1P 4M CMOS	0.13µm FE + 90nm BE 1P 3M CMOS	
Test chip size	3.2mm x 3.2mm	3.0mm x 3.2mm	
Pixel size	2.2µm x 2.2µm	1.4µm x 1.4µm	
Resolution	CIF (352 x 288)	VGA (672 x 512)	
Fill factor	46 %	50 %	Without microlens
Supply voltage	1.2V / 3.3V	1.2V / 3.3V	
Conversion gain	35µV/h^+	**58**µV/h^+	
Full well capacity	6200 h^+	**2000** h^+	
Dark current	500 h^+/s	**39.7** h^+/s	Mean value @ RT
Pixel temporal Noise	6 h^+	**2.4** h^+	In darkness
FPN	21.3 h^+	**4.3** h^+	Without additional correction circuit
Noise floor	40 h^+	**4.9** h^+	Temporal noise, FPN & DSNU in darkness
Dynamic range	44 dB	**52** dB	Usable Well over Noise floor
Sensitivity	1800 h^+/lux.s	600 h^+/lux.s	B/W sensitivity without microlens Halogen 3200K IR cut off 650nm

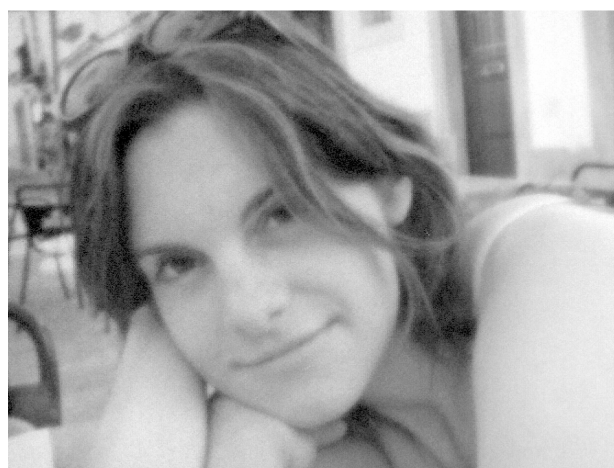


Fig. 8. Image example using the test chip (VGA format)

5. Conclusion

We have proposed a ring-gate design of the 1T charge-modulation pixel structure. It suppresses the need to employ STI in the pixel, thus allowing smaller size and/or higher fill factor. This also reduces dark current by limiting peripheral leakage current and minimizing band-to-band tunneling effect.

Acknowledgment

The authors would like to thank the front-end technology and manufacturing (FTM) group of STMicroelectronics for wafers processing. Thanks are extended to all members of the FTM imaging group for their dedicated effort in design, test and process integration.

References

[1] G. Agranov et al., “Optical-electrical characteristics of small, sub-4µm and sub-3µm pixels for modern CMOS Image Sensors”, *in Proc. IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Nagano, 2005, pp. 206-209.

[2] S.-H. Lee et al., “The features and characteristics of 5M CMOS image sensor with topologically Unique 1.7x1.7µm² pixel”, *in Symposium on VLSI Technology Dig. Tech. Papers*, Honolulu, 2006.

[3] K-B Cho et al, “A 1/2.5 inch 8.1Mpixel CMOS Image Sensor for Digital Cameras”, *in International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, San Francisco, 2007, pp. 508-509.

[4] M. Cohen et al., “Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensors”, *in IEEE International Electron Devices Meeting (IEDM) Dig. Tech. Papers,* San Francisco, 2006

[5] K. Matsumoto et al., “The Operation Mechanism of a Charge Modulation Device (CMD) Image Sensor”, *IEEE Trans. Electron Devices*, vol. 38, pp. 989-998, May 1991

[6] J. Hynecek, “BCMD - An Improved Photosite Structure for High-Density Image Sensors”, *IEEE Trans. Electron Devices*, vol. 38, pp. 1011-1020, May 1991

[7] T. Miida et al., “A 1.5MPixel Imager with Localized Hole-Modulation Method”, *in International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, San Francisco, 2002, pp. 42-43.

[8] A. Tournier et al., “Implementation and electrical characterization of CMOS single-transistor charge-modulation pixel structure”, *in Proc. 8th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, Shanghai, 2006, pp536-538.

A 28M 43cm^2 full-frame CCD Imager for Medical and Scientific Applications ("Big is Beautiful")

Jan T. Bosiers, Bart Dillen and Louis Meessen
DALSA Professional Imaging, High Tech Campus 12a, 5656 AE Eindhoven, The Netherlands
e-mail Jan.Bosiers@DALSA.com; phone +31-40-274 2227; fax +31-40-274 4090

INTRODUCTION

Contrary to many consumer applications where cost is a driver for shrinking pixel sizes, certain medical, scientific imaging and aerial reconnaissance applications [1] require large-format imagers. This paper presents a 'half-wafer-scale' 7k x 4k 86mm x 49mm full-frame CCD imager, to our knowledge one of the largest ICs in the world that is in regular production. Next to the challenges in design and wafer fabrication, the paper also describes the solutions for testing, assembly and application development for this very large device.

SENSOR DESIGN

A schematic representation of the sensor is shown in Fig.1. Stitching is used in lithography to manufacture this sensor [2]. The building block concept was presented in [3]. The sensor has 28M 4-phase pixels of 12 x 12μm^2 size, a 3-phase readout register both at the top and bottom, and four identical output amplifiers. Readout can be done through one, two or four outputs by applying the appropriate driving pulses to the horizontal and vertical clocks. To achieve efficient highlight handling, fast electronic shutter and excellent charge transport, a buried channel CCD structure in a p-well on an n-type substrate was chosen [4]. The four-phase bi-directional image section is also beneficial for aerial reconnaissance since it allows a 'TDI'-mode of operation for motion compensation [1].
Special performance challenges relating to very-large imagers had to be met. The first one relates to the RC-time constants of the image electrodes. These 84mm long poly-silicon gates have a resistivity of 35Ω/ . Reducing the resistance by increasing the thickness of the electrodes is no option, since this would decrease the optical transmission. Thus, to achieve a sufficiently high vertical transport frequency, other solutions had to be found. First, etching 'windows' in the pixel area reduced the capacitance of the electrodes, Fig. 2. The reduction in capacitance is larger than the reduction in resistance since a major part of the capacitance is formed by the poly-p^+ channel stop capacitance. The capacitance between the electrodes was further reduced by using anisotropic etching for the second poly layer, resulting in adjacent, i.e. non-overlapping electrodes [5].
The holes that are generated in a CCD imager need to be drained efficiently, especially during over-exposure [6]. This means the resistance of the 48mm long p^+ channel stops must be small enough to avoid a significant voltage drop. The implant dose was adjusted accordingly.
The doping profiles for the pixel were optimized for operation in "standard mode" (integration with three integrating gates at 8V, blocking gate at 0V; and transport with clock voltages from 0V to 11V) and in "high-charge capacity mode' (integration at 10V and transport at 14V). This required careful optimization to combine good overexposure control with excellent transport efficiency since the risk of charge being trapped at the interface for large charge packets transported increases at 14V [7]. By transporting with externally applied clock voltages larger than the integration voltages, the effective clock swing in the center of the image by the RC time constants is significantly reduced to avoid charge transport problems.
Charge binning is supported; the horizontal and vertical binning ratios can be independently controlled by an appropriate choice of pulse waveforms. Vertical binning is done in the horizontal register and is facilitated by over-dimensioning this register for 2x the maximum charge of the image pixel. Horizontal binning, e.g. 2x, can be achieved by adding charge under the last gate (SG, summing gate) before the output gate or on the floating diffusion, respectively by clocking SG or the reset gate (RG) at half the register frequency. To support the required high charge capacity, SG and RG can be clocked with a 10V clock swing.

SENSOR FABRICATION, TEST AND ASSEMBLY

For an imager in regular production, a predictable, stable and 'high' yield is important. Both the technology and design were optimized for performance as well as for yield. A process using three layers of poly-silicon and one layer of metal is used for manufacturing the sensor. Only 13 mask layers are required. For yield optimization, the minimum feature size used is 0.7µm, while 0.35 µm is technologically possible.
Another aspect of regular production is the fit of the imager design with the parametric test equipment of the wafer fab. By having separate connections for the four quadrants, and by placing all bond pads for the imager present close to the four corners of the design, the sensor parametric test can be performed with 'standard size' probecards on standard parametric test equipment. A +-shaped probecard, common for the whole family of 12 x 12μm^2 pixel-size full-frame imagers, is used to probe four corners of four adjacent devices in a single sequence (Fig. 3).
The sensor is functionally tested on wafer in the assembly clean room at the sensor development site, using a standard wafer prober combined with dedicated optics and electronics. Hermetical sealing in a ceramic package with glass lid without out-gassing problems was achieved by the implementing correct specifications of the package, glass and die and cover glass adhesive, and by a proprietary sealing technique. After assembly, the sensor is fully tested in a dedicated test set up.

SENSOR APPLICATION AND PERFORMANCE

The sensor performance at 20kHz vertical transport and 10MHz horizontal transport is identical to that of smaller devices using the same 'building blocks' [8]. No effect of the imager size is seen on highlight handling or charge transport efficiency. Table 1 shows a performance summary.
The sensor can be operated by existing peripheral circuitry as shown in Fig. 4, thus allowing a compact, 'low-power' application. The power consumption of the sensor itself, when reading 0.25 fps through one amplifier only, and with 11V image clock swing, is only 1.5W, the equivalent of 3W per wafer or 35mW/cm^2, which implies that this device can be considered a true low-power imager…
Table 1 summarizes the performance. Fig. 5 shows two sensors on a 6" wafer after processing, and Fig.6 the assembled sensor. Fig. 7 shows an image obtained with this sensor.

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Many DALSA associates contributed to the success of this imager. The authors would especially like to thank Raymond Frost, Piet Jansen, Wilco Klaassens and Claudia Stoldt for their support.

REFERENCES

[1] B. Mathews, "An ultra high resolution, electro-optical framing camera for reconnaissance and other applications using a 9216 by 9216 pixel, wafer scale, focal plane array", SPIE Conf. on Airborne Reconnaissance, San Diego, CA, 1998
[2] A. Theuwissen et al., "A 2.2 Mpixel FT-CCD imager according to the Eureka HDTV-standard", IEDM Tech. Digest, 1991.
[3] G. Kreider et al.,"An mK × nK bouwblok CCD image sensor family - Part I: Design", IEEE T-ED vol. 49 no.3, 2002.
[4] J. Bosiers et al., "A 1/3" 1280(H) x 960 (V) FT-CCD for digital still camera applications", IEDM Tech. Digest, 1997.
[5] H.Peek et al, "A Low Dark Current Double Membrane Poly-So FT-Technology for 2/3 Inch 6M Pixel CCD Imagers", IEDM Tech. Digest, 1999.
[6] A. Theuwissen, "The hole role in solid-state imagers", IEEE T-ED vol. 53 no.12, 2006.
[7] J. Bosiers et al., "A 35-mm format 11M pixel full-frame CCD for professional digital still imaging ", IEEE T-ED vol. 50 no.1, 2003.
[8] G. Kreider et al., "An mK × nK bouwblok CCD image sensor family—Part II: Characterization ", IEEE T-ED, vol. 49 no.3, 2002.

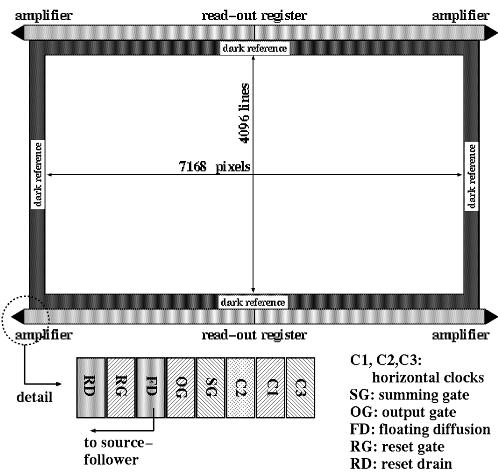

Fig.1. Schematic representation of 43cm^2 CCD imager

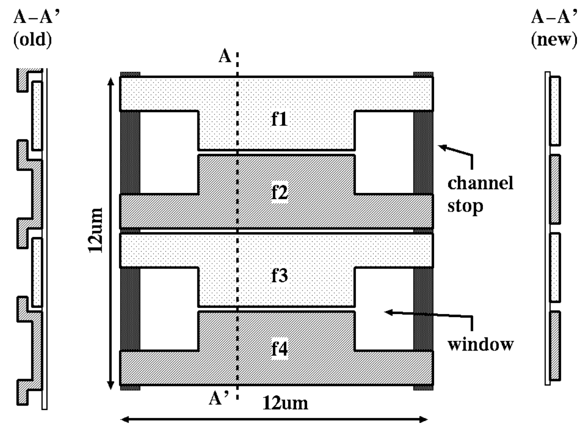

Fig.2. Top view of image pixel and cross-section of electrodes with old (isotropic; left) and new (anisotropic; right) etching method

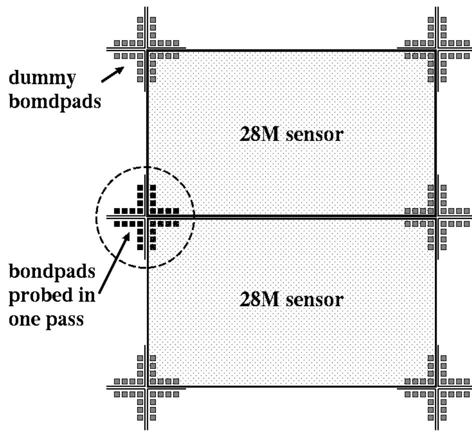

Fig. 3. Parametric probing scheme for 43cm^2 CCD imager

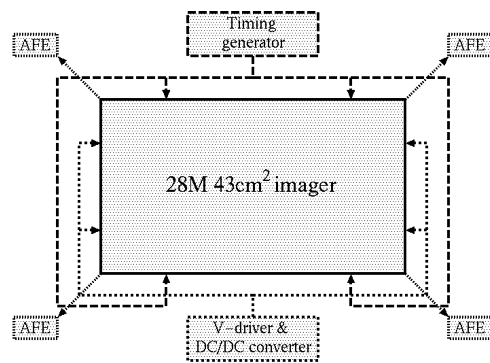

Fig.4. Application schematic. The circuitry is identical to that needed for smaller devices using the same building blocks (AFE: analog front-end with CDS & ADC)

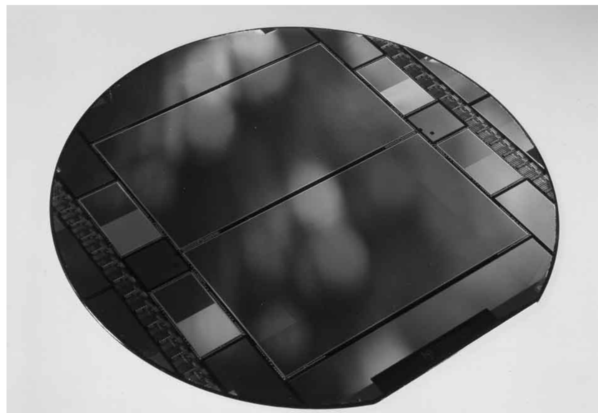

Fig.5. 6" wafer with two 28M 43cm^2 CCD imagers

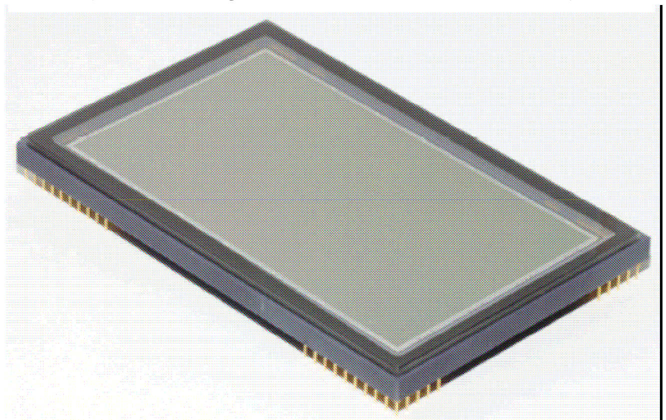

Fig. 6. Assembled sensor in hermetic PGA package

CCD type	Full-frame
Optical size	86mm x 49mm
Chip size	43cm^2
Active area	42cm^2
Resolution	7168 (H) x 4096 (V)
Pixel size	12 x 12 μm^2
Technology	Three poly-silicon layers, one metal layer
Minimum feature size	0.7 μm
Image pixel	Four-phase, bi-directional, 100% fill factor
Image performance	Vertical anti-blooming (200x overexp.), electronic shutter
Readout register	Three-phase, bi-directional
Number of outputs	4
Output amplifier type	Triple source follower, external load for 3rd stage
Output formats	Full resolution & n x m binned
Output mode	Single, dual, quadruple output
Maximum vertical frequency	20kHz
Pixel charge capacity (0V-8V int., 0V-11V transp.)	380,000 electrons
Pixel charge capacity (0V-10V int., 0V-14V transp.)	550,000 electrons
Maximum horizontal frequency	10Mhz
Clocks swing readout register	5V
Charge transport efficiency (H&V)	> 0,999 999 5
Readout register charge capacity	800,000 electrons
Maximum charge capacity (horizontal binning, detection node)	800,000 electrons (10V SG and RG clock swing)
Output amplifier conversion factor	8 $\mu V/e^-$
Amplifier noise after CDS processing	35 e^-
Package	Ceramic, 104-pins PGA with hermetical seal (available also without cover glass)
Flatness	25μm

Table 1. Overview of device specifications

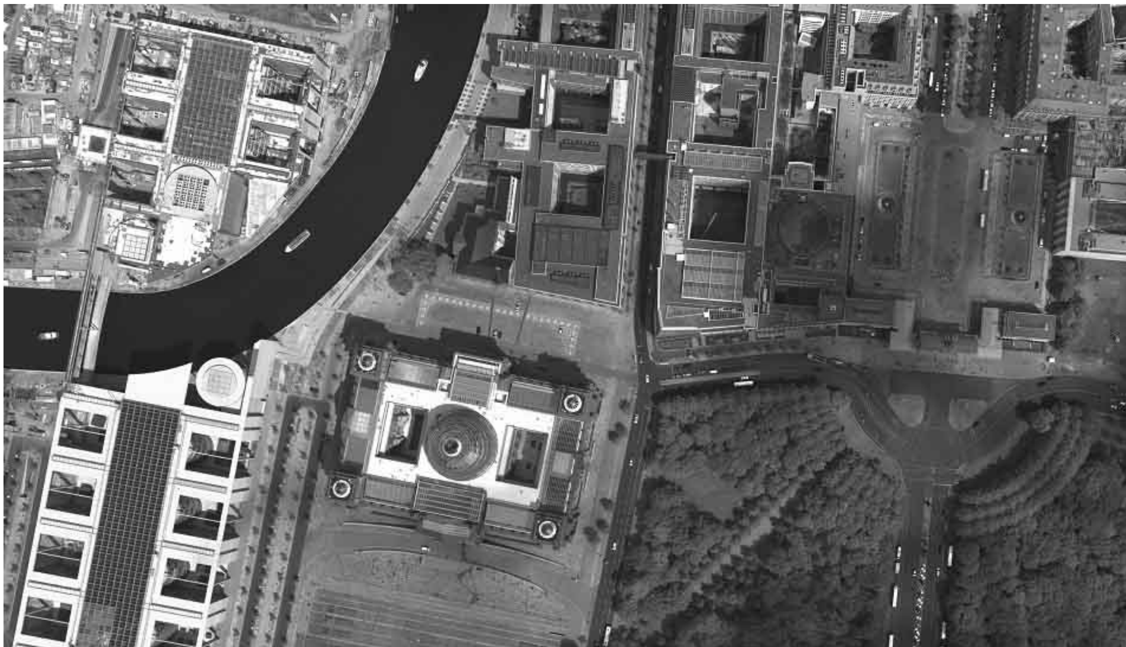

Fig.7. Image obtained with 28M 43cm^2 imager (Reichstag, Berlin)

Orthogonal Transfer Arrays for Wide-Field Adaptive Imaging†

Barry E. Burke[a]*, John L. Tonry[b], Michael J. Cooper[a], Peter E. Doherty[a], Andrew H. Loomis[a], Douglas J. Young[a], and Peter Onaka[b]
[a]MIT Lincoln Laboratory, 244 Wood Street, Lexington, MA USA 02421
[b]Institute for Astronomy, University of Hawaii, Honolulu, HI USA 96822

The orthogonal transfer array (OTA) is a novel charge-coupled device (CCD) imager based on the orthogonal-transfer CCD (OTCCD). The OTCCD, in turn, is a device capable of charge transfer in all directions and has been developed for adaptive imaging in ground-based astronomy. By using a bright guide star as a beacon, the OTCCD can correct for wavefront tilt due to atmospheric effects as well as compensation for telescope shake, which in turn enhances the resolution and SNR [1]. However, for wide field-of-view imaging the atmospheric wavefront distortions decorrelate over distances more than a few 10's of arcmin and hence an array of independently driven OTCCDs is required.

To resolve this issue we developed the OTA, which consists of a two-dimensional array of OTCCDs combined with addressing and control logic to enable independent clocking of each OTCCD. This device enables spatially varying electronic tip-tilt correction and was developed for the Panoramic Survey Telescope and Rapid Response System (Pan-STARRS) program at the University of Hawaii Institute for Astronomy (UH/IfA) [2]. The basic architecture is illustrated in Figure 1, and features an 8×8 array of OTCCDs on a 50×50-mm die. Figure 2 describes the individual OTCCD, or cell, comprising a 590×598-pixel imaging array of 10-µm pixels, serial register and readout circuit. A small block of NMOS logic controls the parallel clock drive to each OTCCD and the schematic for this logic is shown in Figure 3.

Each logic block is addressed by a row and column select line and accepts three data bits, D0–D2. These bits in turn set the state of three lines, Z0–Z2, which are connected to pass transistors that in turn control the parallel clocks and video output. Line Z1 enables four parallel clocks from off-chip drivers to be applied to the gates, while Z0 sets the gates in a standby state with two phases (1, 2) high and the remaining two low. During image readout, Z1 and Z2 are high, but only one cell in a column can be read out at a time since all eight cells in a column share a video output bus.

The device operation consists of about 30 s? of image acquisition followed by a readout period. During the integration period the parallel clocks of each cell must perform pixel shifts to track the image motion. To measure the local wavefront tilt, a small subset of cells (up to 5) in an OTA are used to image bright guide stars at rates up to 30 Hz. From the image deflection data of these star images, the optimum pixel shifts for the remaining cells ("science cells") can be computed. Each of the science cells is addressed sequentially and the appropriate pixel shift applied. At the end of the image acquisition time, the science imagery is read out one row at a time. A two-stage amplifier at the output of each cell provides sufficient drive for read rates greater than 1 Mpixel/s.

Two important performance measures for this device are high quantum efficiency, especially in the I band (730-900 nm) and small charge point-spread function (PSF). This necessitates the use of thick, high-resistivity material with a design that enables substrate bias. The OTA is fabricated on p-type, 150-mm wafers having a resistivity of 5 000 Ω·cm or greater. Figure 4 illustrates in cross section the features that enable such a capability. The back surface, which is a thin p^+ layer, is biased from the front of the device via an undepleted path around the device perimeter. To prevent excessive front-to-back hole current, the channel stops are narrow and the remaining non-active device area filled with an n+ doped layer biased to a positive potential [3]. This approach has another feature of interest, namely, it effectively isolates the ground reference of the CCD from the logic. This in turn allows us to bias the logic, which passes the parallel clocks to the pixels, below ground. This is favorable for the performance of buried channel CCDs in terms of well capacity and charge-transfer efficiency. We typically use low parallel clock rails of -3 to -6 V. The serial clocks come directly from off-chip drivers and therefore are likewise not constrained as to voltage rails.

The advantages of substrate bias can be seen clearly in Figures 5 and 6. Figure 5 shows the improvement in RMS charge spreading with substrate bias. For Pan-STARRS the goal is less than 4 µm. Figure 6 shows the improved quantum

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†The MIT Lincoln Laboratory portion of this work was performed under a Collaboration Agreement between MIT Lincoln Laboratory and The University of Hawaii, Institute for Astronomy (UH/IfA). Opinions, interpretations, conclusions, and recommendations are those of the authors, and do not necessarily represent the view of the United States Government.
* bburke@ll.mit.edu.

efficiency resulting from an increase in device thickness from 45 µm (our standard for non-substrate biased devices) to 75 µm. The device has a two-layer anti-reflection coating optimized for the visible/near IR with a reflectivity null near 850 nm. This coating and the increased device thickness virtually eliminates the problematical Fabry-Perot "fringing" from sky glow.

Figure 7 is an image taken with a back-illuminated OTA at -70˚C. The device comprises 22.6 Mpixels, and the fill factor is 0.90.

A photo of a front-illuminated packaged device is shown in Figure 8. The package base is made of Mo, and attached to it are three mounting legs and a custom multi-layer ceramic pin-grid array (PGA). A narrow lip of this ceramic appears at one edge of the Mo base and contains wirebond landings for the 99 device pads. The PGA is located beneath the package and is not visible in this photo. All the device I/O is carried to the support electronics via a flexprint that is press-fitted onto the PGA.

The program goal is a focal-plane array of 64 OTAs comprising collectively about 1.4 Gpixels, as illustrated in Figure 9. The devices for this focal plane array have been fabricated and packaged, and the assembly of the array is expected to begin this summer. As a stepping stone to the final Pan-STARRS focal plane, a 4×4 array of OTAs from a prototype lot has been assembled and is undergoing testing on the first of the four Pan-STARRS telescopes. A photo taken during the assembly of this array is shown in Figure 10.

References:

[1] J. L. Tonry , B. E. Burke and P. L. Schechter, "The Orthogonal Transfer CCD," Publications of the Astronomical Society of the Pacific, vol. 109, pp.1154-1164, October 1997.

[2] J. L. Tonry, P. M. Onaka, B. E. Burke, and G. A. Luppino, "Pan-STARRS and Gigapixel Cameras," in *Scientific Detectors for Astronomy*, J. Beletic et al. eds., Springer, pp. 53-62, 2005.

[3] B. E. Burke, J. A Gregory, A. H. Loomis, M. Lesser, M. W. Bautz, S. E. Kissel, D. D. Rathman, R. M. Osgood III, M. J. Cooper, T. A. Lind, and G. R. Ricker, "CCD Soft-X-Ray Detectors with Improved High- and Low-Energy Performance," IEEE Trans. Nuclear Science, vol. 51, 2322 - 2327, October 2004.

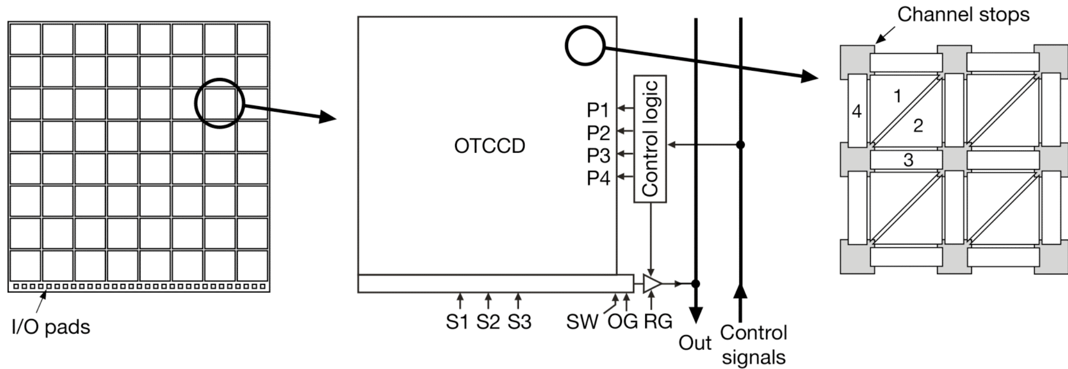


Figure 1. Depiction of the OTA. Each of the 64 cells consists of an OTCCD with 590(V)×598(H) pixels and a serial readout register. The parallel shifting and multiplexing of the video output of each cell is controlled by a logic block. The drawing on the right illustrates the arrangement of the four-phase CCD gates.

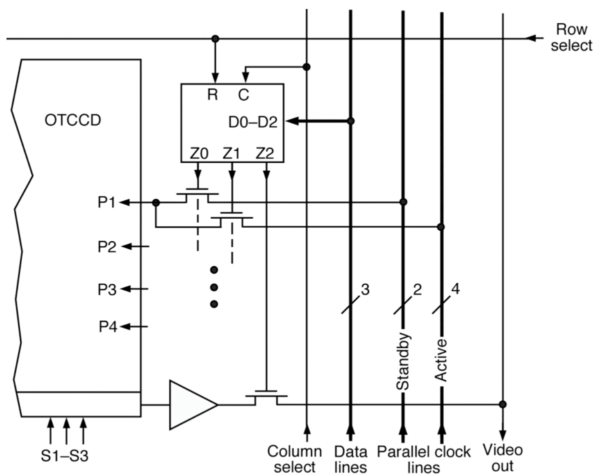


Figure 2. Schematic of the OTA cell and logic control.

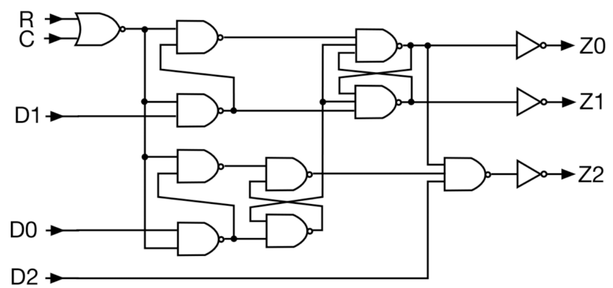


Figure 3. Control logic design used on the OTA.

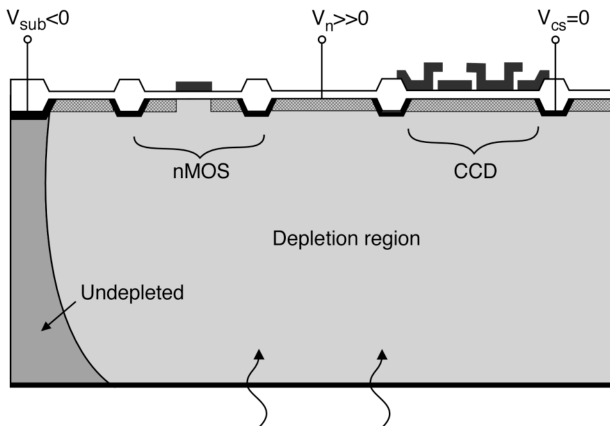


Figure 4. Cross section of OTA with substrate bias capability.

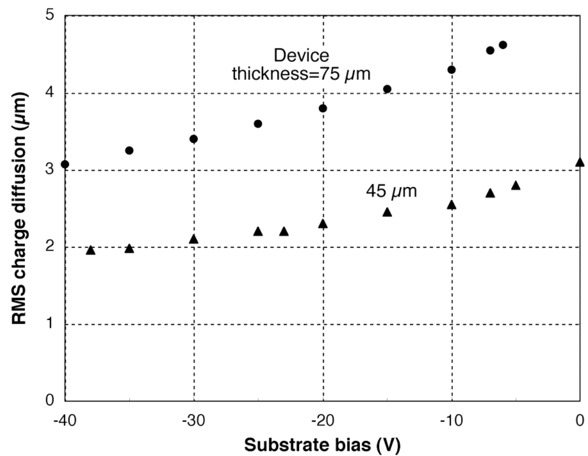


Figure 5. RMS charge diffusion vs. substrate bias for devices of two thicknesses.

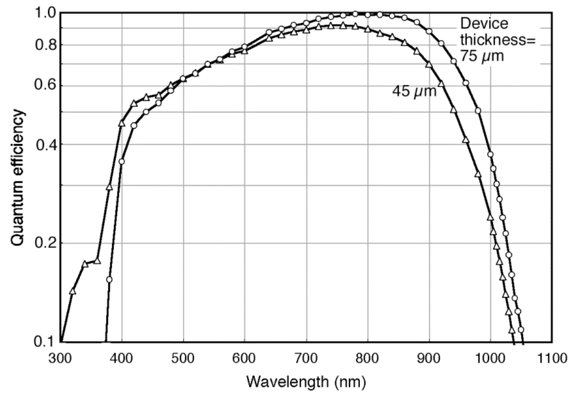


Figure 6. Quantum efficiency vs. wavelength at -70˚C for devices of 45 and 75 µm thickness.

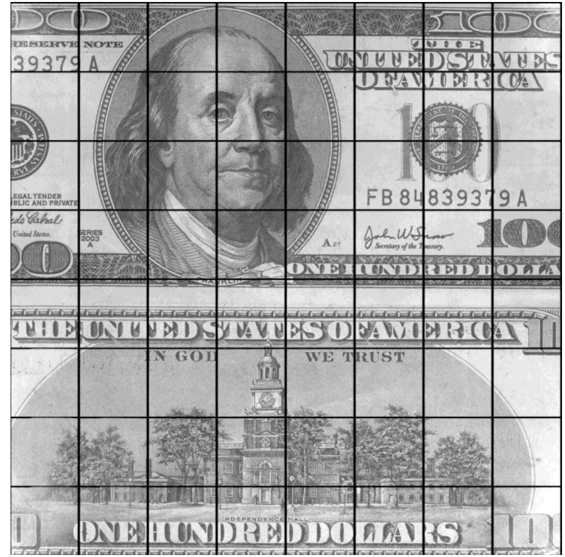


Figure 7. Image from a back-illuminated OTA (22.6 Mpixels) at -70˚C.

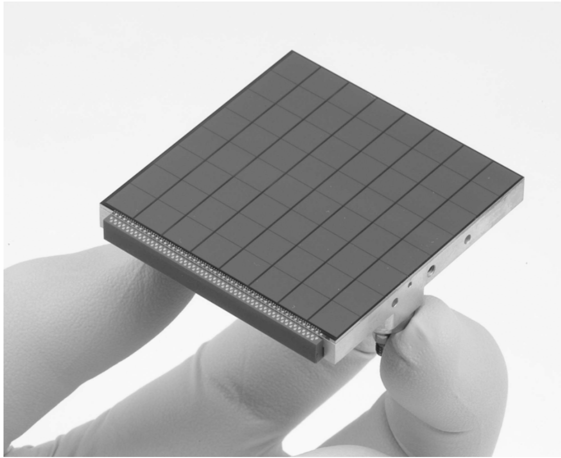


Figure 8. Photo of a packaged front-illuminated OTA.

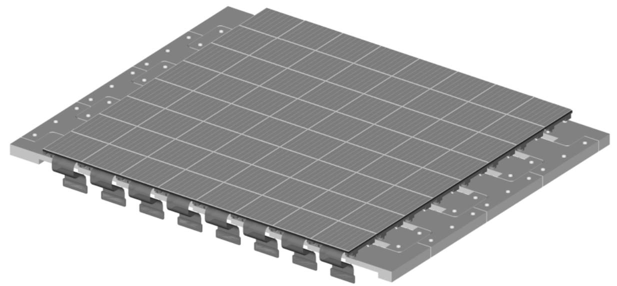


Figure 9. Depiction of the full 8×8, 1.4 Gpixel focal-plane array for Pan-STARRS.

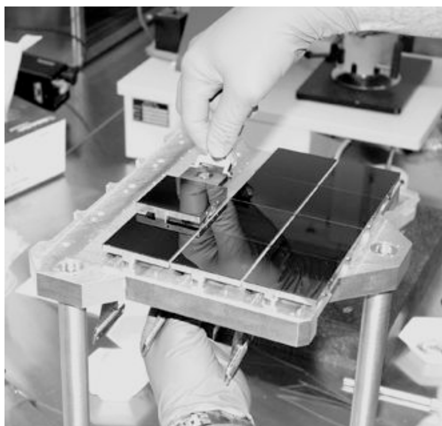


Figure 10. Photograph of the assembly of a 4×4 prototype focal plane array of OTAs for intital tests on the first Pan-STARRS telescope.

High Performance CMOS Image Sensor for Low Light Imaging

Xinqiao (Chiao) Liu, Boyd Fowler, Hung Do, Steve Mims, Dan Laxson, and Brett Frymire
Fairchild Imaging, Inc., 1801 McCarthy Boulevard, Milpitas, CA 95035

Abstract

We present a prototype CMOS image sensor (CIS) intended for low light imaging applications. The prototype sensor contains 320 x 240 pixels with 36 different pixel architectures. Pixel size is 10.8 µm x 10.8 µm. The measured QE is 55% at 555nm, dark current is 11pA/cm^2 at 30 ˚C, read noise is 1.9e- RMS operating at 30 Mpixels/sec, and the conversion gain is 1046 µV/e-. We present the pixel design that achieved the best performance taking into account dark current, image lag, QE, and read noise. We also describe the low noise readout circuitry that achieves the lowest read noise published to date for any area CIS.

Keywords: CMOS, image sensor, CIS, scientific image sensor, FPA, low light level, read noise

Introduction

Many scientific, medical and industrial imaging applications demand low-light solid-state focal plane sensors that have photon counting sensitivity, megapixel or higher resolution, and hundreds or even thousands of frames per second readout speed. Some examples include live-cell fluorescence microscopy, DNA sequencing, electron microscopy, X-ray crystallography, and security surveillance. To achieve high sensitivity, the sensor needs to have very low dark current (ideally less than 1e-/pixel/frame at 60 ˚C), very low read noise (ideally less than 1e-), and very low image lag (ideally less than 1e- per transfer since image lag introduces excess noise). Further, the sensor needs to high QE (>50%), high MTF (>50% at Nyquist), good linearity, and good uniformity (PRNU <2%).

The introduction of the pinned photodiode technology and the advance of low noise readout circuitry have dramatically improved the image quality of CMOS image sensors [1], [2]. These developments are rapidly making CMOS sensors the preferred technology for developing new high-performance low-light image sensors.

Fairchild Imaging has always been at the forefront of the high performance imaging development. Previously we presented a CCD / CMOS hybrid focal plane array for low light level imaging applications [3]. In this paper, we present a prototype monolithic CMOS image sensor design that further enhances our low light imaging capabilities. The sensor has a measured conversion gain of 1046 µV/e-, a dark current density of 11pA/cm^2 at 30C, and sensor read noise of 1.9e- RMS operating at 30 Mpixels/sec.

In the following sections, we present the pixel design that achieved the best performance taking into account dark current, image lag, QE, and read noise. We will also describe the low noise readout circuitry that achieves the lowest read noise published to date for any area CIS.

Sensor Architecture

The prototype sensor was fabricated using a 0.18 µm CMOS image sensor process through a commercial foundry. The process features a pinned photodiode for low dark current and specially engineered pixel transistors for improved voltage swing and low 1/f noise. The design also features a thinned backend process with reduced the stack height. Figure 1 shows the chip layout and Figure 2 shows the block diagram. The prototype sensor contains 320 x 240 pixels with a total of 36 different pixel designs. The sensor has two analog output ports and can operate at up to 30 Mpixels/sec per output port. The pixel size of the sensor is 10.8 µm x 10.8 µm. Figure 3 shows the analog signal chain schematic. The signal path includes the pixel circuit, column amplifier, sample and hold capacitors, and analog multiplexing circuit.

Contact info: chiao.liu@fcimg.com, (408) 433-2605

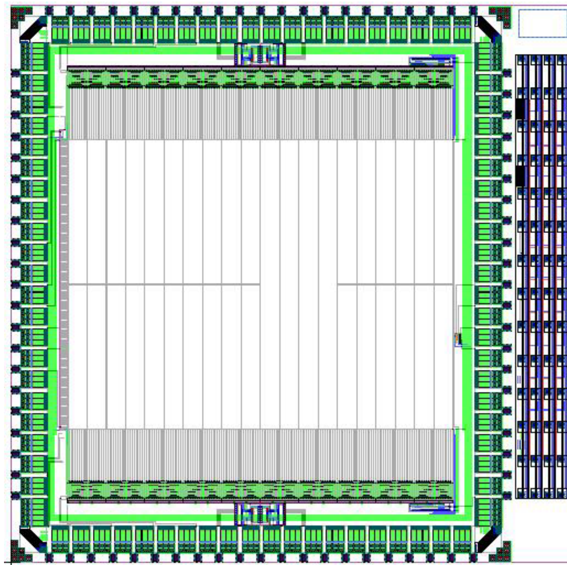


Figure 1. Prototype chip layout

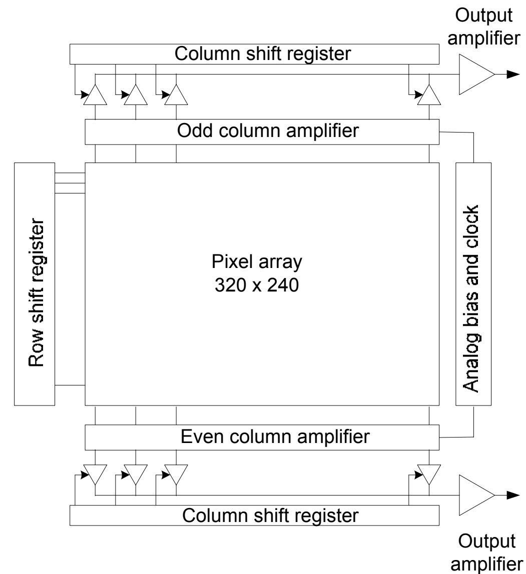


Figure 2. Sensor block diagram

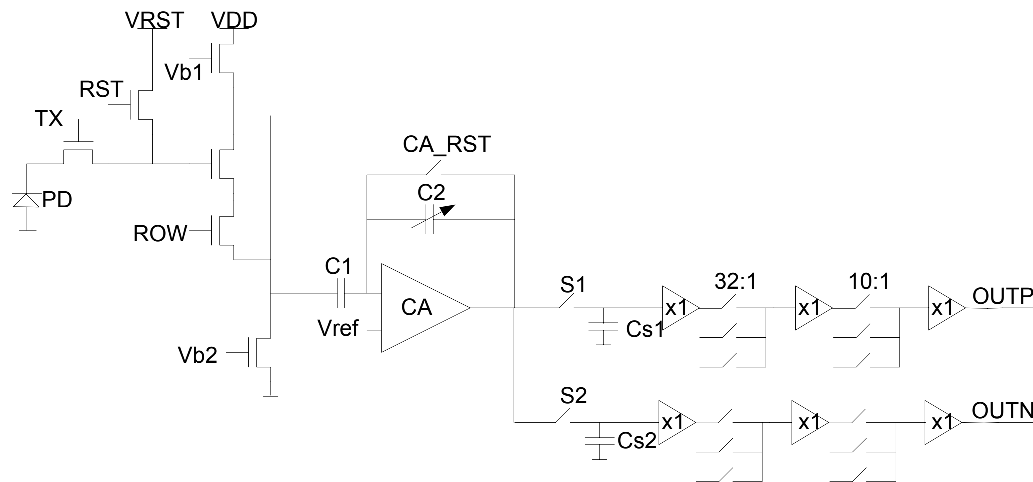


Figure 3. Analog readout signal chain

The 10.8 μm pixel employs a 5T APS circuit where the fifth transistor on top of the source follower transistor is used for power supply noise rejection and impact ionization noise reduction. The column amplifier has two gain modes: a high gain mode of 1046 μV/e- and a low gain mode of 32 μV/e-. The full well capacity is limited by the final output voltage swing in high gain mode with a well capacity of 1.4 ke-; and it is limited by the voltage swing at the floating diffusion node in low gain mode with a well capacity of 30 ke-. The column amplifier bandwidth was carefully adjusted such that minimum thermal noise contribution from the amplifier is achieved in high gain mode. To reduce the 1/f noise, the size of the source follower transistor inside the pixel is larger than minimum size.

Pixel reset noise is cancelled by the correlated double sampling circuit. The two sampling capacitors at the column amplifier output further reduce the KTC noise due to the column amplifier reset transistor. The sampled reset and signal voltages are multiplexed and read out in pseudo differential mode such that the common mode noise coupled from other sources can be further eliminated at the off-chip differential ADC.

Pixel Design Optimization

A total of 36 different pixel designs are in the main array. Pixel variations are intended to help optimize critical sensor parameters such as dark current, QE, image lag, and read noise. Figure 4 shows the cross section of the pinned photodiode. The varying parameters within different designs include the distance from the buried diode to the STI edge (d1), the overlap of the transfer gate threshold adjustment implant, and the size and shape of the photodiode (d2).

Figure 5 shows a typical pixel layout, where the green region is the photodiode and the grey region is the active area. The effective pixel fill factor is 81%. Color filters and micro-lenses were not used in the fabrication of this chip. The large pixel area of this design provides a lot of freedom to optimize pixel architecture in order to achieve superior low-light imaging performance. Such opportunity is not available in small pixel designs where the architecture is strongly constrained by the limited pixel area.

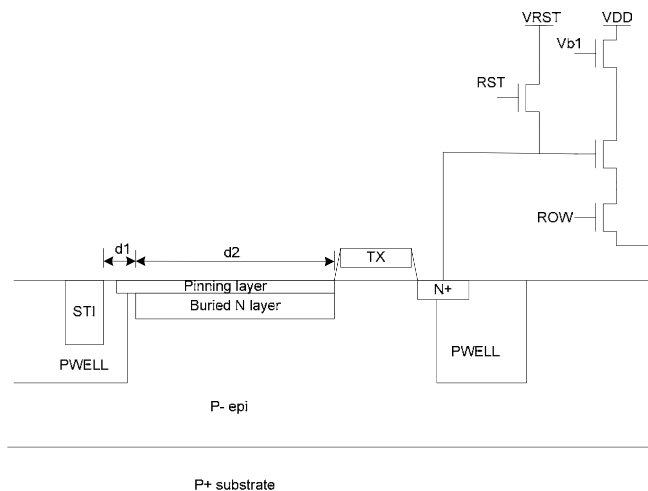


Figure 4. Pixel cross section

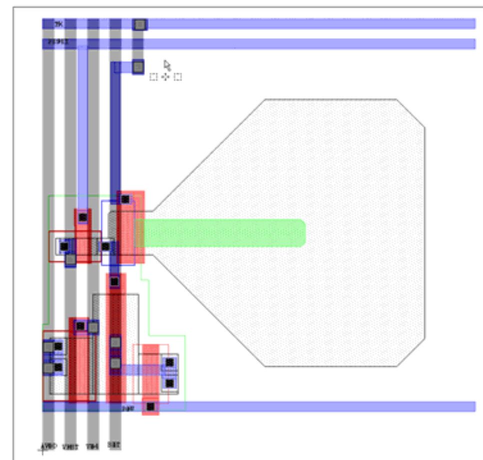


Figure 5. Typical pixel layout

Measurement Results

Figure 6 is a measured photon transfer curve. A conversion gain of 1046 µV/e- was achieved by reducing the floating node capacitance and using a high-gain column amplifier. The non-linearity of the sensor is less than 0.5%. Figure 7 shows the dark current density histogram of one pixel design. The mean dark current density of 10.8 pA/cm^2 was achieved by separating the photodiode edge from STI edge by 1 µm. The histogram also shows white pixels at higher dark current levels. Figure 8 shows the sensor read noise histogram with a mean value of 1.9e- and standard deviation of 1.2e-. The noise measurement was performed at 30 Mpixel/sec output rate, since the readout circuit was designed for a 1k x 1k sensor operating at 30 frames/sec. Further investigation of the noise source revealed that a majority of the noise is a result of the charge transfer operation. The read noise was reduced to 0.7e- RMS if TX gate was maintained low. Detailed modeling and analysis of the charge transfer noise are presented by another paper in this conference [4]. Table 1 summarizes the measurement results of the various pixel designs.

Summary

In this paper, we presented a prototype CMOS image sensor designed for low-light imaging applications. The initial results are encouraging, especially the low sensor readout noise, low dark current, and high sensitivity. These combined with the inherent low power and high speed potential of CMOS imager sensors will enable this technology to make further inroads into high performance imaging applications previously dominated by CCDs.

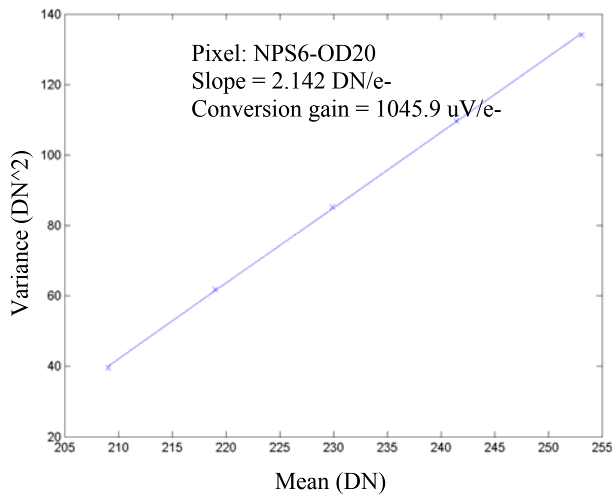


Figure 6. Photon transfer curve and the conversion gain

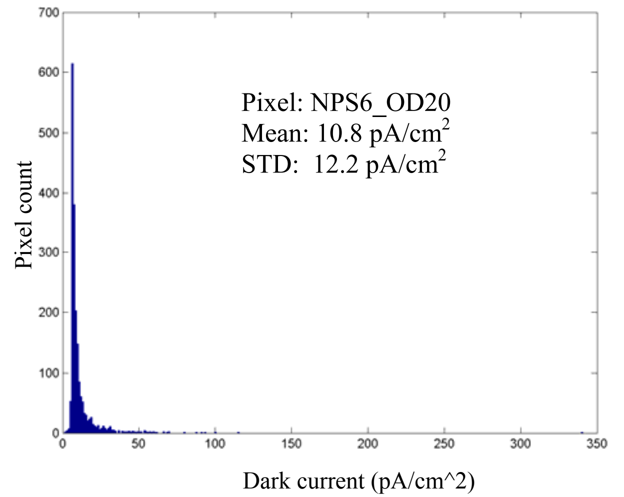


Figure 7. Dark current distribution

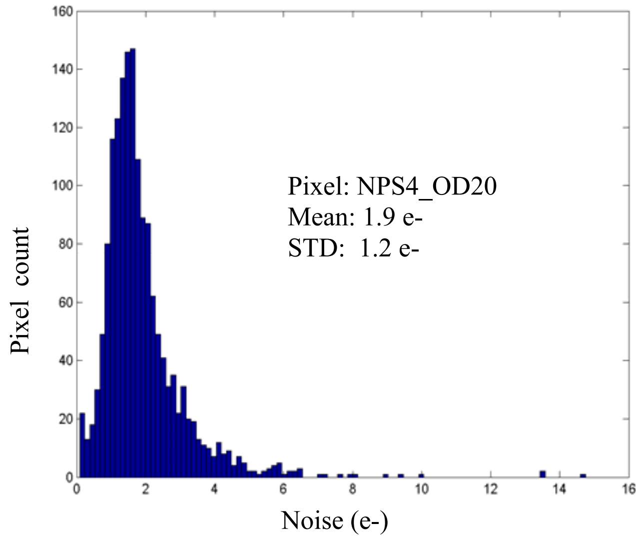


Figure 8. Read noise distribution

Pixel	Conv gain (uV/e-)	Dark current (pA/cm^2)	Read noise (e-)	QE (550nm)	Lag
NPS2_OD10	999	9.0	2.5	48.5%	0.24%
NPS4_OD10	1034	10.1	2.4	52.4%	0.17%
NPS6_OD10	1088	10.3	2.4	50.8%	0.15%
NPS6_OD20**	1046	10.8	2.5	53%	0.18%
NPS4Q_OD10	1189	10.5	1.9	44.9%	8.72%
NPS7Q_OD10	1254	10.8	2.5	49.3%	38.4%

Table 1. Measured results of various pixels

Acknowledgement

The authors would like to thank David Wen, Paul Vu, and Steve Onishi for technical discussions and supports.

References:

[1] Y. Nitta, et. al., "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor", IEEE International Solid State Circuit Conference, Dig. of Technical Papers, 2006
[2] A. Krymski, N. Khaliullin, and H. Rhodes, "A 2e- Noise 1.3Megapixel CMOS sensor", 2003 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors
[3] X. Liu, B. Fowler, S. Onishi, P. Vu, D. D. Wen, H. Do, and S. Horn, "CCD/CMOS Hybrid FPA for Low Light Level Imaging," in Proceedings of SPIE, 5881, July 2005
[4] B. Fowler and X. Liu, "Charge Transfer Noise in Image Sensors", 2007 International Image Sensor Workshop, Ogunquit, Maine, USA

2.5 µm Pixel Linear CCD

Nixon O, Lei Wu, Melanie Ledgerwood, John Nam, Jonathan Huras

DALSA Inc.
605 McMurray Road, Waterloo, ON, N2V 2E9, Canada
Tel.: (519) 886-6001 x2248, Fax: (519) 886-5767, E-mail: nixon.o@dalsa.com

1. Introduction

Machine vision systems are constantly being pushed to inspect objects at higher spatial resolution. These systems are cost constrained to keep the total length of the imaging region below 65 mm. Sensors with imaging regions that are longer than about 60 mm require lenses that are costlier and are not readily available. This imaging region length constraint, along with the need for higher spatial resolution, has pushed the development of smaller pixel sensors.

The pixel sizes of successive generations of linear CCDs have historically decreased by a factor of the square root of two. Earlier generations of linear sensors have 14, 10 and 7 µm pixels. We reported 5 µm pixel linear CCDs in 2005 [1]. Currently, 3.5 µm pixel linear CCDs for color image scanners are available in the market [2]. We report the next step in this evolutionary trend, the 2.5 µm pixel linear sensor.

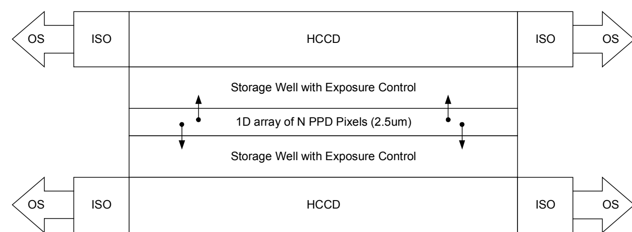
2. Sensor Architecture

We have fabricated and tested two variants of the 2.5 µm pixel sensor. The architectures of sensors are shown in Fig. 1. Alternate pixels or pixel blocks are read out using separate shift registers. Although Fig. 1 indicates four corner outputs, the sensor is fabricated in a CCD process that permits structural blocks to be stitched [3]. The blocks can be patterned during wafer processing to produce sensors of different lengths and with more outputs.

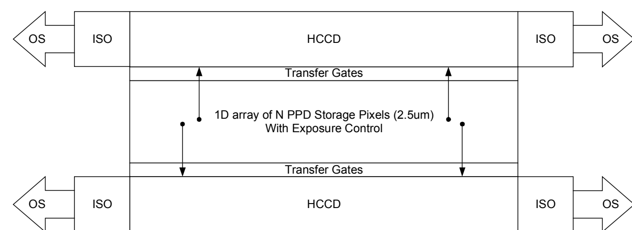
Although the 2.5 µm pixel sensor is functionally similar to sensors with larger pixels, there are a number of new considerations that arise in the new sensor.

3. Full Well and Antiblooming

The first consideration is the full well capacity. Unlike area imagers, reducing the pixel size in linescans does not necessarily result in lower full well. In linear sensors, photogenerated charges can either be stored in a storage gate adjacent to the photosensitive area (see Fig. 2) or stored in an elongated pinned photodiode (see Fig. 3). Both types of storage structures can be sized to store the same amount of charge as larger pixel sensors. Our 2.5 µm pixel sensor has a full well of at least 60,000 electrons. The 2.5 µm pixel sensor has the same full well as the 5 µm pixel sensor.



(a)



(b)

OS = Output Structure, ISO = Isolation Registers, HCCD = Horizontal CCD

Figure 1
Sensor Block Diagram with Two Pixel Variants (a) and (b)

Each of the two pixel structures has its advantages and disadvantages.

The storage gate pixel structure allows a more precise control of the full well capacity since the full well capacity can be adjusted using the storage gate bias. In applications where very high level of antiblooming (> 100x) is required, the pixel capacity can be reduced to increase the headroom between pixel saturation and the onset of blooming. The level of antiblooming can be adjusted by at least an order of magnitude using this method. The mere presence of an antiblooming drain does not automatically result

in an arbitrarily high level of antiblooming because the charge draining capacity of the antiblooming gate and drain can determine an antiblooming limit. This limit is more evident in 2.5 μm pixels since the dimensions of the antiblooming drains are very small. As a result, the current density through the antiblooming drain can be quite high.

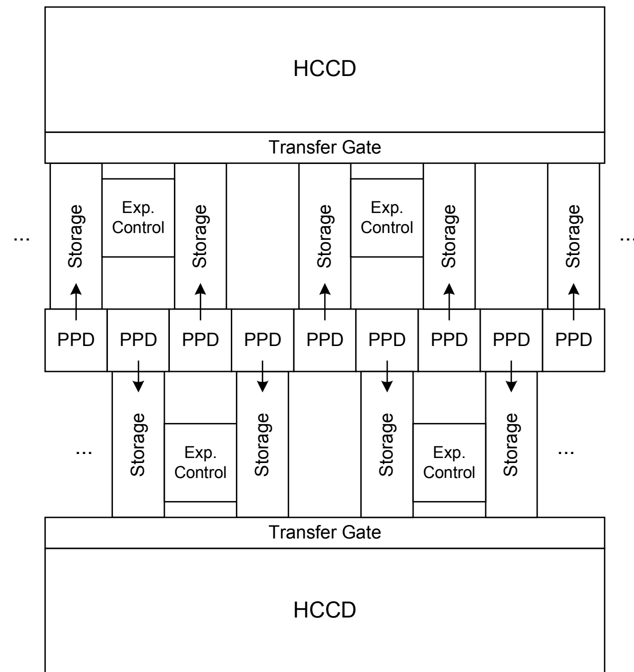


Figure 2
Block Diagram of the Storage Gate Pixel Structure

The pinned photodiode storage pixel structure has lower dark current and is more tolerant of exposure to high energy radiation. The full well capacity of this structure is fixed by geometry and by the channel potential of the pinned photodiode. To achieve at least 60,000 electrons of pixel capacity in a 2.5 μm pixel size, the pinned photodiode portion of the pixel has to be quite long. When charges are read out from the pixel, the charges move primarily because of charge diffusion. Because the diffusion time is proportional to the square of the distance, a larger full well results in a longer or an incomplete readout.

4. Exposure Control

Exposure control is important in many machine vision applications because it allows the number of signal electrons collected to remain constant while the web speed is ramping up or down, or when the arrival time of the object to be scanned is indeterminate. Because the exposure control and pixel transfer gates generate different fringing electric field distribution to the charge storage area, the two gates have different effects on traps in the storage area. These exposure control traps result in isolated pixels exhibiting nonlinear pixel response. The nonlinear behaviour cannot normally be removed by calibration or software correction.

In the new 2.5 μm pixel process, we made significant improvements to passivation and gettering steps in the fabrication process to minimize the number of traps. We have reduced the number of traps by at least an order of magnitude. The same processing steps have also yielded dark current levels that are lower by an order of magnitude.

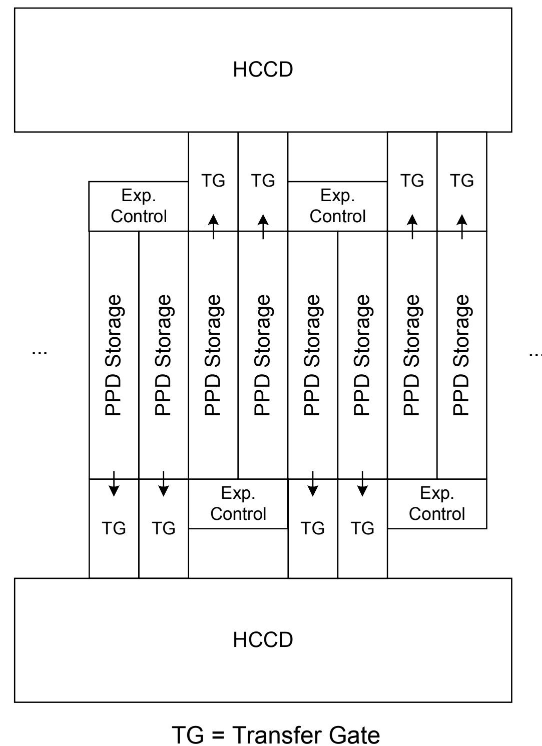


Figure 3
Block Diagram of the PPD Storage Pixel Structure

Exposure control traps can also appear as a result of pixel design, even without material non-idealities. The 2.5 μm storage gate pixel structure introduced unique design challenges since we had to incorporate a pinned photodiode photosite, a storage gate, an exposure control/antiblooming gate, an antiblooming drain, and a pixel readout gate in a very confined space. Each of these gates is affected by short and narrow channel effects, both of which become significantly more prominent at 2.5 μm pixel dimensions, where gate dimensions can be as small as 0.5 μm. We have carefully designed the pixel so that the short and narrow channel effects do not form unintended design traps in the charge transfer path.

5. MTF and QE

Linescans are normally fabricated in a relatively thick (15 to 20 µm) p- epitaxial layer grown on top of a p+ silicon substrate. Photoelectrons are generated throughout the p-epi. This thick charge generation region ensures good quantum efficiency in the red and near infrared. This is advantageous since the tungsten halogen bulbs commonly used in industrial inspection have significant red and infrared outputs.

The depletion region of the pinned photodiode does not normally extend much deeper than 5 µm from the silicon-oxide interface. Electrons diffuse randomly in the field free region underneath this depletion layer. The charge diffusion in the field free region of the epi results in the degradation of the modulation transfer function (MTF). Despite this MTF degradation, in 5 µm pixel sensors, the trade-off still favors thick epi because the effect in red and infrared sensitivity is large while the degradation in MTF is small.

In a 2.5 µm pixel imager however, the degradation in MTF due to charge diffusion becomes a lot more significant. We calculated the MTF for 650 nm illumination for 5, 3.5, and 2.5 µm pinned photodiode pixels with a 17 µm thick epi, using a model [4] that has been corroborated by measurements on a 5 µm pixel. The results are shown in Fig. 4.

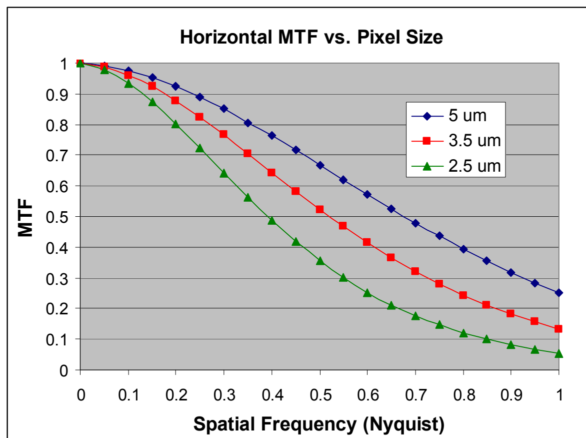


Figure 4
Linescan Horizontal MTF as a Function of Pixel Size

If we choose an acceptable MTF threshold of 30%, the 5 µm pixel is usable up to 93 lp/mm (93% of Nyquist), the 3.5 µm pixel is usable up to 103 lp/mm (72% of Nyquist), and the 2.5 µm pixel is usable up to 110 lp/mm (55% of Nyquist). These numbers suggest that there is no resolution benefit in using pixels that are smaller than 5 µm with a 17 µm thick epi. The spatial resolution benefit of a smaller pixel is negated by the degradation in MTF due to charge diffusion.

While it is theoretically also possible to improve the MTF of small pixels by increasing the depletion depth of the pinned photodiode using a more lightly doped epi, in practice, it is difficult to extend the depletion depth of the pinned photodiode without concurrently overextending the depletion region of the CCD photogates.

To bring the MTF of the 2.5 µm pixel back to around 30% at Nyquist, we have to limit the thickness of the field free region in the epi. We calculated that the epi of a 2.5 µm pixel should not be more than 5 µm thick.

The ratio of epi thickness to pixel size (17/5 = 3.4, 5/2.5 = 2) is smaller for smaller pixels. The pixel size dependence of the epi thickness required to achieve a minimum acceptable MTF is non-linear because the charge diffusion distance does not scale with pixel size. On smaller pixels, a higher percentage of photogenerated charges can diffuse to adjacent pixels.

A thinner epi will improve MTF but degrade the red and infrared response. The spectral response of a pinned photodiode pixel in 17 and 5 µm epi is shown in Fig. 5. The quantum efficiencies are calculated using a model that has been corroborated by measurements on 17 µm epi.

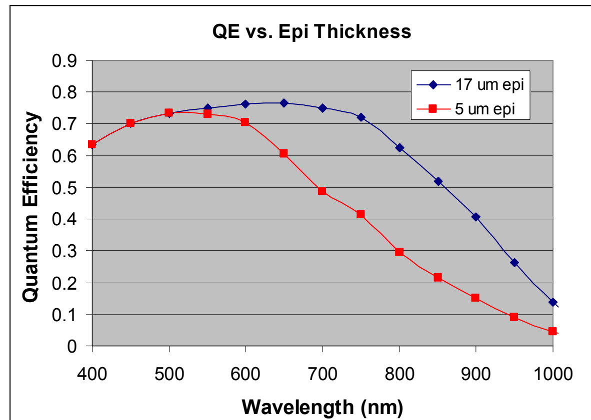


Figure 5
Spectral Response as a Function of Epi Thickness

The spectral response suggests that a transition to 2.5 µm linescan pixel needs to be accompanied by a reduction in the wavelength of illumination, perhaps through the use of high output LEDs.

6. Speed and Noise

Another important consideration is noise at high readout speeds. The odd and even pixels of the 2.5 μm pixel sensor read out in oppositely placed CCDs. As a result, the readout CCDs have 5 μm pitch. The 5 μm shift registers are two-phase CCDs with separately biased barrier and storage phases. The CCDs operate with 4.5V clocks.

Although the charge transfer efficiency of the sensor remains nearly ideal (> 0.99999) at readout speeds exceeding 60 MHz, we operate linescans at 40 MHz per output to strike a balance between noise, speed, electronic complexity, and temperature stability. Correlated double sampling becomes less effective at readout speeds that are greater than 40 MHz. In arrays with multiple outputs, crosstalk between outputs becomes more untenable at output speeds of over 40 MHz.

Machine vision systems have constantly pushed for faster inspection speeds, which we accommodate through the use of parallel outputs. Assuming no improvements in illumination, the increasing line rates will result in the push for lower readout noise.

One method of reducing the readout noise is by increasing the charge conversion efficiency (CCE) of the output node. While area CCDs have CCE's that routinely exceed 40 μV/e and CMOS imagers have CCE's with twice this value, machine vision linescans have CCE's that remain near 14 μV/e. This is mainly because the processes used to fabricate 60 mm long linescan arrays do not have the design rules necessary to achieve higher CCE. The use of a stitched process separated these two constraints and allowed us to break this barrier. We have achieved 18 μV/e in the new process and believe that a CCE between 20 to 25 μV/e is possible with optimization. While this number is admittedly below the state of the art for CCDs, it is the highest available in a high speed linescan CCDs. There are two factors that constrain the CCE in high speed linescans. The first is the large amplifier bandwidth requirement, which forces the dimensions of the input FET to be larger than the FET dimensions in slower speed devices. The second is p-epi substrate. Unlike processes with p-well on n-substrate, the substrate of the amplifier FETs cannot be connected to the source to mitigate the body effect. The body effect results in lower amplifier gain. We achieve an average readout noise of approximately 25 electrons rms at readout speed of 40 MHz.

7. Conclusions

We have successfully designed and fabricated a 2.5 μm pixel linear CCD. This represents the next step in the evolution towards smaller pixel sizes.

We discussed the various considerations and trade-offs associated with 2.5 μm pixel linescans, including the trade-off between full well capacity, antiblooming, and pixel readout duration; the need to consider short and narrow channel efforts in the exposure control structure; the system level trade-off between MTF, red quantum efficiency, and wavelength of illumination; and the trade-off between speed, noise, and sensitivity.

REFERENCES

[1] B. Benwell, N. O, G. Allan, J. Huras, and M. Ledgerwood, "12k 5-μm linescan CCD sensor with 320-MHz data rate", 2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 10-12, 2005, Karuizawa, Nagano, Japan.

[2] Sony ILX555K (http://products.sel.sony.com/semi/PDF/ILX555K.pdf)

[3] G. Kreider and J. Bosiers, "An mKxnK bouwblok CCD image sensor family. I. Design", IEEE Trans. On Electron Devices, vol. 49, no. 3, March 2002, pp. 361-369.

[3] D. Barbe, "Imaging devices using the charge-coupled concept", Proc. IEEE, vol. 63, Jan 1975, pp. 38-67.

Performance of NIR InGaAs imager arrays for science applications

S. Seshadri[a], D.M. Cole[a], B. Hancock[a], P. Ringold[a], C. Peay[a], C.Wrigley[a], M. Bonati[b], M.G. Brown[c], M. Schubnell[c], G. Rahmer[b], D. Guzman[b], D. Figer[d], G. Tarle[c], R.M. Smith[b], and C. Bebek[e]
[a]Jet Propulsion Laboratory, [b]California Institute of Technology, Pasadena, CA, [c]University of Michigan, Ann Arbor, MI, [d]Rochester Institute of Technology, Rochester, NY and [e]Lawrence Berkeley National Laboratory, Berkeley, CA, Department of Physics
MS 300-315, Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, CA, USA 91109, Email: suresh.seshadri@jpl.nasa.gov; PH: (818)-354-8370

Despite its many potential advantages, the use of InGaAs-based arrays for scientific imaging in the near-infrared is minimal[1] and not widespread. For example, InGaAs imaging arrays are used in commercial Dense Wavelength Division Multiplexing (DWDM) telecommunications, military and aerospace applications.[2,3] In terms of performance, InGaAs detectors with high, flat QE already exist.[2] Technologically, a transparent InP substrate and substrate removal technology, such as that used to increase short wavelength performance and minimize cut-off wavelength non-uniformities and cosmic ray effects in HgCdTe, also exists. These advantages offer imagers based on InGaAs technology the potential to be a lower cost, higher reliability alternative to those based on HgCdTe. The work described herein provides more complete characterization of the low temperature performance of an InGaAs-based imager array than presently exists to assess the suitability of this technology for scientific imaging applications.

We characterized a nominally 1.7um cut-off wavelength 1kx1k InGaAs (lattice-matched to an InP substrate) photodiode array fabricated by Sensors Unlimited, Inc. (now Goodrich Corporation). The array was hybridized to a Rockwell H1RG multiplexer under the Lawrence Berkeley National Laboratory-led SuperNova/Acceleration Probe (SNAP) mission concept development program.[4,5,6] The detector was operated in the H1RG's slow readout mode, with buffered output, with an external current source.

The mean-variance and conversion gain (C_g) for the InGaAs detector are shown in Figures 1 and 2.[7] Note that the engineering definition of C_g (uV/e-) differs from the astronomers' definition (e-/DN, where DN=Digital Number or e-/ADU, where ADU=Analog-Digital Unit). We call the latter, the inverse gain (=1/C_g). From the figure, it is apparent that C_g is signal-dependent, with noticeable deviation from constancy at signal levels as low as 10-15 % of full scale. The interpixel capacitance factor was calculated to be 0.87, resulting in a ~13% gain error.[8,9] Thus, the resulting low signal *inverse* gain is 6.3 e-/DN. The measured linearity and full well, calculated using the conversion gain data, are illustrated in Figure 3. The full well for a 0.5V detector bias was calculated to be 435K e-.

Figure 4 illustrates the relative QE of the InGaAs detector at 140K. The curve has been adjusted to achieve the same maximum absolute 300K QE data. A nominal room temperature curve is also shown in the figure for comparison. It is evident that the spectral shape is retained, with the wavelength being shifted towards shorter wavelengths due to the band gap shift of the detector band edge. The shift corresponds to ~80nm shorter cut-off wavelength at 140K relative to 300K. This result is a bit higher than the ~100 nm shift expected using the 0.625 nm/K rate expected from theory.[10] However, the data correlates well with recent results obtained by others.[11]

Figure 5 illustrates histograms of the dark current at various temperatures. Figure 6 illustrates an Arrhenius plot of the temperature dependence of the mean dark current. The curve is relatively well behaved with an extrapolated value that matches nominal room temperature data. The calculated activation energy of 0.25 eV is a bit lower than the 0.37 eV expected for purely generation-recombination in the depletion region. The flattening of the dark current at low temperatures is thought to be due to the effect of photo-generation from diffuse cosmic rays in the InP substrate, as has been observed for non-substrate-removed HgCdTe.[6] Figure 7 illustrates the noise performance of the InGaAs focal plane array versus sampling depth. Secondly, while the electronics noise is well behaved, decreasing in line with the expected square root dependence with increasing Fowler sample, the excess detector noise does not. Persistence in the InGaAs detector, Figure 8, is seen to decay to <0.1% of the original signal level almost instantaneously, with a subsequent, well-behaved, 55 sec decay constant.

In conclusion, the low temperature performance of existing InGaAs detector technology is well behaved and sufficient for all but the most stringent scientific applications. The results presented are comparable to those obtained from existing HgCdTe imagers. The key differences observed are the magnitude of the temperature-

dependent shift in cut-off wavelength and the fact that the read noise is higher than that obtained for the most recently-developed HgCdTe.

ACKNOWLEDGEMENTS

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REFERENCES

1. R.J. van der A et al., *Low noise InGaAs infrared (1.0-2.um) focal plane arrays for SCIAMACHY,* SPIE Proceedings V2957, 1997, p54.
2. T. Martin, et al., *640-512 InGaAs focal plane array camera for visible and SWIR imaging*, Infrared Technology and Applications XXXI, edited by Bjørn F. Andresen,Gabor F. Fulop, Proc. of SPIE Vol. 5783 (SPIE, Bellingham, WA, 2005, p12.
3. A. Hoffman et al., *Megapixel InGaAs Arrays for Low Background Applications,* Infrared Technology and Applications XXXI, edited by Bjørn F. Andresen,Gabor F. Fulop, Proc. of SPIE Vol. 5783 (SPIE, Bellingham, WA, 2005, p32.
4. M.G. Brown, *Development of NIR Detectors and Science Driven Requirements for SNAP*, Astronomical Telescopes and Instrumentation 2006, Proc. SPIE 6265 paper 113.
5. M. Schubnell et al., *Near infrared detectors for SNAP*, Astronomical Telescopes and Instrumentation 2006, Proc. SPIE 6276 paper 29.
6. R. Smith, et al., *Noise and zero-point drifts in 1.7um cutoff detectors for SNAP,* Astronomical Telescopes and Instrumentation 2006, Proc. SPIE 6276 paper 30.
7. B. Pain and B. Hancock, *Accurate Measurement of Conversion Gain and Quantum Efficiency in CMOS Imagers,* IS&T/SPIE 15th. Annual Symposium, Sensors, Cameras, and Systems for Scientific/Industrial Applications Conference 5017A, January 22, 2003.
8. A. Moore et al., Proc. SPIE V. 5167 (2003).; A. Moore et al. *QE overestimation and Deterministic Crosstalk Resulting from Interpixel Capacitance*, Optical Engineering, V 45-7.; G. Finger, et al., *Conversion Gain and Interpixel Capacitance of CMOS Hybrid Focal Plane Arrays*, Proc. Scientific Detectors for Astronomy 2005, Eds. J.E. Beletic, P. Amico, Springer Astrophysics and Space Sciences Library, V336, 477-490.
9. Autocorrelation calculation performed by M. Bonati of California Institute of Technology, Department of Astronomy, Optical Observatories group.
10. V.A. Wilkinson and A.R. Adams, *The effect of temperature and pressure on InGaAs band structure,* Properties of lattice matched and strained InGaAs, P. Bhattacharya, ed., INSPEC EMI Series 8, 1993.
11. R. Guntupalli and R. Allen, *Evaluation of InGaAs camera for scientific near infrared imaging applications*, in Infrared and Photoelctronic Imagers and Detector Devices II, R.E. Longshore and A. Sood editors, Pric. SPIE V6294, (2006) p.1.

FIGURES

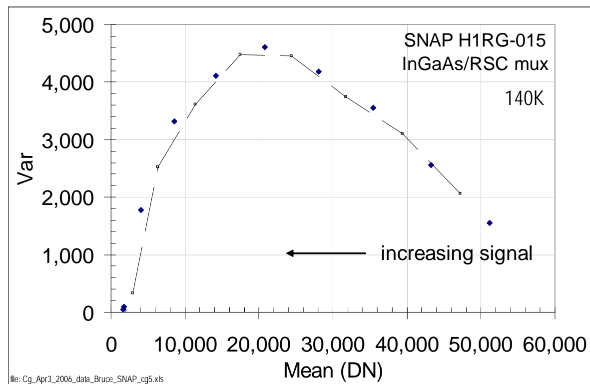

Figure 1: Mean-variance curve for an InGaAs detector biased at 0.5 V at 140K.

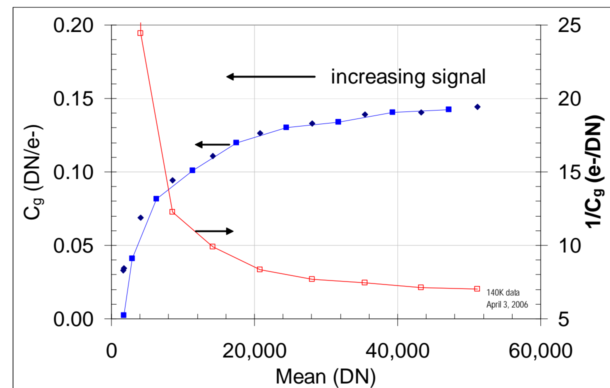

Figure 2: Conversion gain plot at 140K. Each data point represents a spatial average of 6-frame temporal variance from each of a 32x32 block of pixels.

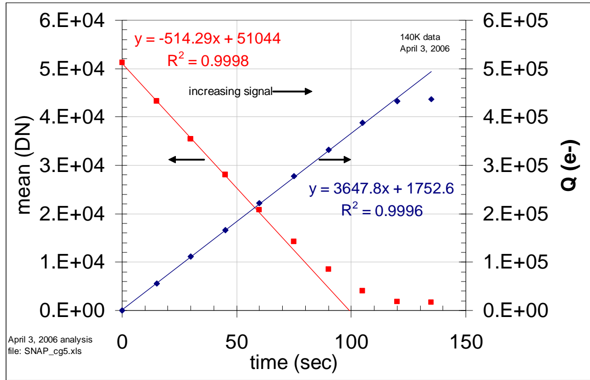

Figure 3: Linearity and full well of the InGaAs/mux hybrid package at 140K. The (red) line corresponds to a linear fit to the first 5 points in the mean data.

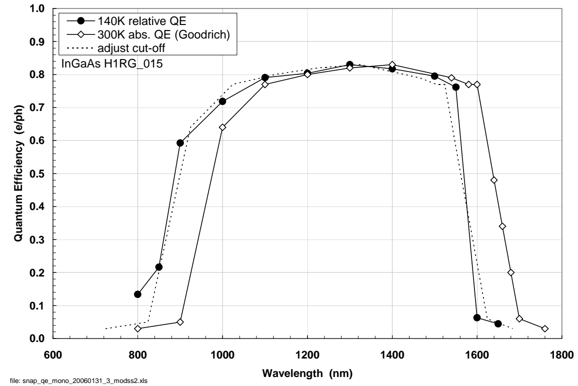

Figure 4: Relative quantum efficiency of the InGaAs detector at 140K. The dashed curve overlaying the 140K data is a copy of the 300K curve, shifted by 76 nm.

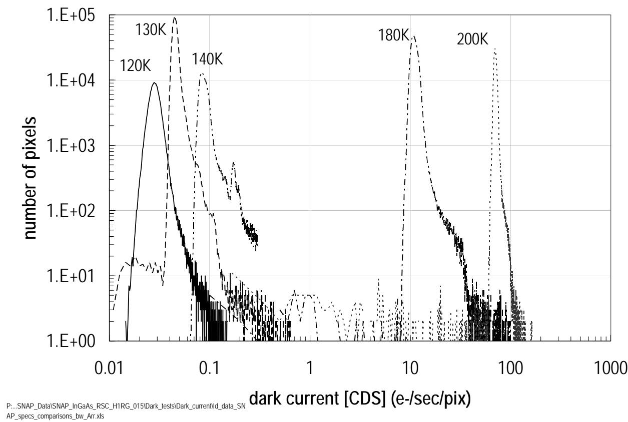

Figure 5: Dark current histograms at selected temperatures.

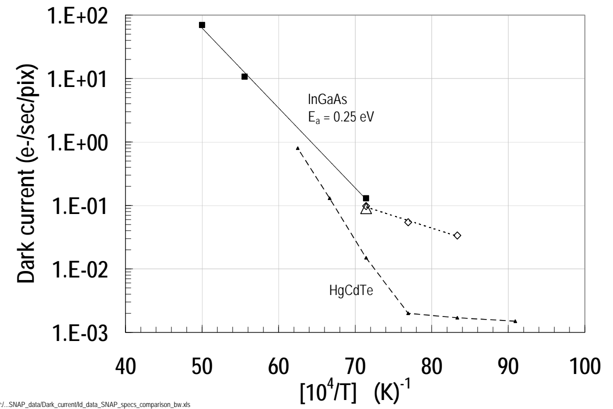

Figure 6: Arrhenius plot of dark current for InGaAs and state-of-the-art HgCdTe.

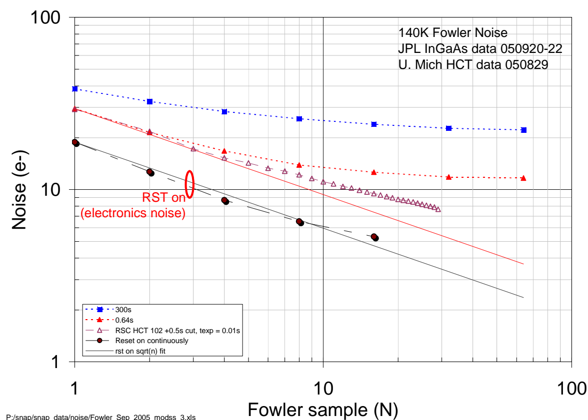

Figure 7: Noise vs number of samples at integration intervals of 0.64s and 300s. A curve of the electronics noise of our setup, scaled by C_g is shown for comparison.

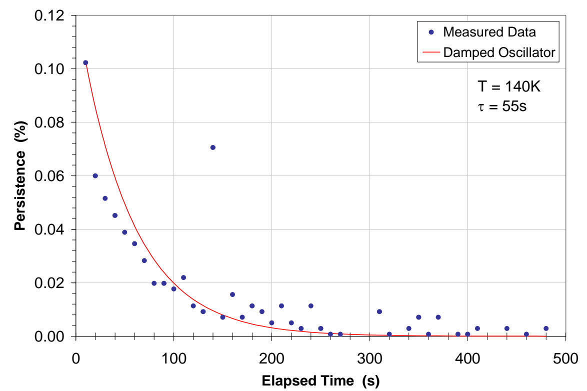

Figure 8: 140K persistence data for an InGaAs focal plane array. The initial illumination level was ~80% of full well.

2007 International Image Sensor Workshop Participants

First Name	Last Name	Afflilation
Kenichi	Abe	Graduate School of EngineeringTohoku University, Japan
Gennadiy	Agranov	Micron Technology Inc, USA
Salman	Akram	Micron Technology Inc, USA
Juha	Alakarhu	Nokia, Finland
Hiroaki	Ammo	Sony Corporation, Japan
Bernard	Aspar	SOITEC, France
Thomas	Baechler	CSEM, Switzerland
Alex	Belenky	Ben-Gurion University of Negev, Israel
Morley	Blouke	Ball Aerospace and Technology Corporation, USA
Jan	Bosiers	DALSA Corporation, The Netherlands
Richard	Bredthauer	Semiconductor Technology Associates, Canada
Barry	Burke	MIT Lincoln Laboratory, USA
Sophie	Caranhac	E2V, France
Peter	Centen	Grass Valley, The Netherlands
Chung-Wei	Chang	TSMC, ROC
Eduardo	Charbon	EPFL, Switzerland
Ho-Ching	Chien	PixArt Imaging Inc., ROC
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Kwang-Bo	Cho	Micron Technology Inc., USA
Seong-Ho	Cho	Samsung Electronics Company Ltd., Korea
Thomas	Cunningham	Jet Propulsion Laboratory, USA
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Tobi	Delbruck	UNI-ETH Zurich, Switzerland
Donal	Denvir	Andor Technology, UK
Grzegorz	Deptuch	Brookhaven Laboratory, USA
Bart	Dierickx	Caeleste; IMEC, Belgium
Taner	Dosluoglu	Dialog Imaging System Inc., USA
N	Egami	NHK Science & Technical Research Labs, Japan
John	Ellis-Monaghan	IBM, USA
Keith	Findlater	Gigle Semiconductor, UK
Eric	Fossum	Siimpel Corporation, USA
Boyd	Fowler	Fairchild Imaging Inc., USA
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Hiraoki	Fujita	Eastman Kodak Company, USA
Jeff	Gambino	IBM, USA
Arie	Gavriely	Advasense Technologies, Israel
Alexander	Getman	Samsung Electronics Company Ltd., Korea
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Lindsay	Grant	ST Microelectronics, UK
Tomas	Guerts	Cypress Semiconductor, Belgium
Roman	Gutierrez	Siimpel Corporation, USA
Homayoon	Haddad	Magnachip Semiconductor, USA
Takayuki	Hamamoto	Tokyo University of Science, Japan
Hyung-Jun	Han	MagnaChip, Korea
Robert	Henderson	Univ Edinburgh, UK
Jochem	Herrmann	Adimec, The Netherlands
Ken	Hoagland	KAH Engineering Services, USA
Jed	Hurwitz	Gigle Semiconductor, UK
Joon	Hwang	Dongbu Company Ltd., Korea

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First Name	Last Name	Afflilation
Jerry	Hynecek	Magnachip Semiconductor, USA
Yoshirin	Iida	Toshiba Corporation, Japan
Manuel	Innocent	Cypress Semiconductor, Belgium
Masaaki	Iwane	Canon Inc., Japan
Keiichiro	Kagawa	Nara Institute of Science and Technology, Japan
Nobuhiro	Karasawa	Sony Corporation, Japan
Shoji	Kawahito	Shizuoka University, Japan
Craig	Keast	MIT Lincoln Laboratory, USA
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Tadakuni	Narabu	Sony Corporation, Japan
David	Ng	Nara Institute of Science and Technology, Japan
Shouleh	Nikzad	Jet Propulsion Laboratory, USA
Tetsuo	Nomoto	Sony Corporation, Japan
Nixon	O	DALSA Corporation, Canada
Paul	O'Connor	Brookhaven National Laboratory, USA
Se Jung	Oh	SiliconFile Technologies Inc., Korea

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First Name	Last Name	Afflilation
Jun	Ohta	Nara Institute of Science and Technology, Japan
Yusuke	Oike	Sony Corporation, Japan
Kee-Hyun	Paik	Samsung Electronics Company Ltd., Korea
Bedabrata	Pain	Jet Propulsion Laboratory, California Institute of Technology, USA
Armand	Peizerat	CEA-LETI, France
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Shri	Ramaswami	Foveon, Inc, USA
Padmakumar	Rao	Delft University of Technology, The Netherlands
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Francois	Roy	ST Microelectronics, France
Tomonari	Sawada	Shizuoka University, Japan
Don	Scansen	Semiconductor Insights Inc., Canada
Jens-Uwe	Schulssler	University of Dresden/ Infineon, Germany
Johannes	Solhusvik	Micron Technology, Norway
David	Stoppa	ITC-IRST, Italy
Graeme	Storm	ST Microelectronics, UK
Richard	Stover	University of California, Santa Cruz, USA
Shigetoshi	Sugawa	Tohoku University, Japan
Vyshnavi	Suntharalingam	MIT Lincoln Laboratory, USA
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Keichi	Tachikawa	Matsushita Electric Industrial Co, Japan
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Hidekazu	Takahashi	Canon Inc., Japan
Isao	Takayanagi	Micron Japan Ltd., Japan
Nagataka	Tanaka	Toshiba America, USA
Jose	Tejada	Texas Instruments, Japan
Nobukazu	Teranishi	Matsushita Electric Industrial Co, Japan
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Arnaud	Tournier	ST Microelectronics, France
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Paul	Vu	Fairchild Imaging Inc., USA
Xinyang	Wang	Delft University of Technology, The Netherlands
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