CMOS image sensor with two-shared pixel and staggered readout architecture

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***Abstract*—A two-shared pixel architecture is presented that uses a staggered readout circuitry approach. It is used in a very high resolution and large area CMOS image sensor manufactured in a 0.18 µm CIS technology. The benefit in using this sharing approach lies in the more uniform cross talk behavior and angular response compared to the conventional sharing architectures. Moreover, the manufacturing yield is expected to be higher if a number of defect single lines can be tolerated in the envisaged application.**

***Index Terms*-- CMOS Active Pixel Sensor (APS), pixel sharing, staggered readout, pixel uniformity, manufacturing yield.**

I. INTRODUCTION

Over the recent years, the pixel size in CMOS image sensors for consumer applications has been drastically reduced. One of the solutions to further shrink the pixel size while maintaining the pixel performance is the sharing of readout circuitry between neighboring pixels. However, it is also well-known that conventional sharing architectures can lead to severe pixel-to-pixel differences in cross talk behavior and angular response [1][2]. In this paper, we present a two-shared pixel approach using staggered readout that reduces non-uniform pixel characteristics.

The pixel architecture that is described in this paper is used in a large area, very high resolution CMOS image sensor that is manufactured in a 0.18 µm CIS technology. Uniform MTF behavior is required across the pixel array. Recently, a similar pixel architecture has been described [3], however, with a different purpose and therefore slightly deviating solution.

In the first section of the paper, the concept of two-shared pixels with staggered readout circuitry is discussed. The main advantages in terms of pixel-to-pixel uniformity of sensitivity and MTF, and yield are explained. The technique can also be used to add redundancy into the readout circuitry and can be applied to color devices. In a second section, a more detailed layout of the pixel is shown and first results of test pixels are described.

II. CONCEPT OF STAGGERED READOUT CIRCUITRY

The typical arrangement of a 2.5T/pixel two-shared pixel is shown in Figure 1. The pixel building block has a reset and select line, two transfer lines and a single column bus. Compared to non-shared pixels, the obvious advantage is that less readout circuitry is required in the pixel array (i.e. results in more area for photodiodes) and that only 2 instead of 3 horizontal metal lines need to be routed per pixel pitch.

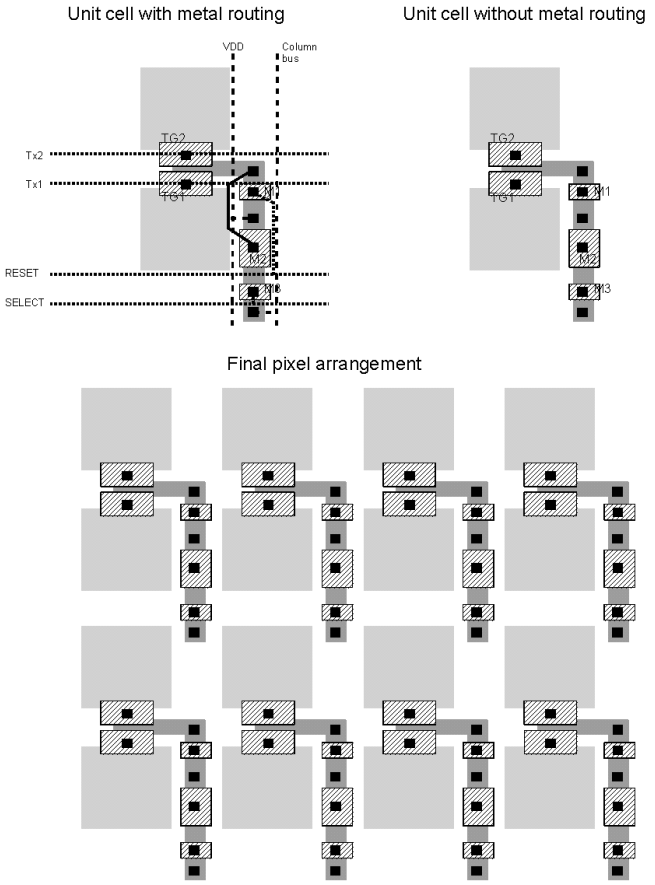

Figure 1. Conventional two-shared pixel architecture. Unit cell (top) and final pixel arrangement (bottom).

This arrangement, however, cannot be used for the envisaged application as it leads to an asymmetrical pixel configuration. Moreover, the manufacturing yield could be degraded to an unacceptably low level. Figure 2 shows a typical example of correction patterns in case of defect pixels. The figure shows five by five pixel blocks of which the pixel in the center is defect (black), i.e. the pixel exhibits out of specification performance. Pixels used to correct the defect pixel by interpolation are indicated in dashed light grey. As can be seen from this example, a defect pixel can be corrected

in case the defect pixel has two non-defect neighboring pixels along a vertical, horizontal or diagonal axis (top row); or at least two out of four non-defect neighboring pixels on horizontal or vertical axis (bottom row). As a consequence, small cluster defects (e.g. 2x2 defect pixels, 5 defect pixels in 3x2 window) are allowed. Pixels of two neighboring defect rows or columns can, however, not be corrected.

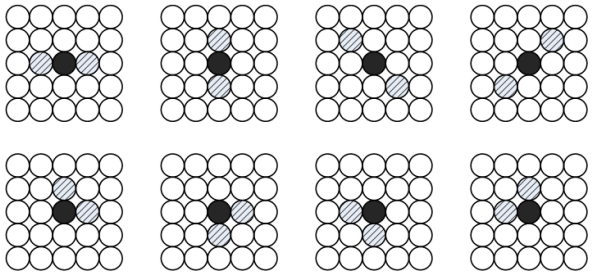

Figure 2. Example of possible correction patterns for defects pixels.

The application does not allow non-correctable defect rows or columns, and only a limited set of small cluster defects. Since a single reset and single select line are used for two neighboring rows in the conventional sharing method, processing defects (short or open circuit on metal lines) would immediately result in a defect sensor. Since the sensor is a large area device, such defects are to be expected in a reasonable number of devices on the wafer. Therefore, this conventional sharing architecture would lead to an unacceptable manufacturing yield. The same holds for shorted neighboring transfer lines as they run next to each other across the complete pixel array.

To avoid this low yield, we use still the same approach of vertically sharing readout circuitry for two photodiodes, but contrarily to the conventional sharing approach, the readout circuitry of adjacent photodiodes on the same row are placed in a staggered manner. This pixel arrangement is shown in Figure 3. The advantage of this sharing architecture is that still less readout circuitry is required in the pixel array and that the capacitive load due to junctions and gate capacitances on the column bus, reset as well as select lines is reduced by a factor of two. This is important for large area, large resolution sensors that need to be readout relatively fast. Compared to the pixel of Figure 1, this approach requires however 3 horizontal metal lines to be routed per pixel pitch (like the non-shared pixel) instead of 2. The latter could be regarded as a drawback; however it is beneficial for final sensor manufacturing yield even though the number of metal lines is increased.

Figure 4 illustrates how single defect lines translate in defect pixels on the sensor in case of this new pixel sharing approach with staggered readout. A single defect transfer line (top left) results in a different defect pixel configuration as a single defect row/select line (bottom left). A single defect line results in most cases in a single correctable defect line. Note that in one of two cases a single defect row/select line combined with defect column results in two non-correctable pixels at the crossing. Light grey defect pixels are correctable pixels according to the definition used in Figure 2, black defect pixels are not correctable.

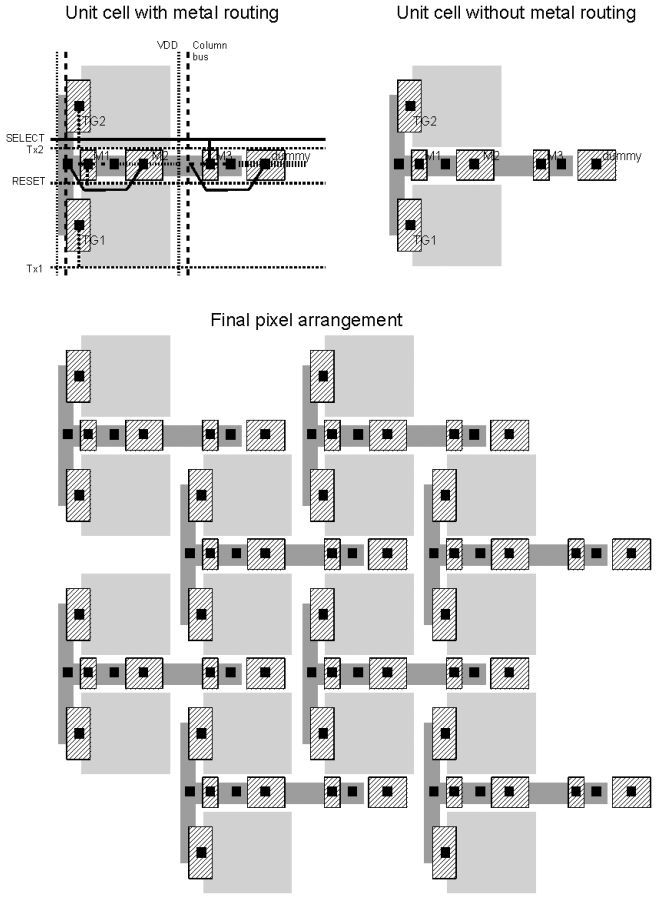

Figure 3. Used two-shared pixel architecture with staggered readout. Unit cell (top), final pixel arrangement (bottom).

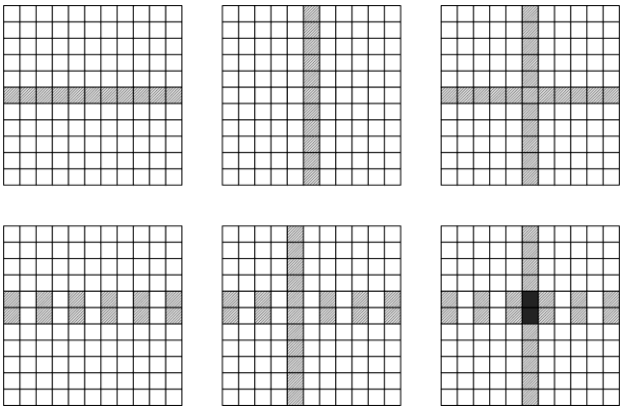

Figure 4. Defect pixels resulting from single defect lines in case of the used two-shared pixel architecture with staggered readout.

The extra area that is freed by sharing the readout circuitry of pixels can also be traded against further yield improvement. A yield problem can occur when the select line of a particular row is stuck to a high voltage. In such case, the readout of

other rows is disturbed resulting in a bad device even in case single defect rows would be tolerated. Figure 5 shows a shared pixel where a second select transistor is added in series. In such pixel, even if one of the select lines is stuck to a high voltage, the pixels of the particular row can still be disconnected from the column bus lines through the second select line.

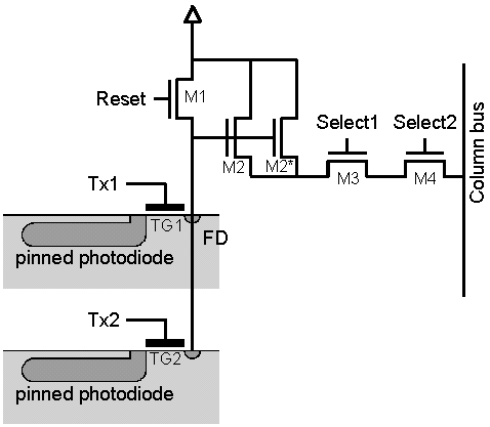

Figure 5. Shared pixel with double select gate to improve final device yield.

The pixel of Figure 5 has also an additional source follower M2*. This can be beneficial for noise performance and readout speed.

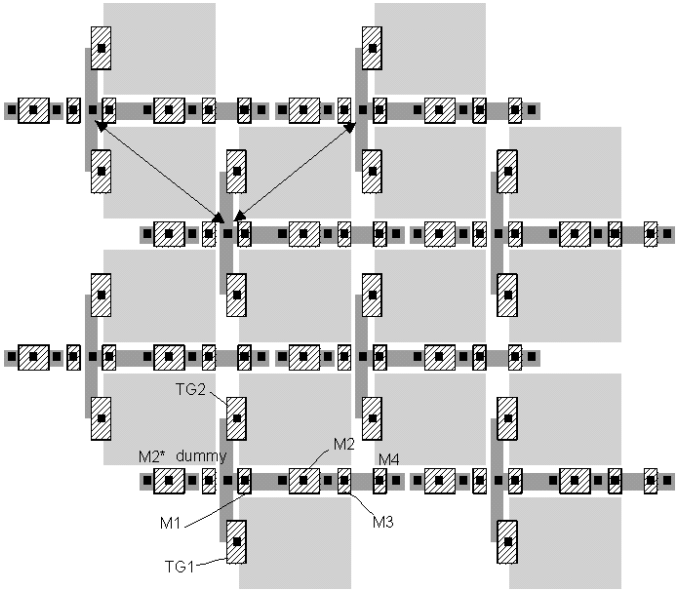

Figure 6. Possible final pixel arrangement of pixel from Figure 5.

Figure 6 shows a possible pixel arrangement for the pixel of Figure 5. Compared to non-shared pixels, the area used for readout circuitry is very similar. However, by sharing readout circuitry and having a staggered readout configuration, the final device yield can be improved and the readout speed can be increased, which are important advantages for high resolution and large area sensors.

The concept can also be applied to color devices. Figure 7 shows a pixel unit cell for a two-shared pixel with staggered readout that could be used in combination with a color filter array (CFA). This proposed configuration is different from the one described in [3]. The two photodiodes that share their readout circuitry are positioned diagonally with respect to each other.

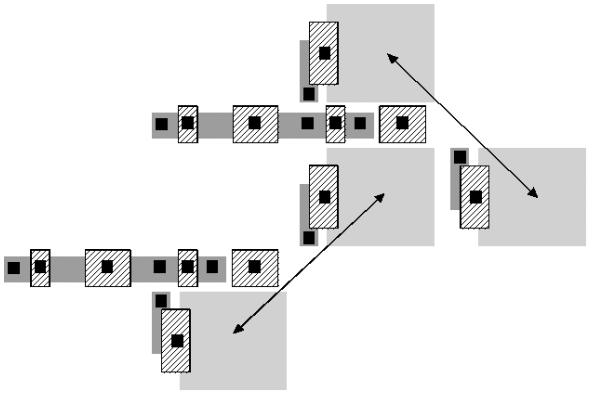

Figure 7. Pixel unit cell for two-shared pixel with staggered readout and use of color filter array.

The sharing configuration that is shown in Figure 7 is not the only possible solution and also different CFA implementations could be used. A possible combination with the proposed sharing architecture is shown in Figure 8.

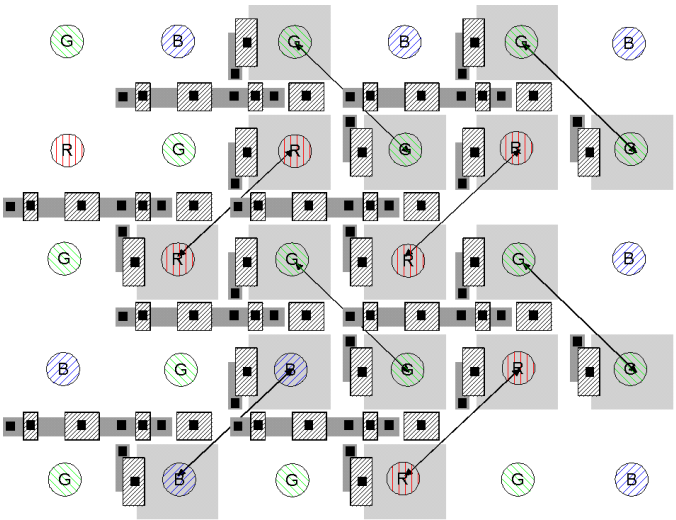

Figure 8. Pixel arrangement and possible color filter array implementation (variants possible).

Since all pixels have basically the same layout, any imbalance in sensitivity is reduced. Compared to the implementation in [3] (not matching sensitivity characteristics for monochrome devices), also binning of two pixels of the same color can be implemented. Alternatively, using the pixel arrangement of Figure 3, the resulting image could also be composed of the complementary colors. This is illustrated in Figure 9. The CFA kernel is a slightly modified Bayer pattern. Binning on this shared array will result in four types of binned pixels: Cy, Ye, Mg and G. From these binned pixels, a color filter image at one fourth of the full resolution can be reconstructed. Alternative schemes can be thought of, e.g. starting from a complementary CFA system in full resolution.

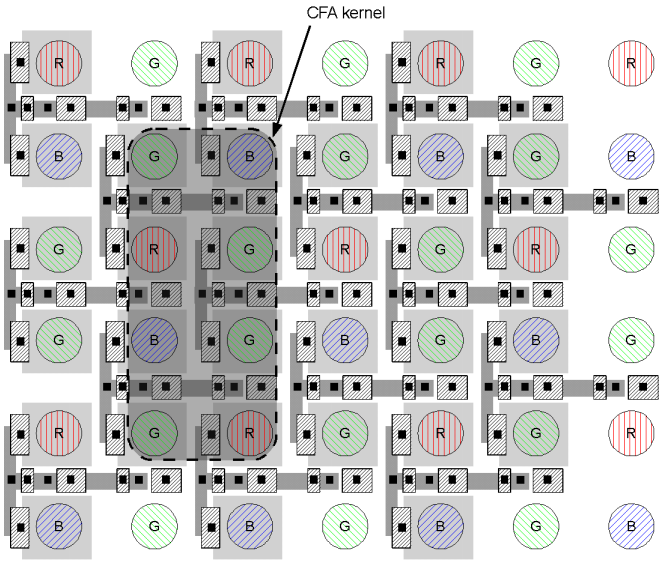

Figure 9. Possibility for binning to complementary colors in two-shared pixel array with staggered readout.

III. Results

The layout of a small portion of the array (pixel pitch of 3.1 µm) is shown in Figure 10. Note that the layout of all the pixels is almost as identical as in case of non-shared pixels. Reset transistor M1 and the select transistor M3 have the same positions relative to an adjacent photodiode. In the unit cell block at the top of Figure 3, reset transistor M1 and select transistor M3 are each located at the left-hand edge of adjacent photodiodes. A dummy poly is added to match the relative position of source follower M2. M2 and the dummy poly are each located near the right-hand edge of adjacent photodiodes. The metal routing is also made as symmetrical as possible with only minor differences between sharing pixels to avoid different cross talk behavior.

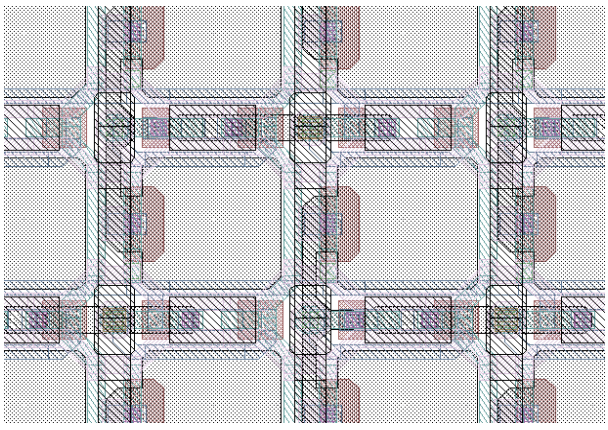

Figure 10. Layout of a small portion of the pixel array.

Table I summarizes the pixel performance that has been measured on a limited set of pixels of different size on a test chip. The test chip was processed in a 0.18 µm CIS 1P4M process.

TABLE I
ELECTRO-OPTICAL PERFORMANCE OF TEST PIXELS

Feature	Pixel pitch			
	3.2 µm	**4 µm**	**5 µm**	
technology	0.18 um CIS 1P4M			
full well charge (FWC)	15	48	85	Ke-
dark read noise	3.9	5.8	6.1	e-
QE x FF w/o µlens	35	54	56	% (@ 550 nm)
linear dynamic range	71.7	78.4	82.9	dB
image lag	< 0.1	< 0.1	< 0.1	%
dark current	50	57	77	e-/s @ 30 C

The first prototypes of the full size sensor are currently being processed at the foundry. First characterization results are to be expected by the end of May 2009. The pixel has been further optimized in terms of sensitivity (fill factor and conversion gain) and increased full well charge.

IV. Conclusion

Sharing of readout circuitry for vertically adjacent pixels has some advantages in terms of speed, power consumption and electro-optical performance compared to non-shared pixels. Shared pixel layouts traditionally require approximately half of the interconnect lines of non-shared pixels, and are therefore expected to have better yields (e.g. in terms of shorts between metal lines since less interconnect lines are vulnerable to defects). However, the conventional sharing approach is susceptible for single defect lines. A defect line immediately would result in non-correctable defect lines for the envisaged application.

The new sharing approach that is discussed in this paper does not result in an increase of non-correctable pixel lines while maintaining some of the advantages of sharing. It also leads to symmetric pixel layouts, resulting in a similar MTF for the different pixels with shared readout transistors. This is not the case with conventional implementations of shared pixel layouts.

The combination of sharing readout circuitry and staggering can also be used to further increase the final device yield in high resolution and large area devices where the area that becomes available because of the sharing is used to add redundancy into the circuitry.

The advantages of the architecture were discussed for monochrome as well as for color devices for which various color filter arrangements are possible. Binning of color pixels is also feasible with the proposed pixel architecture.

References

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