Limitations to the frame rate of high speed image sensors

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Abstract

This article studies the speed limitations to the access of pixels arranged in a pixel array of high-speed CMOS image sensors. It models the frame readout time in function of ROI and focal plane array dimensions. It also suggests measures to reduce pixel array access time.

1. Introduction

The introduction of CMOS image sensor technology has accelerated the development of high frame rate image sensors, which are used in broadcast, sports and research applications, and in motion and impact analysis. The CIS architecture allows exchanging resolution for frame rate. Small windows or regions-of-interest in the image can be read out at higher frame rates. Furthermore, the CIS architecture achieves faster frame rates than CCDs, due to the in-pixel charge-to-voltage conversion and the fast multiplexing of voltage signals in CMOS circuits. The speed advantage offered by scaling as described in Moore's Law can be fully exploited in the design of high-speed CMOS image sensors, which has lead to a continuous increase in sensor speed [ref. 1…5]. High frame rates are achieved by massive parallelism, through the use of multiple output channels. Traditionally the maximum frame rate achievable by a CMOS image sensor is determined by the maximum data bandwidth in the column multiplexers or output amplifier, or by the maximum data rate of the column or output stage AD converter. This limitation could be eliminated by design measures, like pipelined operation of pixel sampling, column AD conversion and column readout; by the development of faster column ADCs; or by massive parallel readout circuits. The fundamental limitation for the frame rate is then imposed by the time to sample the signals from the pixel array into the column amplifiers. With increasing resolution and focal plane area, this pixel access time becomes larger due to increased load capacitances of the pixel control and readout lines. Also in region-of-interest (or ROI) readout mode, the pixel access time is a considerable part of the time to read out the ROI. This article studies what can be done to fasten pixel access time in CMOS image sensors. The article starts with modeling of the pixel access time, and continues with various methods to reduce this time.

2. Modeling of the pixel access time and CIS frame rate

A CMOS pixel for high-speed image sensors with typical control lines, output lines and a source follower as column line driver can be modeled as shown in Figure 1. High frame rate image sensors typically employ a global shutter pixel, and scan the image stored in an in-pixel capacitor at high speed. The capacitor is read out via a source follower and select transistor and one or more output busses. The pixel control lines can be modeled as distributed or lumped RC lines. For high-speed CIS, the select line is most important, since it must be operated at line frequency. Transfer, reset and sample signals operate only after image capture, which occur only once in each frame in global shutter pixel arrays, and can operate at slower timing. The select line should be designed for low load capacitance and resistance. Its capacitance is typically dominated by the gate capacitance of the transistor attached to the line. The delay can be modeled via distributed or lumped RC lines. When the select line switches on, the output line more or less follows the select line voltage, until select line voltage exceeds the voltage stored on the in-pixel storage capacitor. The required end-value on the select line for proper operation depends thus on the in-pixel voltages. Since this varies amongst the different types of global shutter pixels, the select line is modeled in this generic analysis as a simple RC network. We take 3RC as the settling time for the select line, which is somewhat arbitrary, but satisfactory for a generic analysis. This gives the following settling time for the select signal:

$$t_{sel} = 3 \cdot x \cdot R_{sel} \cdot x \cdot C_{sel} \qquad (1)$$

with x the number of columns, R_{sel} the resistance of the select line in one pixel, and C_{sel} the capacitance of the select line in one pixel.

The speed of the source follower is determined for small signals by its transconductance (g_m) and the load capacitance. However, for large falling signals, like fore example the typical case in 4-T charge transfer pixels where the photosignal immediately follows after the reset level output, the

sample time is dominated by a slew-rate limitation, which is influenced by the bias current and load capacitance only. For high-speed image sensors, double sampling is sometimes avoided due to the double data rate on the column busses. But also in that case, the worst case (slowest) settling time appears when switching from a dark pixel on a row to a saturated white pixel on the next row. This means that, in worst case, the source follower settling time is simply described by:

$$t_{sf} = \frac{y \cdot C_{col} \cdot \Delta V}{I_{col}} \qquad (2)$$

with y the number of rows in the array, C_{col} the capacitance of the column line in one pixel, I_{col} the bias current on the column line, and ΔV the max. voltage swing at the output of the pixel. This worst-case value must be taken as the baseline for the timing of the pixel array.

Note that neither the RC delay of the select line (eq. 1), nor the speed of the source follower (eq. 2), is influenced by the ROI window size. The following equation can be derived for the frame readout time t_{frame} in function of resolution and ROI window size:

$$t_{frame} = n_x n_y t_{pix} + n_y (x^2 3 R_{sel} C_{sel} + y \frac{C_{col} \Delta V}{I_{col}} + t_{colADC}) \qquad (3)$$

in which n_x & n_y refer to the ROI size, x and y refer to the number of columns and rows in the pixel array, t_{pix} is the period of the pixel output clock, and t_{colADC} is the time that the column AD converter needs to digitize the row. The first term in the formula refers to the output bandwidth limitation, the second and third term refer to the time to read the data of the pixel array into the column amplifiers. The fourth term in equation (3) is applicable only when a column AD converter is used, it may be eliminated or reduced through pipelining of the column AD conversion process and the pixel sampling process. The first term can be eliminated similarly by pipelining the pixel array sampling (or AD conversion) and the column multiplexing. For high-speed image sensors, we assume that this pipelining is present, and the equation simplifies to the terms related to pixel array access time only:

$$t_{frame} = 3 n_y x^2 R_{sel} C_{sel} + n_y y \frac{C_{col} \Delta V}{I_{col}} \qquad (4)$$

This depends on the ROI size but more on the size of the pixel array. For small ROI, n_x and n_y are small, while x and y remain large, meaning that the pixel array access time is dominant. With (C)DS operations, two pixel values are sampled from the array and the frame access time roughly doubles.

Figure 2 shows a practical example of frame rate versus ROI window size The chart shows the frame rate in function of the number of columns of the ROI for a 1.3 MPixel image sensor with 24 output channels at 50 MPixels/second, and a column AD converter operating at 2 µs conversion time. The maximum number of rows (1024) are assumed in the ROI. In full resolution the speed is limited by the output bandwidth. At ½ of the column resolution, the frame rate is limited by the AD conversion process. With a faster AD converter, the frame rate could increase up to 4000 frames/s for small ROI as shown by the dashed line. The pixel access time limits the frame rate to 4000 frames/s.

Figure 3 shows the max. frame rate calculated from the model of eq. (4), with input parameters applied from typical CMOS pixels with a small pitch (3 µm), and typical 0.18 µm CIS process parameters. Eq. 4 assumes pipelined multiplexing and pixel array sampling processes, in which the latter is dominant. The dashed line shows the frame rate for full resolution readout, which obviously decreases for larger array sizes due to the increased capacitive load in the pixel column lines and the increased delays on the pixel control lines. As indicated in the chart, the frame rate in ROI (windowed) mode decreases also for large focal plane arrays, even for the same ROI size. The pixel access time increases for large resolutions and focal plane areas. The largest resolution shown in fig. 3 is 64 MPix.

3. Techniques to reduce the pixel array access time

The model above only considers the basic case of a typical CIS global shutter pixel. High-speed image sensors require higher frame rates that require further optimization. Typically larger pixel sizes are used for reasons of light sensitivity, which allows implementing several tricks to increase frame rate. Most of them consist in either reducing the capacitance of a column, introducing more parallelism or implementing buffering or repeaters.

Parallelism in the pixel array is a first step. For instance, a second column bus could be used; each column bus being connected to only half of the column pixel (Figure 4). Since the dominant capacitance on the column line is typically the source diffusion of the select transistor, this halves the column line capacitance. A similar principle could be used with two parallel selection lines, which reduces the RC delays on the select lines by 50%.

Figure 5 shows various organization of the pixel array. In the classical organization, the column bus is continuous along the column. An obvious way to double the speed consist in splitting the column bus in two and read out the pixel array from both top and bottom sides (b). This allows only centered ROI readout, which is a disadvantage. Increasing the speed is possible by increasing the current biasing of the column; however there are practical limits like voltage drop aver supply lines, etc. The maximum bias current in the column lines is set by resistive drops in the bias and power and ground lines in the pixel array and column amplifier. When only a part of the columns is read out, the column bias current I_{col} can be increased in these columns and shut down the current sources in the unused column, thus not increasing the overall current (c). This fastens the pixel access time and results in higher frame rates in ROI mode.

A more drastic measure, which is helpful for large area high-speed focal plane arrays, is the inclusion of a second level buffer amplifier or repeater in the pixel array at regular locations. Such repeater replaces one of the pixels on certain locations. Information of the missing pixel is to be interpolated from neighbors. Ideally, repeaters are placed on a distance equal to the square root of the number of pixels on each column. In this way an equal capacitance of the output busses of the repeaters and the pixel outputs can be achieved. The pattern where the repeaters are placed could be staggered to allow for better pixel data interpolation at the place of the repeaters.

4. Conclusions

High-speed CMOS image sensors can be limited in frame rate in ROI mode by pixel access times, rather than output bandwidth. The article shows the relation between frame rate and pixel array parameters, and describes solutions to reduce this pixel access time.

References

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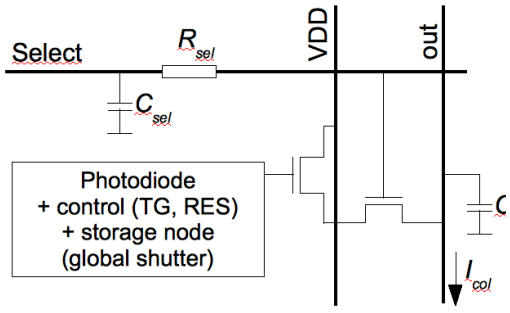

Figure 1: generic global shutter pixel.

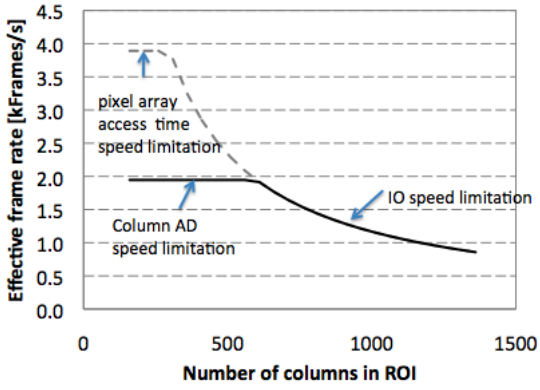

Figure 2: frame rate for 1280x1024 array in function of number of columns in the ROI.

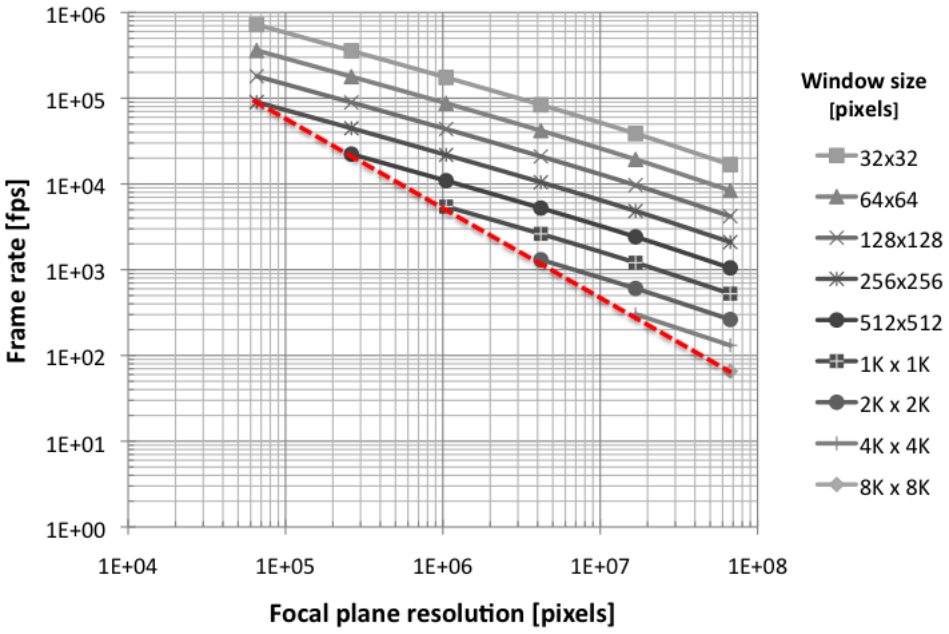

Figure 3: frame rate vs. focal plane resolution for various ROI window sizes for a typical 3 µm 4T pixel. The dashed line indicates the frame rate for full resolution.

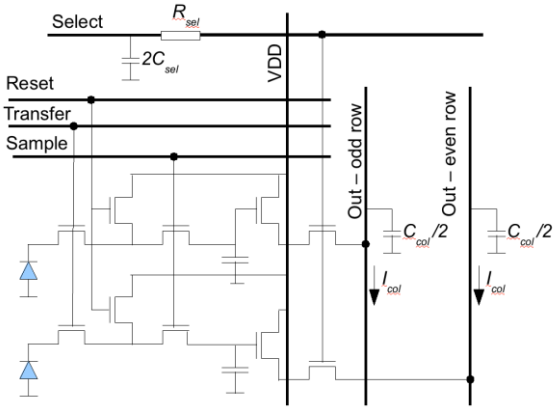

Figure 4: 5-T T-type global shutter pixel. Two output busses reduce column line capacitance by 50%.

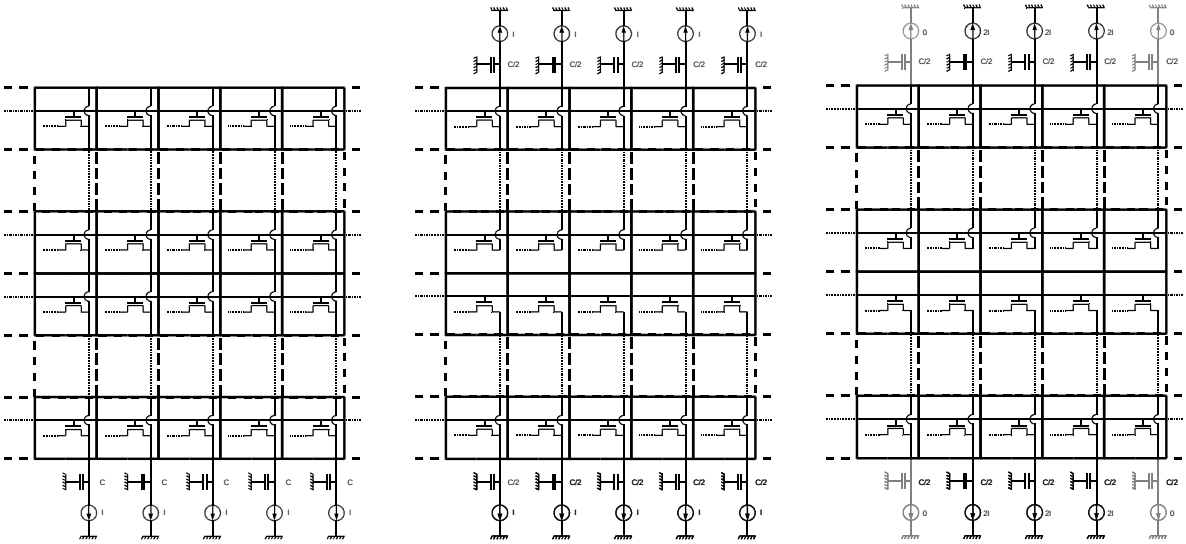

Figure 5: various organization of the array. (a) Classical. (b) Column split. (c) Switching of current sources of idle column with ROI readout.