The State-of-the-Art of Mainstream CMOS Image Sensors

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Abstract - The steady growth of mobile phones sales (feature and smartphones) has been the primary driver for CMOS image sensor (CIS) unit shipment growth over the last 3-5 years. As CIS market revenue has grown, so have R&D spending and patent filings. This effort has resulted in advanced mobile camera systems containing phase detection pixel arrays for fast autofocus (AF), ~1 µm generation pixels with improved low-light sensitivity, advanced chip-stacking, featuring a back-illuminated CIS wafer joined with an image signal processor (ISP) wafer, and video recording up to 4K. Innovation for smartphone cameras will continue, although given the competition for these high-volume sockets, many IDMs and fabless companies are developing chips for emerging, higher margin imaging applications such as automotive, security, medical, etc. These emerging opportunities are driving technology transfers from mobile imaging to these growth areas.

I. Image Sensor Market Conditions

The market for imaging chips continues to be in a growth phase. The consensus of many market research firms for the 2014 CIS market size is about $9 billion USD. Yole has predicted a 10.6% CAGR for the CIS market from 2014 to 2020 [1]. Of this total, it is estimated that Sony, Samsung, and OmniVision hold about two-thirds revenue market share, driven primarily by mobile phone and tablet camera chips. The mobile imaging market is expected to grow at a 13% CAGR from 2014 to 2020. The current market pull for mobile imaging systems includes: improved image quality, reduced power consumption, and faster AF.

II. Inventions: A Benchmark of Sector Maturity

Imaging companies, like all semiconductor companies, do face a number of risks. One risk is the potential for technology convergence leading to consolidation of overall market share, or for disruption within a sub-sector. Fortunately, the strong image sensor patenting growth trend [2] suggests continued opportunities for differentiated products.

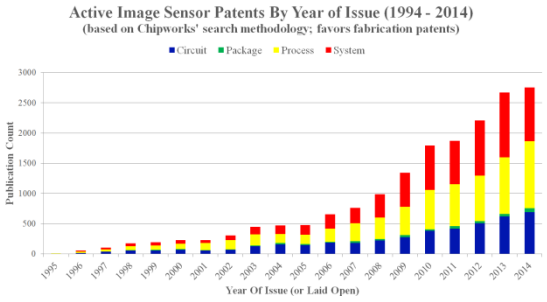

Fig. 1: Image Sensor Patent Trend Analysis (Favors Process Patents)

III. Evolutionary Technical Events: Isolation Schemes, Phase Pixels, Non-Bayer CFA

Most of the imaging chips designed in to marquee consumer products have used incremental evolutions of existing concepts. Noteworthy pixel structural optimizations include optical stack thinning and crosstalk suppression techniques. Panasonic's SmartFSI [3], which features light separation walls between the color filters of front-illuminated pixels, is a concept that has been adapted to recent back-illuminated CIS chips. The closest example is ON Semiconductor's (Aptina) Clarity+ chips, which feature color filters embedded in cavities etched in a blanket oxide film deposited over the back surface [2]. This structure, in effect, creates a per-pixel light pipe while matching the 1.5 µm record for optical stack thinness. The device analyzed does not use a metal aperture grid, but instead relies on the light pipe effect and microlenses for optical isolation.

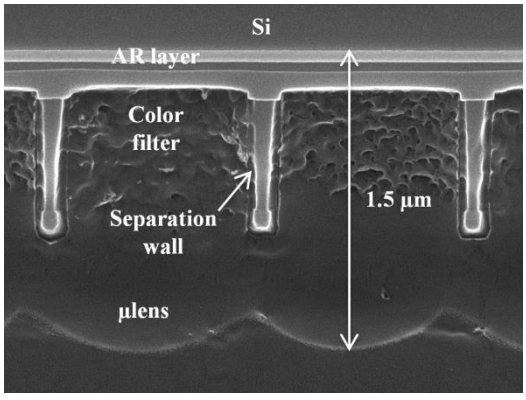

Fig. 2: ON Semiconductor (Aptina) AR0842 Clarity+ 1.1 µm Pixel

Sony and Samsung both use a back metal aperture grid and have similarly adapted the SmartFSI-like structure by embedding color filters into the grid metal. Previous generations from each manufacturer had used a gap-filling organic buffer layer beneath the CFA. Sony's implementation of embedded filters has resulted in a 1.5 µm thick optical stack for the co-record optical stack thinness (based on Chipworks' analysis) [4]. As reported by Sony [5], thinning the optical stack has improved the sensitivity of edge pixels.

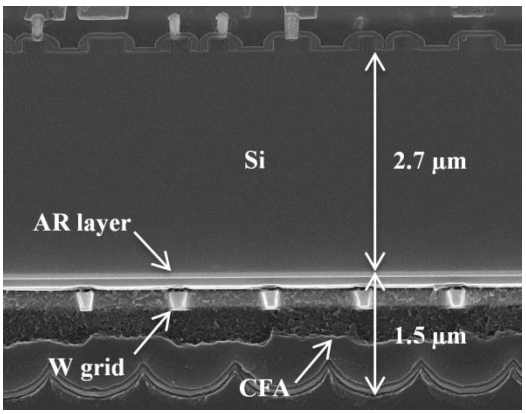

Fig. 3: Sony IMX214, 1.12 µm Pixel, Embedded Color Filter Array

Samsung's embedded color filters are comparatively thicker, resulting in a 1.9 µm optical stack thickness [6]. However, its strategy is to combine embedded filters with first generation deep trench isolation (DTI) technology to reduce electrical and optical cross-talk in the substrate. The first generation isolation trenches penetrate about 1.6 µm deep into the back of a 2.6 µm thick substrate. A hafnium oxide-based trench fill provides a charge trapping layer to passivate the Si surface and also serves as an anti-reflective layer. Samsung has announced further work to fully isolate each pixel with its ISOCELL technology [7].

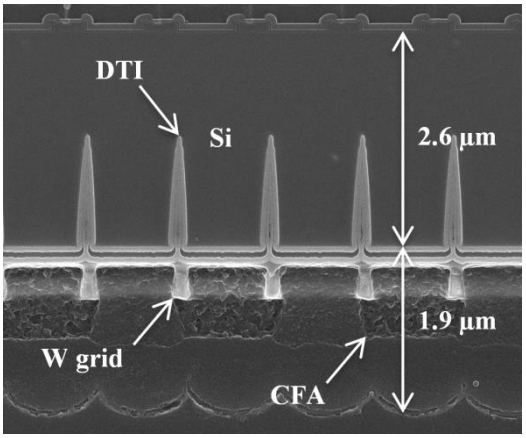

Fig. 4: Samsung S5K2P2XX, 1.12 µm Pixel, Partial DTI

The majority of phase detection systems rely on metal masking of proximate pixel pairs embedded in front- and back-illuminated active pixel arrays. A notable exception is Canon's dual photodiode solution which features four photodiodes per two shared pixels [8].

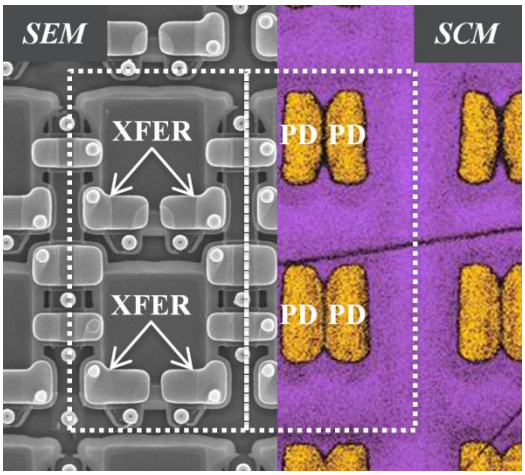

Fig. 5: Canon LC1290A (EOS-70D) 4.1 µm Dual Pixel CMOS AF

For those manufacturers with experience in constructing back-illuminated pixel aperture grids, the fairly recent requirement for phase detection pixel systems has been straightforward to address at the chip level. Examples of half-masked phase pixel pairs and multi-aperture phase pixels are in production. Green or clear filters are preferred for 1.4 µm and 1.12 µm generation phase pixels, while Sony has shifted from the green to blue channel for phase pixels on its 3.9 µm pixel generation APS-C chips [2].

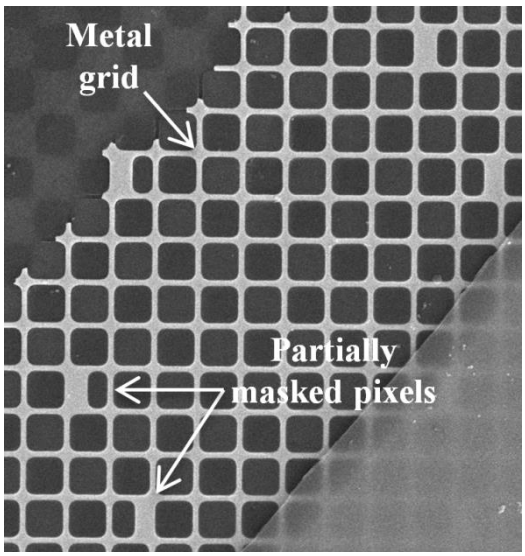

Fig. 6: Sony 8 MP, 1.5 µm 'Focus Pixels' from Apple iPhone 6 Plus

A substantial amount of engineering effort has also been directed towards the introduction of panchromatic pixels.

Both ON Semiconductor (Aptina) and OmniVision had design wins with 1.1 µm generation sensors using non-Bayer color filter arrays, however both required the use of a custom ISP at the systems level. The AR0842 features Clarity+ technology comprising a mix of 25% red, 25% blue, and 50% clear pixels [2]. OmniVision has incorporated diagonal rows of clear pixels into its proprietary RGB Clear color filter mosaic. Adjacent rows include a diagonal green channel and alternating pairs of blue and red filters.

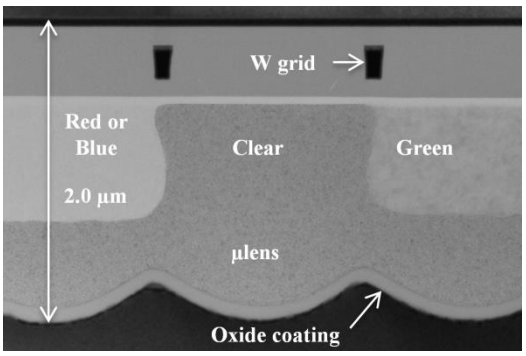

Fig. 7: OmniVision OV10820 RGB Clear (RGBC) 1.4 µm Pixel

IV. Disruptive Technical Event: The Emergence of the Stacked Chip CIS

The motivations for investing in stacked chip CIS development are somewhat varied depending on manufacturer [10], but can be summarized as: adding functionality, decreasing form factor, enabling flexible manufacturing options, and facilitating optimization for each die in a 3D stack.

Sony announced the world's first stacked chip CIS camera systems for consumer electronics in 2012 [11] and 8 MP ISX014 chips were found in a tablet computer in early 2013 [12]. The first generation chips employ via-last TSVs to connect pads from the Sony-fabricated, 90 nm generation CIS die to landing pads on a Sony-fabricated, 65 nm generation ISP. The die stack was partitioned such that most of the functionality of a conventional system-on-chip (SoC) CIS was implemented on the ISP die; the CIS die retained the active pixel array, final stage of the row drivers, and comparator portion of the column-parallel ADCs [13] [14]. Note that due to the mix of design rules, the comparator blocks on the CIS die are pixel pitch matched, while the companion column circuits on the 65 nm ISP die occupy a footprint about 25% narrower than the active pixel array.

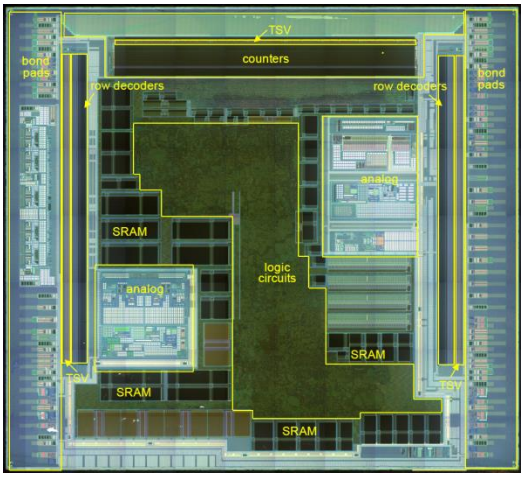

Fig. 8: Sony ISX014 8 MP Stacked CIS – ISP Die at Poly Level

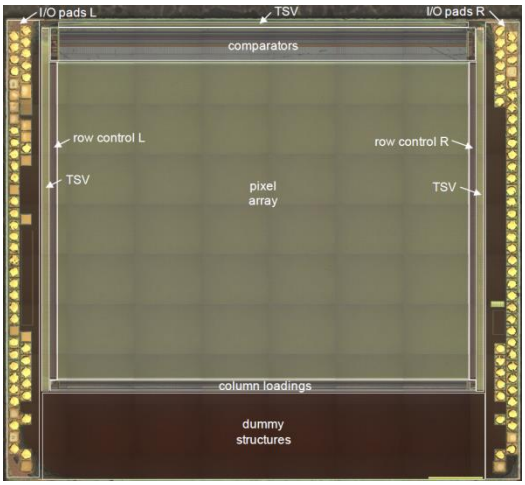

Fig. 9: Sony ISX014 8 MP Stacked CIS – CIS Die at Poly Level

Sony's 13 MP IMX214 second generation stacked CIS chips were similarly fabricated using its 90/65 nm (CIS/ISP) technology generation. However, in a continuation of its FLAT technology [14], first introduced in 2011 and observed in all small-pixel back-illuminated chips since, Sony simplified the IMX214 wafer flow by removing the STI process module entirely. The key work on the second generation stacked process was to evolve the CIS silicon for use solely as the active pixel array substrate and moving the entire column readout chain and peripheral transistors off-die to the underlying ISP.

In 2014 Sony demonstrated flexibility in choice of wafer vendors afforded by chip stacking by using TSMC as a foundry for the ISP on the Apple iPhone 6/6 Plus iSight cameras. These chips incorporate Sony 90 nm CIS wafers and TSMC 40 nm ISP wafers [2].

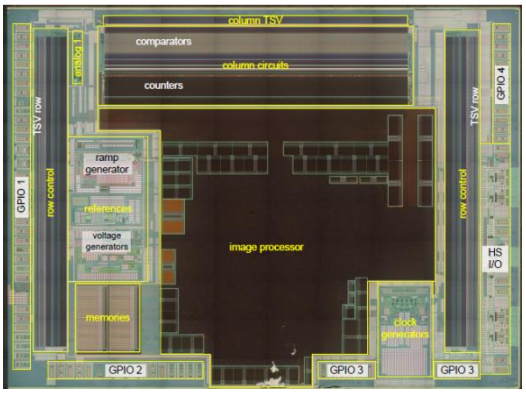

Fig. 10: Sony IMX214 13 MP Stacked CIS – ISP Die at Poly Level

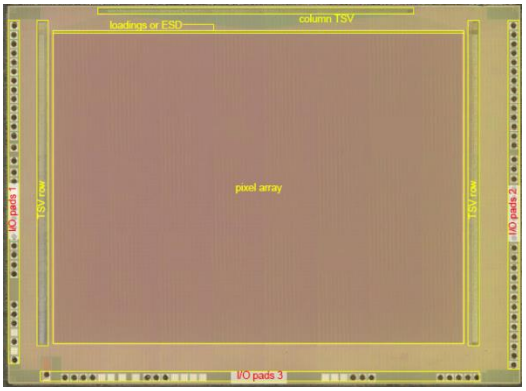

Fig. 11: Sony IMX214 13 MP Stacked CIS – CIS Die at Poly Level

Samsung and OmniVision have both been sampling small-pixel, stacked chip CIS and both are expected to have secured design wins within 2015. Highlights of near-term stacked chip product announcements include: >20 MP resolution, high-dynamic range, and on-chip phase detection pixel array. Additionally, OmniVision has announced the world's first 1.0 µm pixels [16] in a stacked chip process.

Given the continued, aggressive stacked CIS development underway from independent device manufacturers (IDM) and foundries it's predictable that stacked chip adoption will occur very rapidly over the next few years.

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