Back-side illuminated 28M-pixel APS-C sensor with high performance

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Abstract

We present the world first APS-C sized back-side illuminated (BSI) CMOS image sensor with 28 mega pixels and 3.6um-pitch. Combining low power 65nm Cu process and BSI technology [1], we design a high speed circuit which enables 120 fps frame rate with FHD resolution, resulting in world fastest APS-C sized CMOS image sensor. In order to secure high image quality, both the full well capacity (FWC) and maximum sensitivity are increased significantly up to 30,000 e- and 38,000 e-/lux·sec. We are also able to keep the dark characteristics such as dark current and dark random noise under control by optimizing device design and using an improved 65nm Cu process technology.

Introduction

Back-side illuminated (BSI) technology has been the dominant topic in CMOS image sensor (CIS) over last decade as pixel size shrinks close to one micron [1]. While most mobile CIS adopt BSI technology, it is widely believed that there is no necessity in case of large sensors such as APS-C and full frame (FF) sensors. However, as demand for high resolutions and faster speed grows, large-sized sensors are gradually facing unavoidable restrictions of FSI technology.

In this paper, we present the world first APS-C sized BSI CMOS image sensor with 28 mega pixels of 3.6 um pixel pitch. The sensor is fabricated based on 65nm Cu process technology, therefore operated at very low power even in its fastest mode. We show that fundamental pixel properties such as FWC and sensitivity are improved significantly from its FSI predecessor if normalized with respect to a pixel pitch while keeping the optical and dark properties of CIS under control.

High Speed Readout

Fig. 1 shows the overall architecture and data path of the sensor. The pixel array is composed of 3.6um x 3.6um unit size two-shared pixel and readout circuits are placed at both side of the pixel array with mirror symmetry. High-bandwidth data transfer circuit is connected after the ADC to serially transmit digital-converted data to the digital processing unit (DPU). Finally, the DPU outputs image data via serial I/O. The system achieve streaming bit-rate of more than 8Gbps and 1H time to be effectively halved to support FHD 120fps with pixels of 3256x1840.

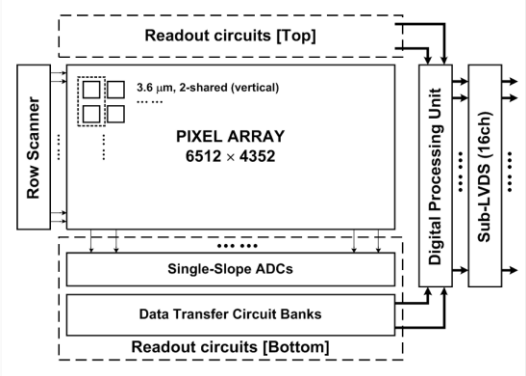

Figure 1. Overall structure of the chip.

In FHD mode, where there are more or equal recess columns compared to the active columns, multiple rows of pixels are processed simultaneously by re-using redundant readout circuits. In this design, 2-row simultaneous readout (2RSR) with 2-binning configuration implemented in industry-standard Bayer pattern is proposed, as shown in Fig. 2.

In order to enable 2RSR mode with 2-binning operation, a column pixel output line is split into two where respective select transistors per pixel output lines are present in a two-shared 4T pixel structure. Each of select transistors selects one of the two-shared pixels for A/D conversion and connects the source follower output to its corresponding pixel output line when turned on. An

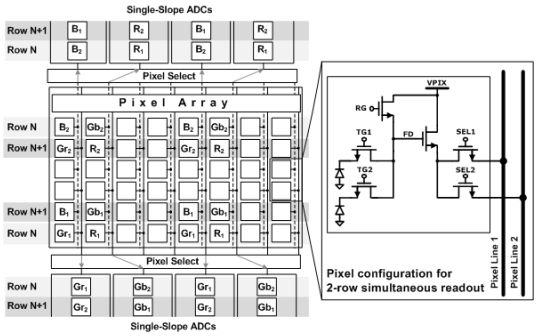

Figure 2. 2-Row Simultaneous Readout with 2-binning mode.

addition of a select transistor does not degrade pixel performance due to BSI technology. Using this configuration, two pixels of different rows in the same column can be A/D converted at the same time; twice the number of rows is readout in the given time window effectively doubling up the readout speed.

Properties of the pixel

The vertical structure of sensor is composed of optical layer, photodiode (PD), and metal layer as shown in Fig. 3 where we adopted a standard BSI process with several modifications that are necessary for improving characteristics of APS-C sensor. We choose thick silicon with carefully designed and simulated doping profile for PD in order to increase the FWC and sensitivity while suppressing electrical crosstalk and blooming. As a result, we are able to achieve the typical FWC of 30,000e- as shown in Fig. 4. We also obtain the maximum sensitivity up to 38,000e-/lux·sec by adjusting and optimizing the optical structure.

One of the advantages of BSI technology is the angular response (AR) due to its low stack height [2]. In order to maximize AR, BSI process consisting of micro lens (ML), color filter (CF), and anti-reflection layer (ARL) is carefully simulated and optimized. Furthermore metal grid is adopted to reduce optical crosstalk which is prevalent in BSI structure [3].

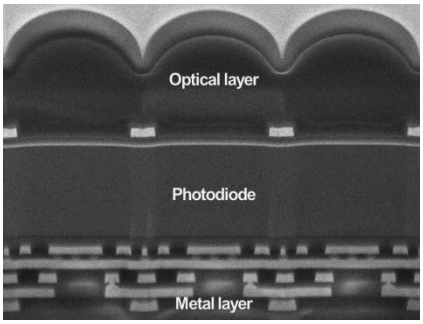

Figure 3. Vertical structure of the pixel.

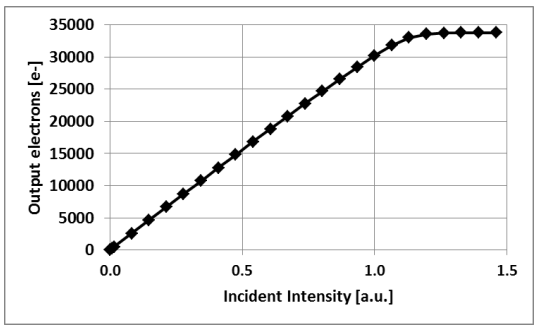

Figure 4. Full-well capacity

It is well known that controlling dark properties such as dark current and white spot defects are the key process in BSI technology since it results in more damage on silicon surface than FSI technology. Hence we apply carefully designed thermal annealing and implant process. In particular we apply thorough treatment on the both side of silicon surface as well as pinned photodiode (PPD) [4-6]. Therefore we are able to improve the dark current and maintain the white spot defects from those of FSI sensor.

In order to reduce the dark random noise (RN), not only the size of source follower (SF) is optimized but also the circuit is carefully designed. Combined with 65nm Cu process, we achieve an excellent dark RN compared to the predecessor as depicted in Fig. 5 and Fig. 6. Even though the size of source follower is smaller than its predecessor, our sensor shows improved dark random noise. In particular, RTS noise is reduced dramatically which was contributed from the quality of gate oxide and surface passivation technology of our 65nm Cu process. Furthermore, a new noise band limiting scheme in Fig. 7 is applied to achieve ultra-low noise sensor. The band limiter can suppress the readout noise about 30% and dark random noise can be achieved to 1.8e- at analog gain of 24dB.

We summarize the characteristics of our chip in Table 1.

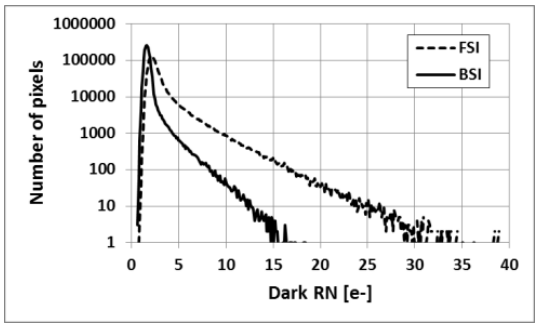

Figure 5. Histogram of dark random noise between FSI and BSI.

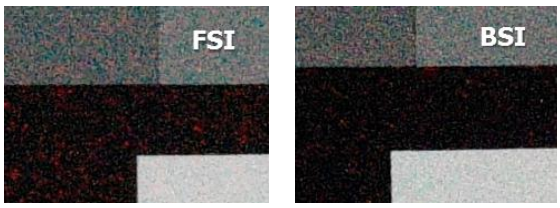

Figure 6. Comparison of dark random noise between FSI and BSI.

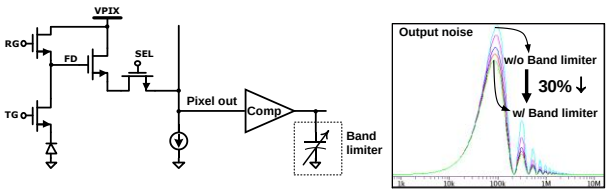

Figure 7. Schematic diagram of Noise Band limiter.

Effective pixels	**6496 (H) x 4336 (V)**
Pixel size	**3.6µm X 3.6µm**
Max. frame rate	**14fps at 14bit ADC**
Power consumption	**760mW at 14fps**
Full well capacity	**30,000 e-**
Sensitivity	**38,000e-/lux.s**
Image lag	**<1e-**
Dark random noise	**1.8 e- at 24dB**
Dynamic range	**77 dB**

Table 1. Chip characteristics

Conclusion

We produce the world first APS-C sized BSI CMOS image sensor fabricated in 65nm process technology. The sensor is able to operate 120 fps with FHD resolution. Full well capacity and sensitivity are improved and angular response is maximized due to the BSI technology. The dark properties are also enhanced dramatically after careful and thorough optimization.

Reference

[1] JC Ahn *et al.*, "Advanced Image Sensor Technology for Pixel Scaling Down Toward 1.0um (Invited)," *IEDM Dig. Tech. Papers*, pp. 1-4, 2008.

[2] K. Lee *et al.*, Int. Image Sensor Workshop, 2011.

[3] H. Wakabayashi *et. al.*, "A 1/2.3-inch 10.3Mpixel 50frame/s Back-Illuminated CMOS Image Sensor," *ISSCC Dig. Tech. Papers*, pp. 410-412, Feb. 2010.

[4] B. C. Burkey *et al.*, "The pinned photodiode for an interline-transfer CCD image sensor," in *Proc. IEDM*, pp. 28-31, Dec. 1984.

[5] E. R. Fossum *et al.*, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 2, pp. 33-43, May 2014.

[6] Y. Lee *et al.*, Int. Image Sensor Workshop, 2011.