

Recent developments on large-area CCDs for professional applications

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Introduction

Though CMOS is taking over from CCD in many application areas, CCDs are still the preferred solution for some very-large (>35mm format) imagers for professional photography and for large field-of-view digital aerial photogrammetry applications. This paper first focuses on some recent developments w.r.t. technology and design, and then presents a 60M-pixel CCD for photography and 32M- and 250M-pixel CCDs for aerial photogrammetry incorporating some of the presented new technology and/or design features.

CCD process and design basics

Our standard CCD process uses an n-channel CCD in a p-well on a n-type substrate for buried-channel operation with anti-blooming and electronic shuttering (draining of charge to the substrate) [1]. Two layers of transparent membrane poly-silicon gates are strapped with Tungsten. A second layer of metal (Al) is used for light shield and off-image interconnects [2]. The minimum litho dimensions are 0.35 μm . Typically, the four-phase bi-directional pixels of the full-frame CCDs are read-out through three-phase bi-directional readout registers to three-stage source followers.

New building blocks

We reduced the stack height in the pixel by 20% to maintain a good angular response with shrinking pixel sizes, Fig. 1. H1 was reduced to obtain a stack of 2.5 μm for H1 + H2. The results are shown in Fig.2 for a 5.2 μm pixel with color filters and microlenses, for the 'green' pixels under white illumination. No negative effects on speed, dark current, yield, etc. were observed.

At IISW 2009 [3], we presented a 12 μm pixel with very low dark current by surface pinning ("AGP", all gates pinning) for scientific applications. Based on this approach, we developed a 6 μm pixel for photography applications, Fig.3. The major challenge was to maintain a high charge capacity and dynamic range with a shrinking pixel size while maintaining excellent

anti-blooming and fast electronic shutter performance. We developed a new pixel concept, requiring only one additional channel implant, that can operate in conventional non-pinned mode ("mode 1") with high charge capacity (for low camera ISO settings), and in low-dark current mode with surface pinning ("mode 2") with slightly reduced charge capacity (for high ISO settings). The results are summarized in Table 1 and compared to the 'standard' pixel without surface pinning option.

The amplifier noise was decreased by optimizing the design and technology. The results are shown in Table 2. Additionally, we propose an amplifier with switchable conversion gain, Fig. 4. By adding an additional RG2, the FD capacitance can be increased for low ISO settings/ high charge capacity, whereas the performance in high-ISO mode is not compromised.

To maintain frame rates with increasing resolution, while maintaining the pixel frequency below 30MHz (application/customer requirement), two multiple-output options have been further developed. The first option is to use multiple taps on each side of the CCD. This was implemented earlier in a CCD for digital cinema with a 8.4 μm pixel [4]. The new implementation now supports pixel pitches down to 5.6 μm , Fig. 5. The challenge was in the design of the trapezoid area and the curved readout register. A second option is to use two parallel registers each at the top and bottom of the CCD for 4-line simultaneous readout, Fig. 6. Complete charge transport through the inner CCD register with a limited available clock swing of 5V was achieved, see Table 3.

60M-pixel CCD for professional photography applications with switchable pixel for large dynamic range or very low dark current

An existing 54mm x 40mm 60M-pixel FF-CCD with 6 μm pixels [5] was upgraded to a version that could additionally offer a very low dark current by implementing the dual-mode AGP pixel as described above (Fig.3). The key performance aspects are listed

in Table 4. The QE is compared in Fig. 7. The higher QE in green for the new pixel is a result of optical stack improvements. An image obtained with 1hr exposure time, at ambient temperature, is shown in Fig. 8.

250M-pixel CCD for aerial photogrammetry with 16 outputs

The CCD imager of 96mm x 82mm has 250M-pixels of 5.6 μ m (Fig. 9). Eight amplifiers each at the top and bottom of the image array – as shown in Fig. 5 - support the frame rate requirement of >1 fps while not exceeding 27MHz pixel frequency per amplifier. The pixels were designed to support forward motion compensation (FMC): during integration, the image can be transported over a few lines without compromising the anti-blooming performance or the charge capacity (TDI operation). The transition area between the image and the register and the curved register design was implemented without any degradation of performance, using only the existing metal-1 (Wm) and metal-2 (Al) interconnect layers. Fig. 10 shows an obtained image, and a zoomed-in detail. Table 5 summarizes the device characteristics.

32M-pixel CCD for aerial photogrammetry with two dual registers

This sensor has 32M-pixels of 5.2 μ m on a 36mm x 24mm image area. Both monochrome and RGB-color versions are available. The pixels have micro-lenses and were designed to support forward motion compensation (FMC). Dual registers similar to Fig. 6 were included in the design. No measurable charge loss or mixing occurs in the transport through the inner to the outer register. The pixel charge capacity of 45kel and output amplifier noise of 11el (at 25MHz pixel frequency, after CDS) result in a dynamic range of 72dB. The performance is summarized in Table 6.

Summary

Recent advances in technology and design for high-end CCDs for photography and aerial photogrammetry are presented, and the performance of several devices using selected new building blocks is shown.

Acknowledgments

The authors would like to thank their colleagues at Teledyne DALSA Semiconductor in Bromont (Quebec, Canada), for their valuable contributions to the technology development and manufacturing of the CCDs.

References

- [1] "A 36x48mm² 48M-pixel CCD imager for professional DSC applications", E.-J. Manoury et al, IEDM 2008.
- [2] "Very-low Dark Current in FF-CCDs", I. Peters et al., IISW 2009.
- [3] "A low dark current double membrane poly-Si FT-technology for 2/3 inch 6M pixel CCD imagers", H. Peek et al, IEDM 2009.
- [4] "Ultra-High Resolution Image Capturing and Processing for Digital Cinematography", A. Theuwissen et al., ISSCC 2003.
- [5] "Flexible binning structure for CCD color imagers", J. Bosiers et al, IISW 2009.

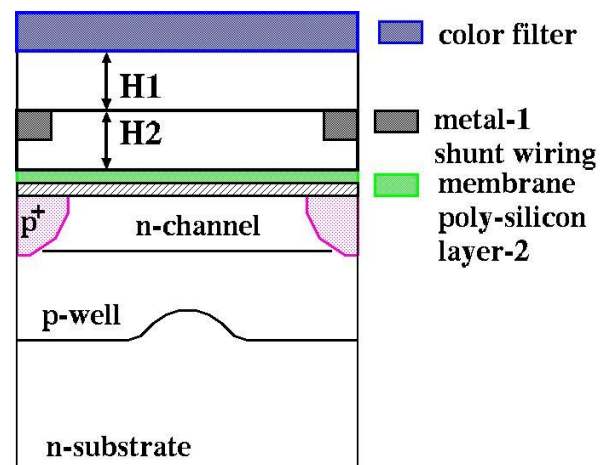


Fig.1. Stack height reduction.

| | Existing | New, Mode-1 | New Mode-2 |
|------------------------------------------|----------|-------------|------------|
| Number of phases | 4 | 4 | 4 |
| Number of integrating gates | 2 | 2 | 2 |
| Integration gate voltage (V) | 11 | 1 | -5 |
| Number of blocking gates | 2 | 2 | 2 |
| Blocking gate voltage (V) | 0 | 0 | -5 |
| Dark current (pA/cm ² , 60°C) | 100 | 100 | 2 |
| Electronic shutter Voltage (V) | 30 | 43 | 43 |
| Bi-directional transport mode | yes | yes | yes |

Table 1. Pixel performance overview of switchable pixel.

| | Old [1] | New |
|---------------------------------------------|---------|-----|
| Amplifier conversion factor (μ V/el) | 37 | 38 |
| Noise (25MHz, after CDS) (el) | 11 | 8 |
| Bandwidth (MHz) | 125 | 125 |
| Maximum charge capacity (5V RG swing) (kel) | 65 | 65 |

Table 2. Improved amplifier performance.

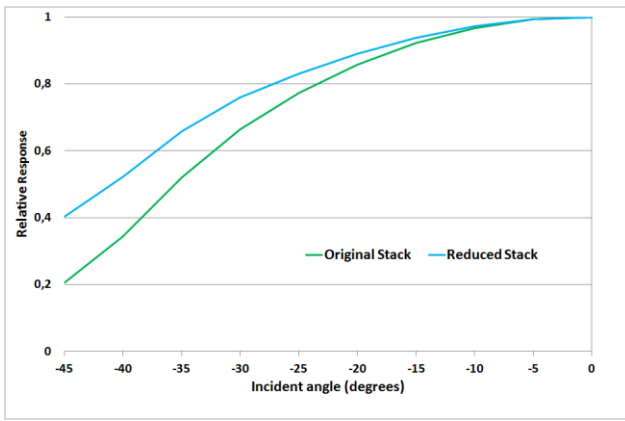


Fig.2. Angular response improvement by stack height reduction

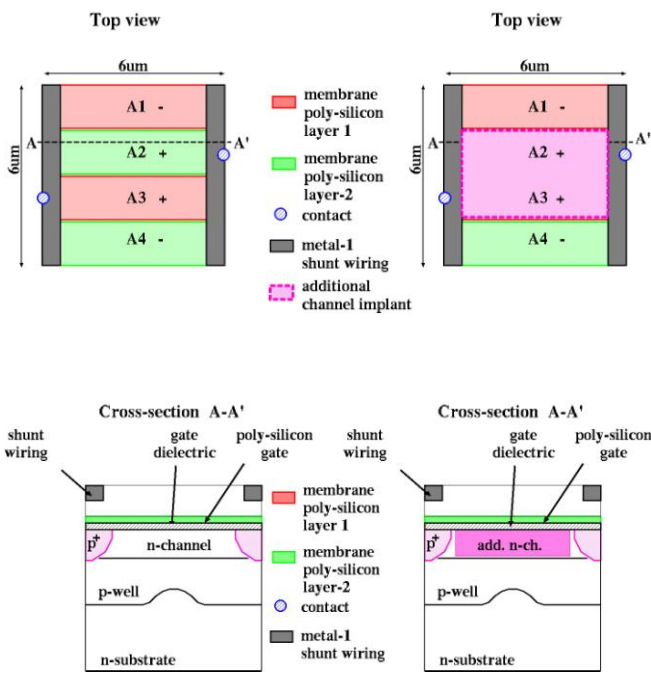


Fig.3. Pixel for switchable AGP (top view and cross section)

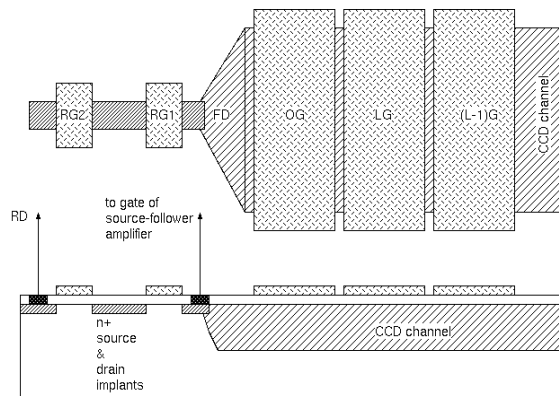


Fig.4. Concept of amplifier with switchable conversion gain.

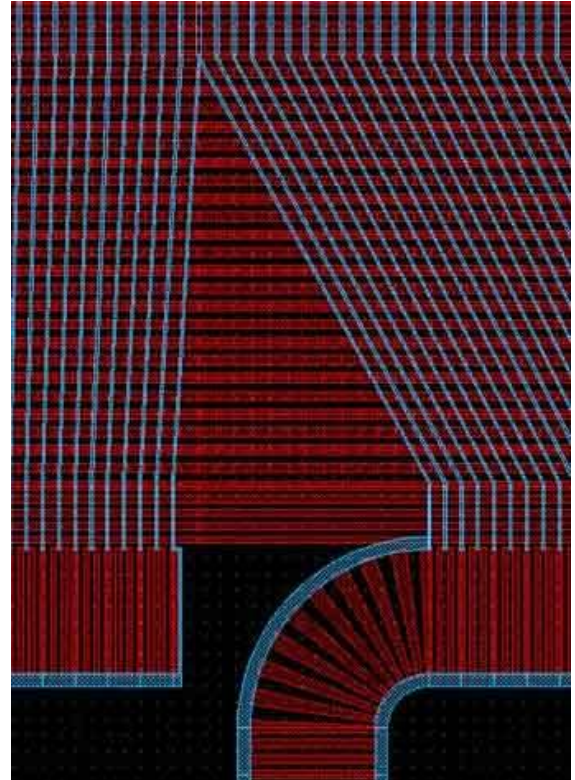
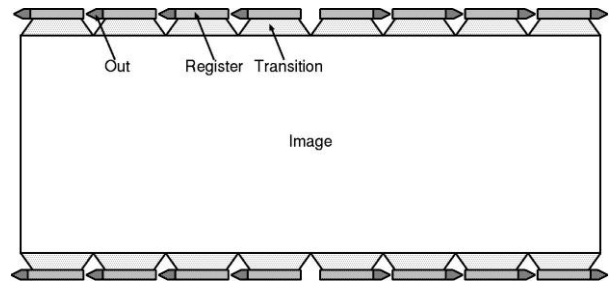


Fig.5. Multiple-tap concept (top) and detail of implementation (bottom).

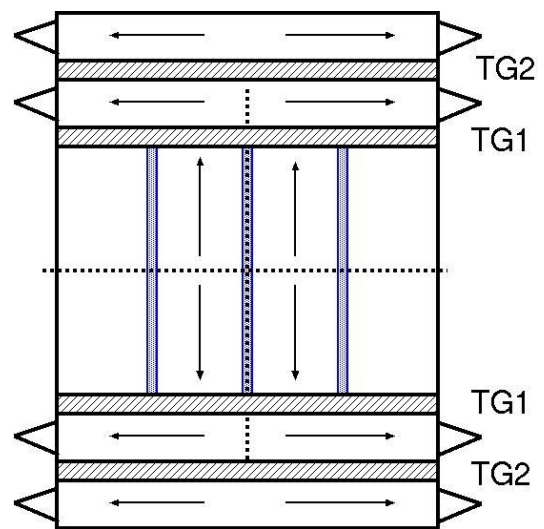


Fig.6. Concept of parallel CCD readout registers.

| | |
|----------------------------------------------|-------------------------|
| Pixel pitch (μm) | 5.2 |
| Number of readout register phases | 3 |
| Width of readout registers (μm) | 30 |
| Charge capacity (kel) | 65 |
| Transport loss (vertical) | Below measurement limit |
| Clock swing readout register gates | 5V |
| Clock swing transfer gate TG2 | 10V |

Table 3. Dual register results.

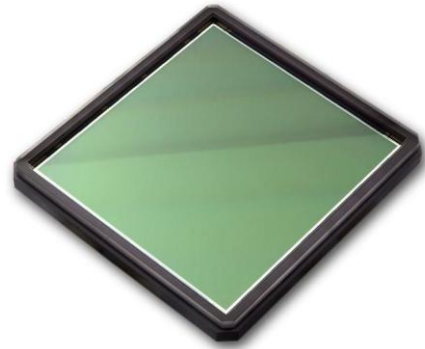


Fig.9. 250M-pixel CCD for aerial photogrammetry.

| | Original | New, Mode 1 | New, Mode 2 |
|-----------------------------------------|-------------|-------------|-------------|
| Image Area (mm^2) | 54 x 40 | | |
| Pixel size (μm^2) | 6 x 6 | | |
| Number of active pixels | 8976 x 6724 | | |
| H & V color binning | Yes | Yes | Yes |
| Maximum frame rate (fps) | 1 | 1 | 1 |
| Amplifier noise (25MHz, after CDS) (el) | 11 | 11 | 11 |
| Dynamic Range (dB) | 73 | 73 | 69 |

Table 4. 60M-pixel CCD key characteristics

| | |
|-------------------------------------------|---------------|
| Image area (mm^2) | 96 x 82 |
| Pixel size (μm^2) | 5.6 x 5.6 |
| Number of active pixels (H x V) | 17216 x 14656 |
| Number of amplifiers | 16 |
| Typical readout frequency (per amp) (MHz) | 27 |
| Maximum readout frequency (per amp) (MHz) | 30 |
| Maximum frame rate (fps) | 1 |
| Amplifier noise (27MHz, after CDS) (el) | 14 |
| Dynamic Range (dB) | 67 |

Table 5. 250M-pixel CCD key characteristics.

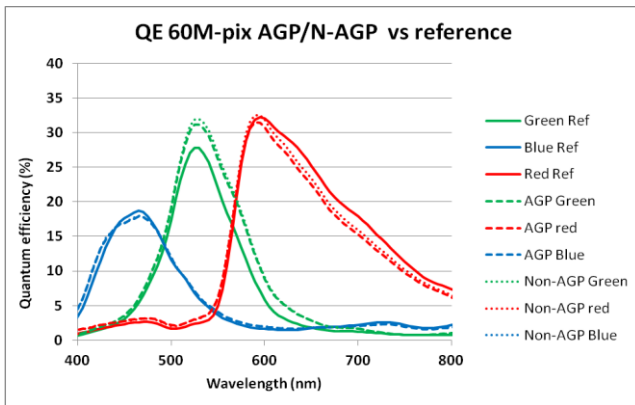


Fig.7. QE comparison of new low-dark current pixel with reference pixel.

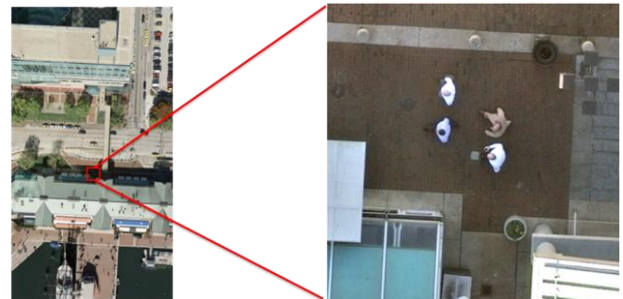


Fig.10. Image obtained with 250M-pixel CCD (left) and detail (right).

Courtesy Z/I Imaging.



Fig.8. Image made with 1h exposure time, ISO140, uncooled, with PhaseOne IQ260camera. Courtesy Digital Transitions.

| | |
|---------------------------------------------------------|-------------|
| Image area (mm^2) | 36 x 24 |
| Pixel size (μm^2) | 5.2 x 5.2 |
| Number of active pixels (H x V) | 6936 x 4616 |
| QE (green), monochrome sensor (%) | 37 |
| QE (green), color sensor (%) | 25 |
| Amplifier conversion factor ($\mu\text{V}/\text{el}$) | 33 |
| Amplifier noise (25MHz, after CDS) (el) | 11 |
| Linear Dynamic Range (dB) | 71 |
| Dynamic Range (dB) | 72 |

Table 6. 32M-pixel CCD key characteristics.