CMOS Charge Transfer TDI With Front Side Enhanced Quantum Efficiency

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Abstract—**This work focuses on the comparison of measurements done with two charge transfer TDI pixels showing a tradeoff between Quantum Efficiency (QE) and Full Well Capacity (Qsat). Both were successfully implemented in a standard CMOS 1P4M 0.18 CIS process. The Charge Transfer Inefficiency (CTI) has been improved by a factor of roughly 30 compared to previous work, making it suitable for industrial and space applications.**

I. Introduction

In the past years, the improved CMOS image sensors have started to take over from CCD technology. However, TDI applications are still a challenge for CMOS APS due to its intrinsic operating mode: charges are directly converted into voltage at the output of each pixel. In order to overcome this limitation, the standard approach consists of moving to digital summation: voltages are converted into digital words which are summed up as the scene is moving through the TDI array. However, the main drawbacks are the summation of noise and the ADC constraint on speed.

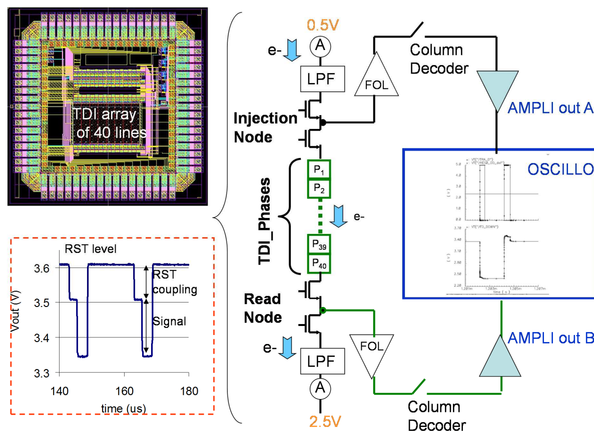

Figure 1 – Analogue Test Chip Presentation and output waveform measured on oscilloscope (bottom left).

The first part of the paper focus on two truly noise free charge transfer structures based on a standard CMOS technology. Analysis is carried out of QE (quantum efficiency), CTI (charge transfer inefficiency) and dark current measurements. The second part focus on the physical understanding of the necessity of using buried channel operation based on measurement and TCAD simulations. The last part focuses on the improvement of the charge transfer technology by proposing an innovative TDI architecture based on sub TDI arrays taking the best from analogue and digital summation.

II. Core Sensor

Two charge transfer structures (see Figure 2) were designed with a 13um pixel pitch, manufactured using a standard 0.18 IS 5V process with epitaxial wafers and embedded in a test chip with analogue outputs (see Figure 1). These structures are an updated version from the first work presented in [2-3].

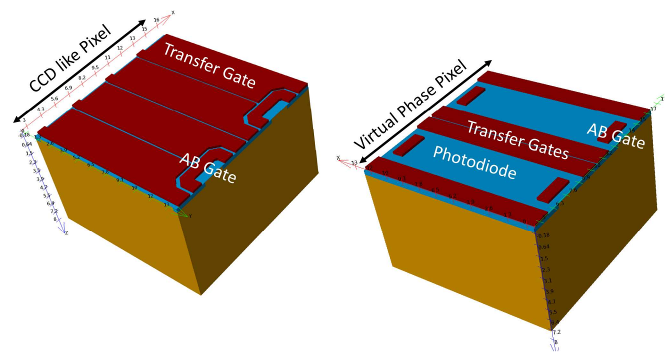

Figure 2 – (Left) CCD like pixel architecture with 4 phases per pixel (Right) Virtual Phase structure with 2 phases per pixel.

The first structure is based on a CCD architecture except the non-overlapping gates (only one poly level is available). The second architecture is based on photodiodes separated by two gates. Removing a part of the polysilicon area leads to higher QE [1] in front side especially in the blue wavelength range. Both structures operate in buried channel mode as explained in the next part of this paper. The operation principle of each pixel is explained in Figures 3 & 4. For the CCD like pixel, the carriers are stored under two gates during integration and under three gates during phase transfer. In the case of the Virtual Phase pixel, the carriers are stored in the photodiode during the integration and the gates allow a directional transfer by getting activated separately in time. In this example, the presented Virtual phase pixel is limited to 2 phases, but it can be extended to 3 or 4 phases (but there is some trade off with the full well capacity).

Both structures have been measured in terms of CTI, QE and dark signal. CTI is the most important parameter for charge transfer technology but also the hardest to achieve in CMOS technology due to the lack of overlapping poly layers and limited voltage swing. Thus the channel potential between gates is not well controlled and may lead to potential corners or barriers. The CTI is measured using a pulsed light source and measuring residual charges in the following dark pixels accordingly to this definition:

$$CTI = \frac{\sum_{residual} V_{empty}}{Nb_{stages}.V_{signal}} \qquad (1)$$

Where V_{empty} is the signal level of the dark pixels, V_{signal} is the level of the last illuminated pixel and Nb_{stages} is the number of TDI stages (here 40 lines). It should be noted that compared to a "classical" CCD, CMOS emulated CCD benefits from parallel column readout that eliminates the need for transfers in a serial register. This drastically reduces the number of transfers a charge packet has to make, relaxing the CTI requirements. As the digital conversion can be organized in CMOS with column ADC working in parallel, higher line rates are reachable compared to "classical" CCDs.

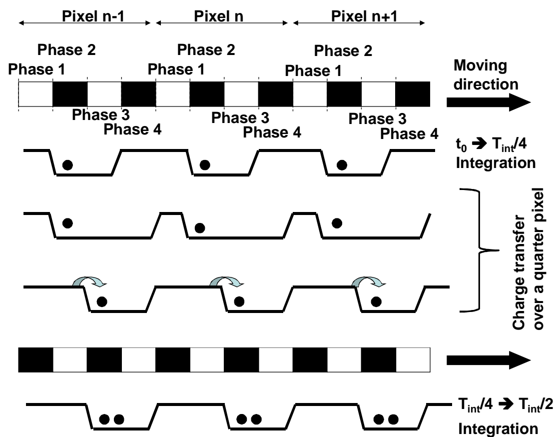

Figure 3 – **Potential well explaining the operation of CCD like structure.**

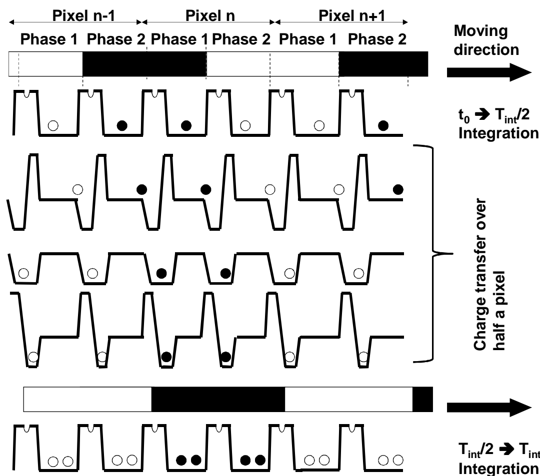

Figure 4 – Potential well explaining the operation of Virtual Phase Pixel Structure.

The CTI measurement is shown on Figure 5 for 2 variants of the CCD like pixel, a virtual phase pixel and a reference from our previous work [2-3]. The changing parameter between both CCD like structures is the interpoly gap (0.2um and 0.25um). Compared to our previous work, the CCD like structure (0.25um gap) has a CTI 10 to 50 times lower depending on the signal level down to ~3.10^{-4}. The main difference comes from the technology used: the previous one operates in surface mode and the transfer gates have N-type work functions, whereas the new one operates in buried channel and the transfer gates have P-type work functions. The explanation for this improvement is given in the next section based on our TCAD simulations. Reducing the interpoly gap allows a further decrease of a factor ~1.5-2 because of the better electro-static control between the gates but may lower the yield of large TDI arrays. The Virtual Phase pixel has the best CTI (~7.10^{-5}), at the limit of our measurement accuracy.

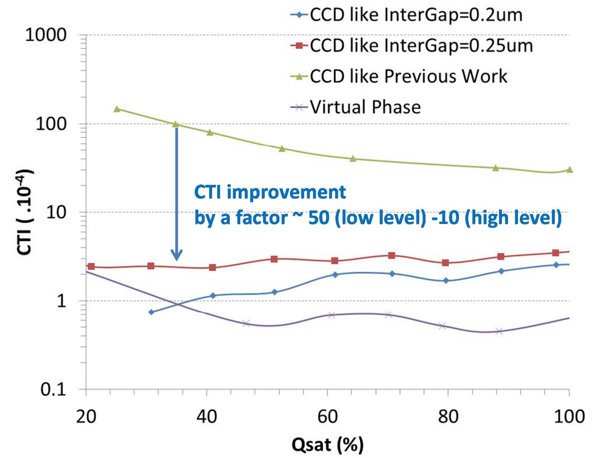

Figure 5 – CTI measurement as a function of the full well capacity (Qsat) .

Using the right pixel architecture with the right starting material allows tuning the QE as shown on Figure 6. In our previous work, we have shown that using a bulk wafer allows to increase the QE in the NIR part, whereas using of a Virtual Phase pixel increases the response in the blue part of the curve.

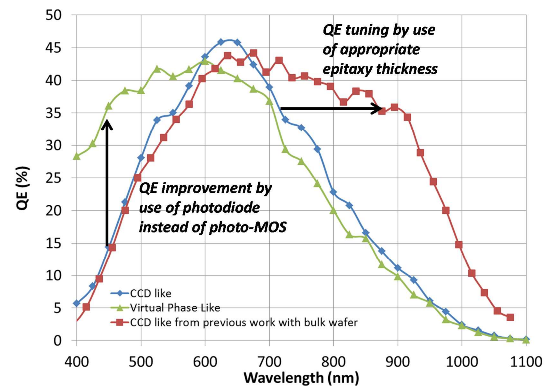

Figure 6 – QE measurement of CCD like and virtual structure. Reference [2-3] is also added

Compared to the CCD like structure, the Virtual phase pixel has lower CTI and better QE. However the Qsat measured on this pixel is poor (18ke-) compared to the CCD like (110ke-). This is due to the fact that the full well is limited here by the transfer gate storage capacitance during the transfer phase. It can be improved of course either by modification of the implant dose or by increasing the gate length at the expense of the photodiode leading to a trade off with the QE (at least if there is no ulens).

A comparison with our previous work and the state of the art is also added (see Table 1). The results are comparable but the strength of our work is to use a standard and industrial imaging process.

III. NECESSITY OF BURIED CHANNEL OPERATION

Using Surface channel devices is of interest in order to increase drastically the full well capacity of the TDI structure. This solution was used in our previous work [2-3] in which the Qsat is only limited by the read out path. We used a technology with flavor A, described by the fact that at 0V on the gate the P- epitaxial layer of Si was not in hole accumulation mode. In this new work, we switched to flavor B characterized among other things by the fact that at 0V, the Si moved to the hole accumulation mode when there is no buried implant. In this new work, we have designed both surface and buried channel devices. However the surface ones were total failures (almost no measurable transfer) whereas the buried ones behave correctly. To understand the discrepancy between the surface devices of our previous work and the new ones, TCAD simulations were undertaken. In CCDs, such kind of behavior can be attributed to the presence of traps located at the oxide/Si interface [6]. Thus in TCAD, we created a structure based on the flavor "B" with and without a buried implant (see Figure 7). These structures are then simulated with and without interface traps (density=$4.10^{11}cm^{-2}$ which is a high value used in this work for demonstration purposes as the simulations are done on a few transfer steps only).

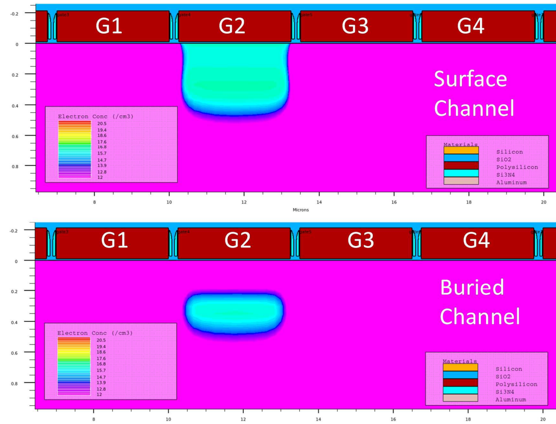

Figure 7 – TCAD structure used to evaluate the impact of traps on the signal in the case of a surface channel device (top) and a buried channel device (bottom).

Carriers are injected via a diode giving a reference potential value under the gate. This potential is then reported gate after gate on Figure 8. The reference device is the surface carrier structure without traps. The potentials remain flat showing a good transfer. Adding the traps leads to a linear increase of the potential showing a loose of carriers. The same simulation with a low potential of 0.9V (instead of 0V before) largely decrease the slope showing that only a few carriers are lost at each transfer. This low gate bias value is close to the threshold value of the transfer gates meaning that the Si is no longer in hole accumulation mode when switching the gate off. In both cases, carriers are in contact with the interface traps. But in the first case once the traps release the electrons, they get in a high density hole environment and they recombine. Whereas in the second case, the released electrons can either drift or diffuse back to the location of the main signal or form a trail of residual carriers decreasing the CTI. Biasing the low gate level at its threshold voltage is physically closed to what is happening in flavor "A". This explains why in our previous work the surface transfer devices were working whereas they do not in this work.

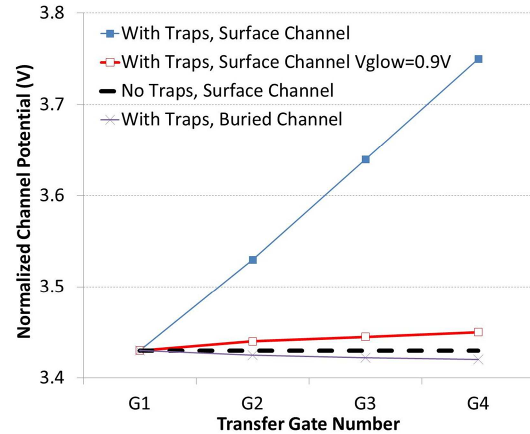

Figure 8 – Extracted Potential under the gates (G1-4) normalized to the level of the surface device: for surface devices with traps (operated between 0V/V_{high} & Vth~0.9V/V_{high}), for buried channel with traps (operated between 0V/ $V_{high'}$) and for a reference surface device without traps. Used trap density is $4.10^{11}cm^{-2}$.

Now looking at the buried devices, they do not show a significate potential variation as the carriers cannot interact with the surface located traps. Thus the TCAD has allowed us to explain the discrepancy between our previous and current work and showed that traps are responsible for the carrier loose mechanism of surface operated devices.

IV. PIXEL IMPROVEMENT AND FUTURE TDI ARCHITECTURE

In order to relax the constraints on the CTI and to optimize the full well capacity, a new "mixed" architecture can be used: the main TDI array is split into M sub arrays (in practice between 2 and 4) of N lines (see Figure 10). Each sub array is converted and summed up with the others. Thus, M digital summations are performed improving the full well capacity (Qsat) by a factor of M without adding too much noise (see Figure 11).

This means that we can tune the TDI focusing either on the saturation level (~maximum SNR, strong point of digital TDI) or the detectivity level (working at lower illumination level or higher speed, strong point of the charge transfer TDI). This tradeoff is shown in Figure 10 (for MxN=40 lines) based on the following dynamic range definition (where SEE stands for Saturation Equivalent Energy and NEE for Noise Equivalent Energy):

$$DR_{CCDlike} = \frac{SEE}{NEE} = \frac{Q_{sat}}{\sigma_{read}}$$

$$DR_{Digital} = \frac{M.N.Q_{sat}}{\sqrt{M.N}.\sigma_{read}} = \sqrt{M.N}.DR_{CCDlike}$$

$$DR_{mixed\,mode} = \frac{M.Q_{sat}}{\sqrt{M}.\sigma_{read}} = \sqrt{M}.DR_{CCDlike}$$

Furthermore, the charge transfers occur only through N lines instead of MxN leading to better overall charge transfer efficiency. This new architecture only comes at the cost of a few black lines between each sub array (for reading the sub TDI) and a higher ADC complexity. It can also be noted that if the number of lines are not the same in each sub-TDI (for example N_1 and N_2, N_2>N_1), then this architecture can be used to increase the dynamic by a factor N2/N1.

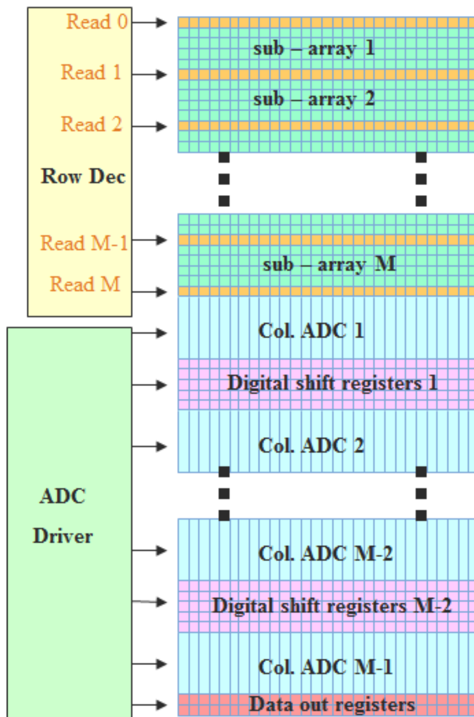

Figure 9 – Mixed TDI architecture.

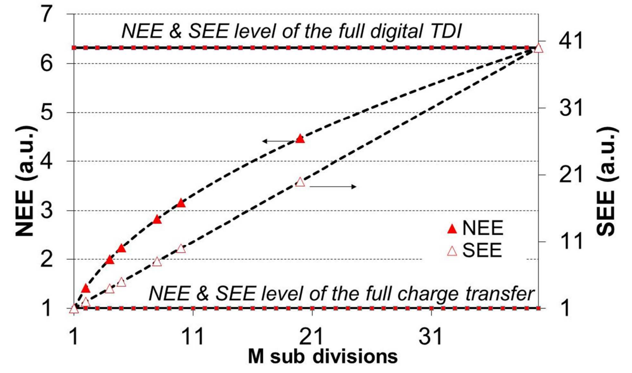

Figure 10 – NEE and SEE as a function of the number of subdivisions: in this example MxN=40 TDI stages.

V. Conclusion

In this work, we compare two structures able to operate with true noise free charge transfer that were fabricated with a standard CIS technology. Key performances were measured (QE, CTI, I_{dark}) suitable for commercial applications, especially when coupled with some design optimization allowing to combine multiple TDI to relax the CTI specification and to optimize the full well capacity.

References

[1] J. Janesick, J. Hynecke and M.Blouke, “A Virtual phase imager for Galileo”, proc. SPIE Vol. 290 (1981)

[2] F. Mayer, H. Bugnet, S. Pesenti, C. Guicherd, B. Gili, R. Bell, B. De Monte and T. Ligozat , “First Measurements of True Charge Transfer TDI”, ICSO 2012

[3] F. Mayer, B. Gili, H. Bugnet, F. Ramus, F. Devriere and T. Ligozat , “Measurements and Analysis of a 13um Pitch Charge Transfer TDI Suitable for Space Applications Using a Standard CMOS Technology”, CNES workshop 2013

[4] M. Popp, B. De Coi, and M. Ledergerber, “TDI System on Chip in OHC15L CCD / CMOS technology”, CNES workshop 2013

[5] A. Ercan, J. Robbelein, K. De Munck, K. Minoglou, A. Lauwers, L. Haspeslagh and P. De Moor, “A TDI Test Imager in Embedded CCD in CMOS Technology”, CNES workshop 2013

[6] M.F. Tompsett, “The Quantitative Effects of Interface States on the Performance of the Charge Coupled Devices”, IEEE Trans. On Elec. Dev., Vol. ED-20, No.1, 1973, pp. 45-55.

	Current work		Previous work [2-3]		ESPROS [4]	IMEC [5]
	CCD	Virtual	CCD	“Hammer Shape”		
Technology (um)	0.18		0.18	0.18	Modified 0.15	0.13
Pixel Pitch (um)	13		13**	13**	7.5	10
Inter Poly gap (nm)	200	250	250	250	Non Available	120
Qsat (ke-)	110	18	170	52	92	Non Available
CVF (uV/e-)	11		7	7	11	Non Available
Idark @RT (nA/cm^{-2})	12	2	10	6	2.6	Non Available
CTI	2.10^{-4}	7.10^{-5}	3.10^{-3}	$1.5.10^{-3}$	$\sim 10^{-4}$-10^{-5}	$\sim 2.10^{-5}$
Buried Channel operation	Yes		No	No	Yes	Yes
QE (%) @ 0.4/0.6/0.9um	2/45/10	30/42/10	2/40/40	10(35*)/45/40	10/80/80 (BSI)	85/85/20 (BSI)

Table1: Comparison with state of the art (*optimized through simulation, **also available in 7um)