A CMOS Image Sensor with 240µV/e$^-$ Conversion Gain, 200ke$^-$ Full Well Capacity and 190-1000nm Spectral Response

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ABSTRACT

In this paper, the structure and the performances of a CMOS image sensor with high conversion gain (CG): 240 µV/e$^-$, high full well capacity (FWC): 200 ke$^-$, wide spectral response: 190-1000 nm and high robustness to ultraviolet (UV) light are described. The developed CMOS image sensor was fabricated by introducing the following key technologies; small capacitance floating diffusion (FD) structure with lateral overflow integration capacitor (LOFIC) for pixel and a thin surface high concentration p$^+$ layer with steep dopant profile for photodiode.

INTRODUCTION

A high sensitivity, high dynamic range and a wide spectral response performance for image sensors are required by various fields such as security, scientific imaging and FA. Image sensors specialized in each of above mentioned performance were developed so far. It would be beneficial to image sensor users to develop an image sensor having all of the advanced performances simultaneously.

For obtaining a wide spectral sensitivity, several methods have been challenged [1-5]. It has been reported that a thin surface high concentration p$^+$ layer with steep dopant profile and a thick p-epitaxial layer in the photodiode (PD) is effective to obtain high sensitivity in a wide spectral range, from UV light to near infrared (NIR) light, and robustness to UV light [2-5]. In order to achieve high CG, ways to reduce FD capacitance (C_{FD}) have been reported [6-9]. Reducing the gate overlap capacitance and p-n junction capacitance are effective for reducing C_{FD} [8]. However, for general four transistor CMOS image sensor, C_{FD} reduction leads to a decrease on FWC. The lateral LOFIC technology was developed in order to achieve both high CG and FWC by a linear response under single exposure time [10].

These technologies have been developed independently, and above mentioned all performances have not been achieved simultaneously in a CMOS image sensor. In this paper, we demonstrate a CMOS image sensor with 240µV/e$^-$ CG, 200ke$^-$ FWC and 190-1000nm Spectral Response. The PD and circuit structures, operation sequence and measurement results of the fabricated CMOS image sensor are described.

DESIGN OF FABRICATED CMOS IMAGE SENSOR

In order to achieve high sensitivity to UV light, a thin surface high concentration p$^+$ layer with steep dopant profile was formed in the flattened Si surface. The CMOS image sensor was fabricated on p-epitaxial layer on n-type Si substrate. The thickness of the p-epitaxial layer was 20 µm to improve the sensitivity to NIR light.

For reducing the C_{FD}, it is critical to reduce the gate overlap capacitance accounting for the highest percentage of C_{FD} in conventional structure [8]. Then in the FD and the drain of the pixel SF, the implantation process of lightly doped drain (LDD) was removed. Therefore, a self-aligned n$^+$ diffusion was formed with an offset structure as shown in Fig. 1. It leads to the reduction of gate overlap capacitance. The implantation process of channel stop under FD was not carried out. This contributes to the reduction of p-n junction capacitance. Regarding the metal capacitance, since the pixel SF was placed near the FD, the wiring between FD and the pixel SF was short. Furthermore the other wirings near the FD were separated from it and these lead to a reduction of metal capacitance. Consequently, a high CG is to be achieved [8-9].

While reducing FD capacitance improves the CG, the FWC at FD becomes lower. For resolving this tradeoff, we introduced the LOFIC technology. Then, under a low illumination condition, integrated photoelectrons are completely transferred from the PD to the small capacitance FD, and high CG signal is read

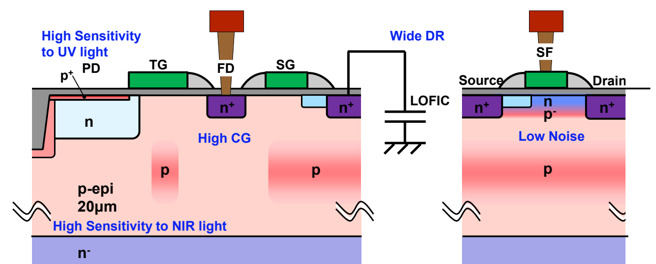

Fig. 1. Cross sectional view of the PD, transfer gate (TG), FD, S gate (SG) for the LOFIC and pixel source follower amplifier. The lightly doped drain wasn't formed at FD and drain of pixel source follower transistor.

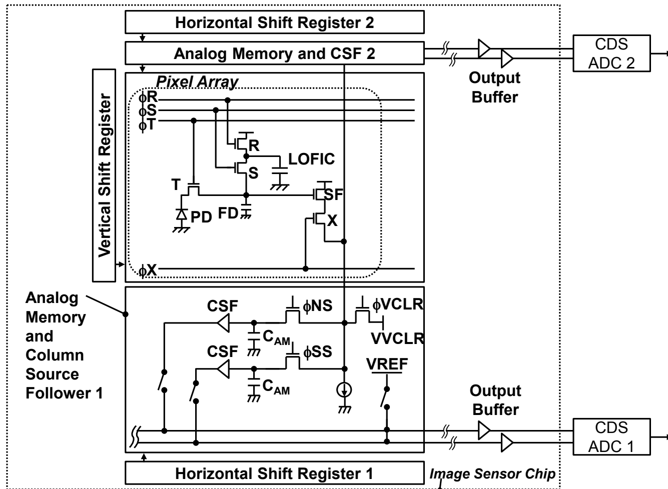

Fig. 2. Block diagram with pixel and column circuits.

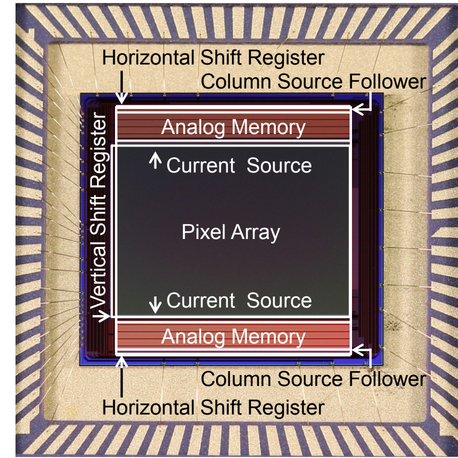

Fig. 3. Chip micrograph.

out. On the other hand, under a high illumination condition, saturated photoelectrons overflow from the PD to the small capacitance FD and the large capacitance LOFIC. And high FWC signal is read out. Since the CG and the FWC are determined independently, a high CG and a wide DR are achieved simultaneously. Additionally buried channel transistor was employed to the pixel source follower for low pixel noise.

Since these technologies are optimized independently, it is challenging to integrate them into one process. We have developed a CMOS image sensor process technology that integrated all of the above mentioned device components in a series of process flow. The orders of ion implantations and activation anneal process steps and their conditions were carefully chosen to optimize all of the performances simultaneously.

For the pixel circuit architecture, vertical and horizontal shift registers and analog memories were placed in the peripheral region surrounding the pixel array as shown in Fig. 3. The outputs from analog memories are amplified by column source follower drivers. The high CG signals: N1 and N1+S1 and high FWC signals: N2 and N2+S2 read out from each pixel are subtracted respectively at the correlated double sampling circuit. N1 and S1 indicate the reset noise and photo-signal at FD, and N2 and S2 indicate reset noise and photo signal at FD+LOFIC, respectively.

The fabricated chip micrograph is shown in Fig. 4. The supply voltage is 3.3 V. The pixel pitch is 5.6 µm. The number of effective pixels is 1280×960 pixels, and the fill factor is 30.4 %. The process technology was 0.18 µm 1-poly-Si and 3-metal CMOS image sensor process with buried pinned PD. The quartz was attached as the package lid to transmit wide light waveband to the sensor.

MEASUREMENT RESULTS AND DISCUSSION

Fig. 5 shows the photoelectric conversion characteristics of the fabricated chip. The employed light source was HDF-51F: Dainippon printing company using four fluorescent lights: FL15W. The vertical and horizontal axes indicate input referred effective signal electron and the relative illuminance, respectively. This graph consists of the S1 and S2 signals obtained under low illumination and high illumination, respectively. The device performances resulted in a high CG of 240 µV/e^-, a high FWC of 200 ke^- and wide DR of 101 dB. It was confirmed that a good linear response was obtained by one time exposure.

Next, spectral sensitivity and the stability of sensitivity toward UV light exposure were evaluated. Fig. 6 shows the measurement system of spectral response. The light source was ultra-high brightness and high stability broadband source EQ-99: Energetiq Technology Inc. The bandwidth of the light source was 190-1100 nm using the monochromator SPG-120UV: Shimadzu Corporation. Fig. 7 shows the spectral distribution of the deuterium lamp used for the UV light exposure stress. The typical UV light intensities are 82.9, 120.6 and 31.7 µW/cm^2 for the wavelength of 180, 204 and 300 nm, respectively. The UV light exposure stress was applied up to 220 hours. The total amount of the light source after 220 hour was 65.7, 95.5 and 25.1 J/cm^2 for the wavelength of 180, 204 and 300 nm, respectively. Fig. 7 shows the spectral response of the fabricated CMOS image sensor before and after deuterium lamp irradiation for 7, 26, 100 and 220 hours. For both cases, high quantum efficiency (QE) was obtained for a wide light waveband of 190-1000 nm. Especially the internal QE was almost 100 %

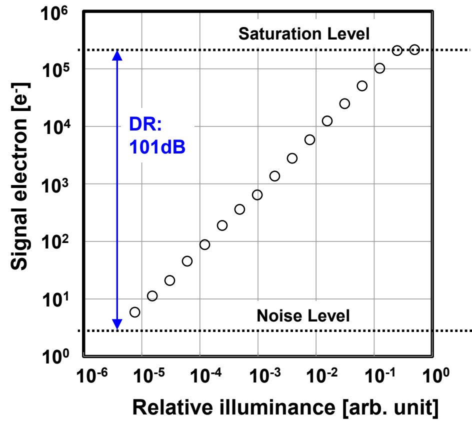

Fig. 4. Photoelectric conversion characteristic.

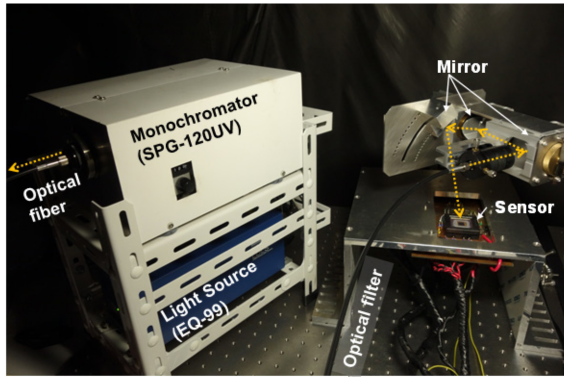

Fig. 5. Picture of spectral sensitivity measurement system.

in UV light waveband. Therefore, the sensitivity degradation after strong UV light exposure stress was negligibly small. The local swing of the spectral response is due to transmission characteristic of the oxide film above PD. Dark current degradation due to strong UV light exposure was not detected.

Fig. 8 shows the sample images captured by the fabricated CMOS image sensor under UV, visible and NIR light. The light conditions during image capturing were, (a) black light with band pass filter having a narrow distribution of waveband from 300 to 370nm, (b) D65 lamp with IR cut filter having a broad distribution from 300 to at least 800nm, and (c) NIR light without optical filter having a distribution peak at 940nm. A UV light transmission lens, PENTAX B2528UV was employed for capturing image (a). The left column images show a hand. In image (a), it was clearly observed that many spots absorbed UV light and in image (c) the blood vessel absorbed NIR light. On the other hand, the right column images show a flower. It was clearly observed that in image (a) the nectar guide absorbed UV light and in image (c) the flower reflects NIR light. The developed CMOS image sensor successfully captured images under UV light, visible light and NIR light with high sensitivity and high FWC performances.

TABLE 1 shows the design specifications and performances of the fabricated chip. The input referred CG is 240 μV/e$^-$, the total dark random noise is 1.7 e$^-$, the FWC is 2.0×10^5 e$^-$, and the DR is 101 dB. The spectral response range was for 190-1000 nm.

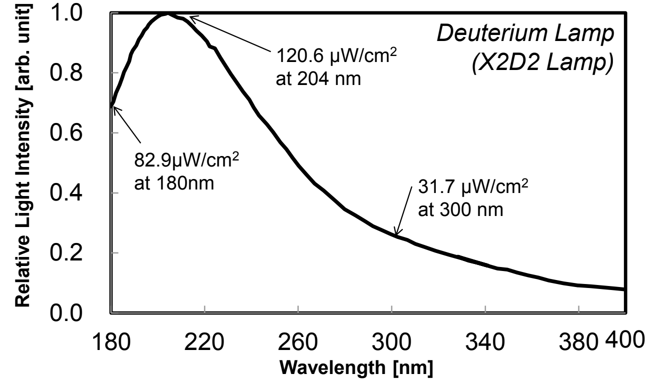

Fig. 6. Spectral distribution of the UV light source used for the UV light exposure stress.

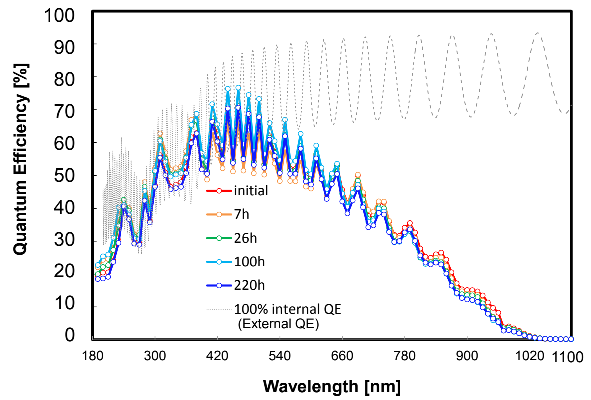

Fig. 7. QE of the fabricated CMOS image sensor's PD for 190-1100 nm performance after the deuterium lamp exposure stress for 7, 26, 100 and 220 hours.

TABLE 1. Design specifications and performance summary.

Process technology		0.18 μm 1P3M CMOS with buried pinned-PD
Supply voltage		3.3 V
Die size		$9.5^H \times 9.5^V$ mm^2
Pixel size		$5.6^H \times 5.6^V$ μm^2
# of pixels	Total	$1312^H \times 968^V$
	Effective	$1280^H \times 960^V$
Fill factor		30.4 %
Conversion gain		240 μV/e$^-$
Dark random noise		1.7 e$^-$
Full well capacity		2.0×10^5 e$^-$
Dynamic range		101 dB
Spectral sensitive range		190-1000 nm

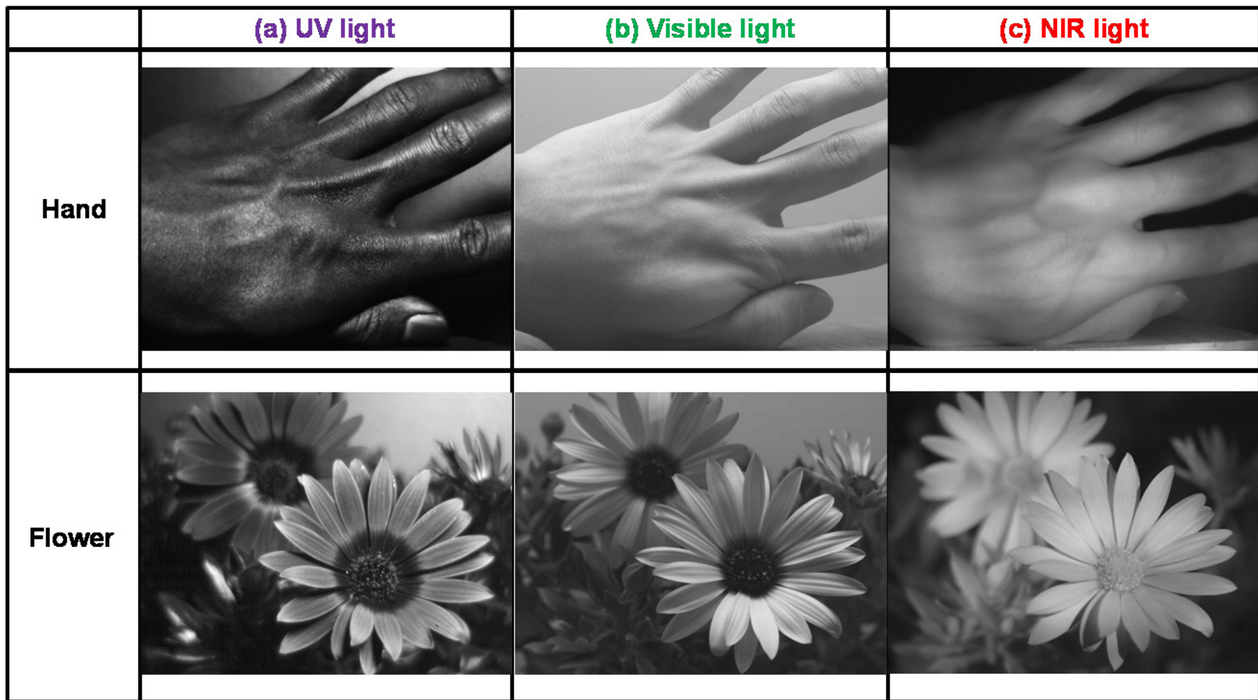

Fig. 8. Sample images under various light conditions. The light conditions during image capturing were, (a) black light with band pass filter having a narrow distribution of waveband from 300 to 370 nm, (b) D65 lamp with IR cut filter having a broad distribution from 300 to at least 800 nm, and (c) NIR light without optical filter having a distribution peak at 940 nm. An UV light transmission lens, PENTAX B2528UV was employed for capturing image (a).

CONCLUSION

A CMOS image sensor with 240 μV/e$^-$ CG, 200 ke$^-$ FWC, 190-1000 nm spectral response and high robustness to UV light was demonstrated by introducing the following key technologies; small capacitance FD structure with LOFIC for pixel and a thin surface high concentration p$^+$ layer with steep dopant profile for PD. The developed CMOS image sensor described in this work is expected to be utilized in various scientific and engineering fields.

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