A 2MP Oversampling Image Sensor with 2.75µs Row Time and Conditional Threshold Comparison

Thomas Vogelsang[*]*, Michael Guidash*[*]*, Craig Smith*[*]*, Jay Endsley*[*]*, Loc Truong*[+] *and Rami Yassine*[+] *(e-mail: tvogelsang@rambus.com)*
** Rambus Inc., 1050 Enterprise Way Suite 700, Sunnyvale, CA 94089, USA*
+ Forza Silicon Inc., 2947 Bradley St. Suite 130, Pasadena, CA 91107, USA

We present a 2MP CMOS image sensor that achieves a row time of 2.75µs by interleaving the pixel operations of three rows. A per-column sense-amplifier in combination with partial transfer allows comparing the pixel charge to a threshold and enabling conditional read. The fast row time enables implementation of 4x temporal oversampling with overlapping exposures at 80 oversampled frames (320 subframes) per second. This is equivalent to 30 temporally oversampled frames (120 subframes) per second in a 12MP sensor. Row address interleaving within a rolling shutter enables efficient implementation of any sequence of oversampled frame durations and exposure time selection.

I. Introduction

The dynamic range of a CMOS image sensor is normally limited by the full well capacity of its pixels.

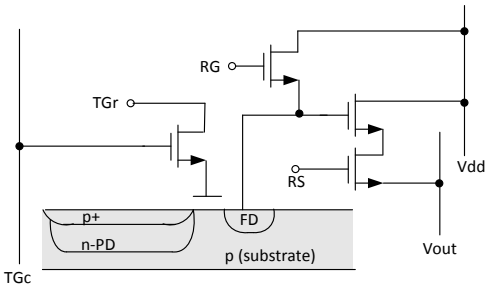

Fig. 1. Pixel circuit. The reset gate RG, row select RS, pinned photo diode and the transfer gate connecting the photo diode to the floating diffusion FD are the same as in a conventional 4-transistor pixel. The transfer gate is however not directly connected to the row parallel signal TGr. It is connected through a switch controlled by a column parallel signal TGc, thereby enabling per pixel control of the transfer.

The dynamic range is too low for many applications, especially for sensors with small pixels typically used for mobile devices. Some of us (Vogelsang, Guidash et al.) have proposed a conditional oversampling technique that increases the dynamic range by oversampling brightly illuminated pixels without affecting the sampling of pixels with weak illumination [1, 2]. A detailed description of the theoretical background of our approach is outside of the scope of this paper. It can be found in [2] together with an analysis of how our approach compares to other previous approaches found in literature.

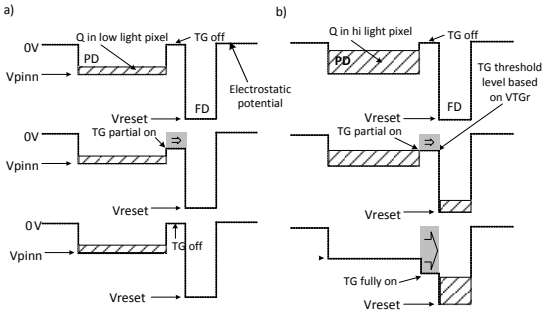

Fig. 2. Electrostatic potential. For below threshold illumination a) the partially turned-on transfer gate does not lower the potential barrier enough to transfer charge from the photo diode to the floating diffusion. Differently for above-threshold illumination b) the partially turned-on transfer gate transfers charge from the photo diode to the floating diffusion. This charge is detected by circuits outside of the pixel array, thereby triggering a full turn-on of the transfer gate.

Implementing our approach requires both fast row times and row scheduling that uses all available row time slots independent of the choice of relative subframe duration (sampling policy) and exposure time.

II. Theory of Operation

To achieve these targets we have implemented interleaving of row operations both on a micro-level (sequence of signals to pixel, sample and hold and ADC) and

on a macro-level (row addresses within a rolling shutter frame). We demonstrate these capabilities with a 2MP sensor designed to achieve a speed of operation sufficient for 4x oversampling of a sensor with 3,000 rows and 30 oversampled frames (120 subframes) per second.

The oversampling approach adds a threshold comparison to the sequence of a single row operation. It requires a pixel design which allows disabling the transfer of charge from the photo diode to the floating diffusion depending on the result of the threshold comparison. Figures 1 and 2 [3] illustrate the concept.

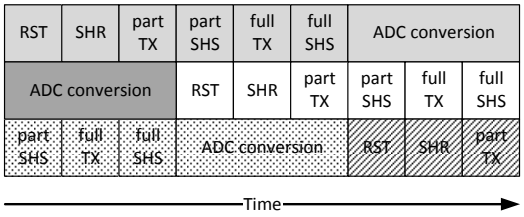

Fig. 3. Overlapping row operations. Each fill pattern represents a different row. The three horizontal bands in the figure refer to the three overlapping state machines running the row operation. The state machines share a sample-and-hold capacitor pair for the threshold comparison but have each their dedicated capacitor pair for the ADC conversion. The total duration of a row operation (floating diffusion reset – RST, sample and hold of reset – SHR, transfer gate operation with partial transfer voltage - part TX, sample and hold of partial transfer signal – part SHS, transfer gate operation for full transfer – full TX, sample and hold of full transfer signal – full SHS and ADC conversion) is three times the effective row time. At each point in time the row parallel pixel signals, the column parallel pixel signals and the ADC are only used by one row, so there is no conflict.

The total time needed for a row operation from the reset of the floating diffusion to the ADC conversion is nearly three times longer than the desired row time of 2.75µs. Figure 3 shows how three banks of sample and hold capacitors can be interleaved to achieve the target speed of operation and Figure 4 shows a block diagram of the architecture.

The macro-level interleaving is shown in Fig. 5. The photo diode reset and four read shutters for four subframes are rolled concurrently and overlapping. Four consecutive row times are reserved for the four subframes. Since each row time is assigned to a specific subframe, the duration sequence of subframes can be adjusted as desired. The reset and the four reads have independent row address pointers.

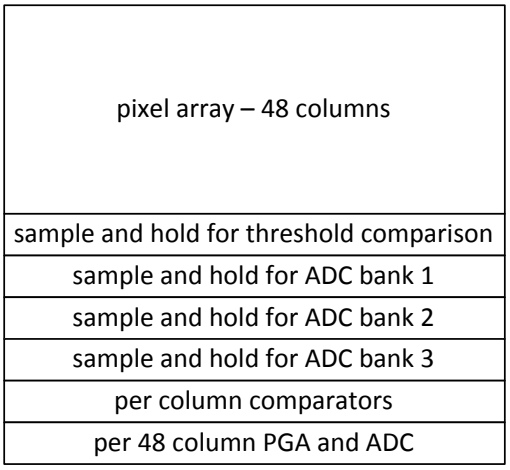

Fig. 4. Column circuit block diagram. One stripe of 48 columns width is shown in the block diagram. There are four banks of sample and hold capacitors, one to store the charge for the threshold comparison and three to store charge for ADC conversion. The sample and hold capacitors and the comparators are implemented per column; the PGA and a SAR ADC are shared between 48 columns.

III. Hardware Results

The hardware results below reflect the status of hardware testing at the time of submission of this text. Characterization has only started and is far from complete. Further results will be part of the slide set at the conference.

A photograph of the frontside of the die is shown in Fig. 6. The pixel array is 1920 x 1080 plus overhead with 1.4um pixels in a TSMC 65nm BSI CIS technology. The readout architecture is per-column comparators for the threshold assessment, per 48 columns PGA and 12 bit SAR ADC. The readout includes logic and memory to reduce power by suppressing conversion of pixels that are under threshold or saturated. Conventional readout (no oversampling) will run at 384 fps.

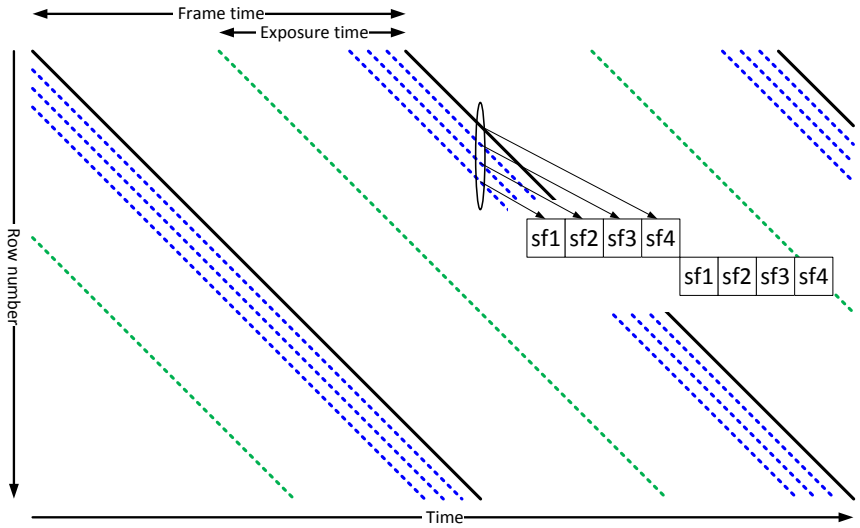

Fig. 5. Rolling shutter timing. The dotted green lines denote the rolling photo diode reset, the dotted blue lines the conditional reads with threshold comparison and the solid black lines the final unconditional read at the end of a frame. Simultaneous and overlapping operation of all four subframe reads is achieved by rolling packets of four consecutive subframe reads as shown in the insert. One independent reset and four read row pointers are used to implement this functionality.

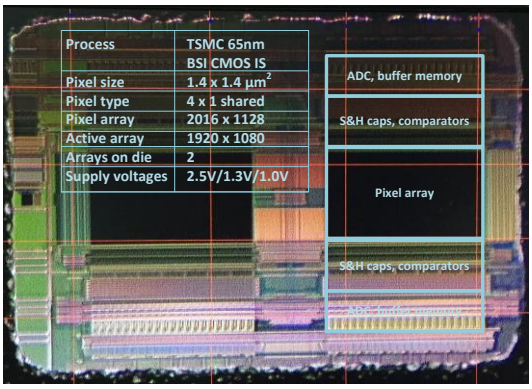

Fig. 6. Die photograph of the sensor front side showing main characteristics. The die contains two copies of the chip with identical periphery circuitry and two pixel variants.

The row and control logic of the test chip is implemented on an FPGA. It is therefore possible to trace the digital signals to the test chip by using Xilinx ChipScope™. Fig. 7 shows the traces of the signals to the die for a non-interleaved timing. The sequence of operations of floating diffusion reset, row select to read the reset level, partial transfer, row select to send the partial transfer level to the sense-amplifiers and full transfer can be seen. At the end of the sequence of operations for one row is a time slot for a photo diode reset of a different row to start integration of that row. The use of set and clear signals to control TG, RG and RS requires holding row addresses only during the assertion of set and clear, not during the whole row time, and thereby enables overlaying commands to different rows as shown in Fig. 3. This functionality is necessary to enable row interleaving.

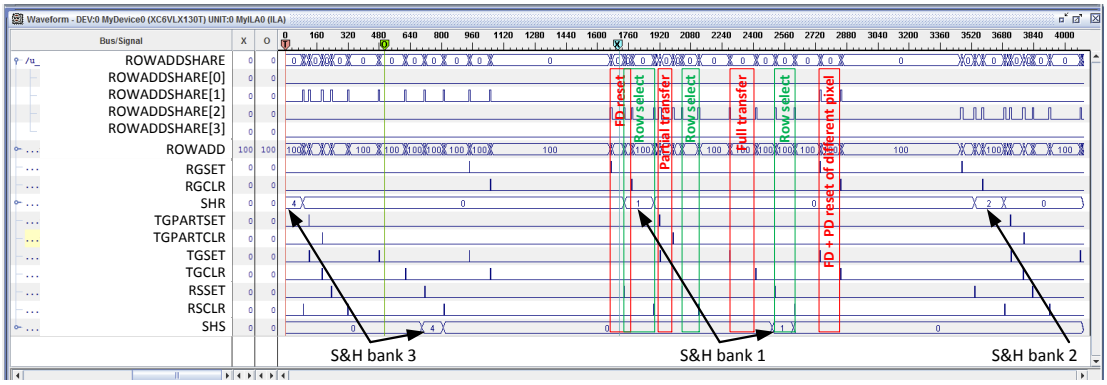

Fig. 7. Xilinx ChipScope™ snapshot of signals from the control and row circuitry on the FPGA to the test chip. In our implementation the MSB of the row address are given as address ROWADD while ROWADDSHARE is a one-hot selector between the four transfer gates sharing the same floating diffusion. Transfer gate TG, reset gate RG and row select RS are controlled by set and clear signals. The transfer gate is switched to the voltage for partial transfer when TGPARTSET is asserted prior to asserting TGSET.

Fig. 8 shows an oscilloscope trace of the pixel output line of one column. The row time is 2.72µs. The times of CDS reset (RST), read of the reset level to the sample and hold bank (SHR), transfer gate operation (TG) and read of the signal level to the sample and hold bank (SHS).

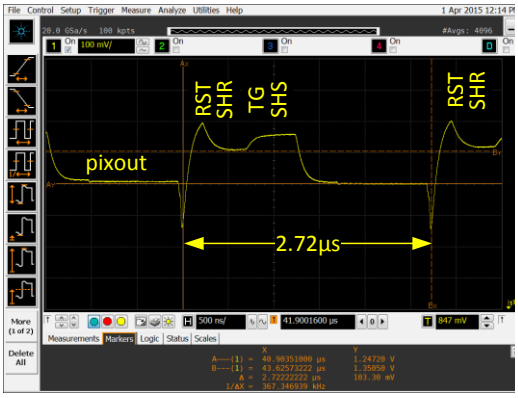

Fig. 8. Oscilloscope trace of the pixel output line of one column. The row time is 2.72µs.

This trace goes to zero in the second half of the row time as the source follower bias current is turned off during that time. In the timing variant with conditional reset TG and SHS will be moved into this free time to allow time for the sense-amplifier to assess the charge from partial transfer as described in Fig. 2.

Acknowledgement

The authors thank the design, test and characterization teams at Rambus and Forza and H. Y. Cheng and his team at TSMC for their support during this work.

References

[1] T. Vogelsang, M. Guidash and S. Xue, “Overcoming the Full Well Capacity Limit: High Dynamic Range Imaging Using Multi-Bit Temporal Oversampling and Conditional Reset,” International Image Sensors Workshop, Snowbird, Utah, USA, June 2013

[2] T. Vogelsang, D. G. Stork and M. Guidash, “Hardware Validated Unified Model of Multibit Temporally and Spatially Oversampled Image Sensors with Conditional Reset,” Journal of Electronic Imaging, pp. 013201-1 – 013201-13, Vol. 23(1), Jan-Feb 2014

[3] M. Guidash and T. Vogelsang, "Non-destructive threshold assessment of a pinned photo diode pixel with correlated double sampling," IEEE International Symposium on Consumer Electronics (ISCE 2014), Jeju, Korea, June 2014